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SRAM Cell Leakage Control Techniques for Ultra Low Power Application: A Survey

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Abstract

Low power supply operation with leakage power reduction is the prime concern in modern nano-scale CMOS memory devices. In the present scenario, low leakage memory architecture becomes more challenging, as it has 30% of the total chip power consumption. Since, the SRAM cell is low in density and most of memory processing data remain stable during the data holding operation, the stored memory data are more affected by the leakage phenomena in the circuit while the device parameters are scaled down. In this survey, origins of leakage currents in a short-channel device and various leakage control techniques for ultra-low power SRAM design are discussed. A classification of these approaches made based on their key design and functions, such as biasing technique, power gating and multi-threshold techniques. Based on our survey, we summarize the merits and demerits and challenges of these techniques. This comprehensive study will be helpful to extend the further research for future implementations.

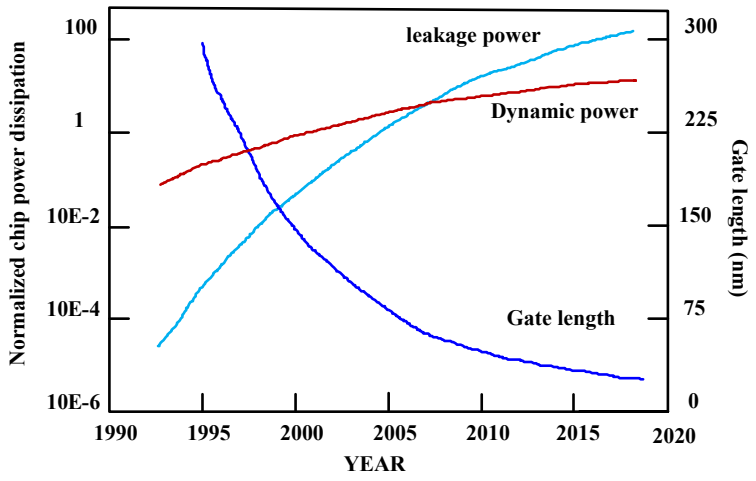
Keywords

Body Biasing, Gate Leakage, Junction Leakage, Power Gating, Multi-Threshold, SRAM Cell, Sub-Threshold Leakage

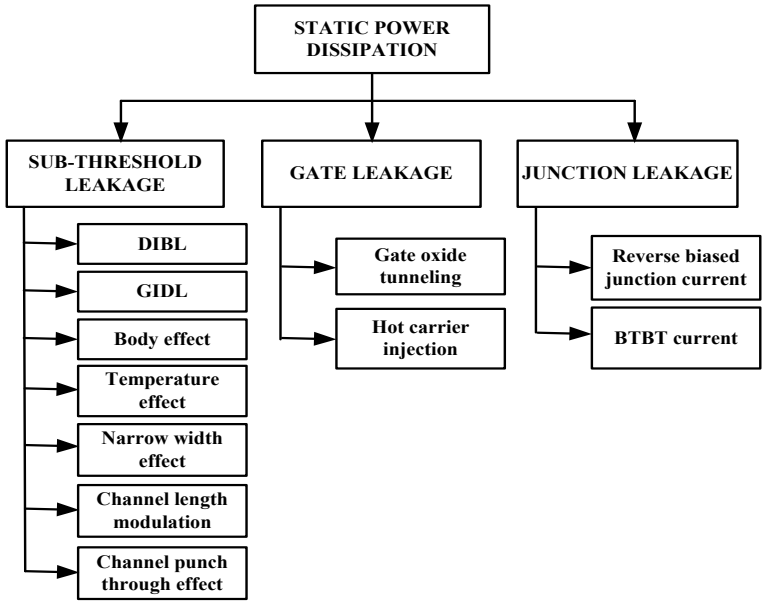
1. Introduction

To accomplish high-density chip, ultra-low power dissipation, and high performance, complementary metal oxide semiconductor (CMOS) devices have been scaled since last 30 years. As a result, the propagation delay time has been reduced by 30% per technology leading to the microprocessor performance being doubled every two years. Scaled technology has reduced the supply voltage to obtain low power consumption [1] [2] [3] [4]. Additionally, a scaled technology also has reduced device parameters such as threshold voltage, channel length and gate oxide thickness. However, the scaled technology has two drawbacks.

First, a low-V_{TH} device has an exponential increase in sub-threshold leakage. Sub-threshold leakage rises by ten times for every 0.1-volt decrease of the threshold voltage [5] [6] [7]. The second problem is the reduction of worst-case performance due to threshold variation at lower supplies [8] [9] [10]. As technology scales down, leakage current in a sub-micron region becomes more significant and is comparable with the dynamic power dissipation. **Figure 1(a)** shows the full chip leakage power dissipation based on the international technology roadmap for semiconductor (ITRS) [11] [12]. Various components affecting the sub-threshold leakage, gate leakage, and junction leakage are depicted in **Figure 1(b)**. However, finding and modelling of the several leakage mechanisms are essential for evaluation and minimization of leakage current for low power application [13] [14].



(a)



(b)

Figure 1. (a) Full chip power dissipation based on ITRS. (b) Leakage currents components.

Generally, device non-conducting current (I_{OFF}) depends on the supply voltage, threshold voltage, length of the channel, surface/channel doping profile, drain/source junction depth and gate oxide thickness [15]. For long channel devices I_{OFF} mainly originates from the drain-source reverse bias junctions. Short-channel device needs low power supply in order to reduce power dissipation [16] [17]. Hence, the reduced threshold voltage causes exponential increase in I_{OFF} current due to the weak-inversion region [18] [19].

A conventional 6T SRAM cell consists of two inverters connected back to back and two access NMOS transistors as shown in **Figure 2(a)**. The SRAM cell leakage versus technology scaling is shown in **Figure 2(b)**. It shows that the

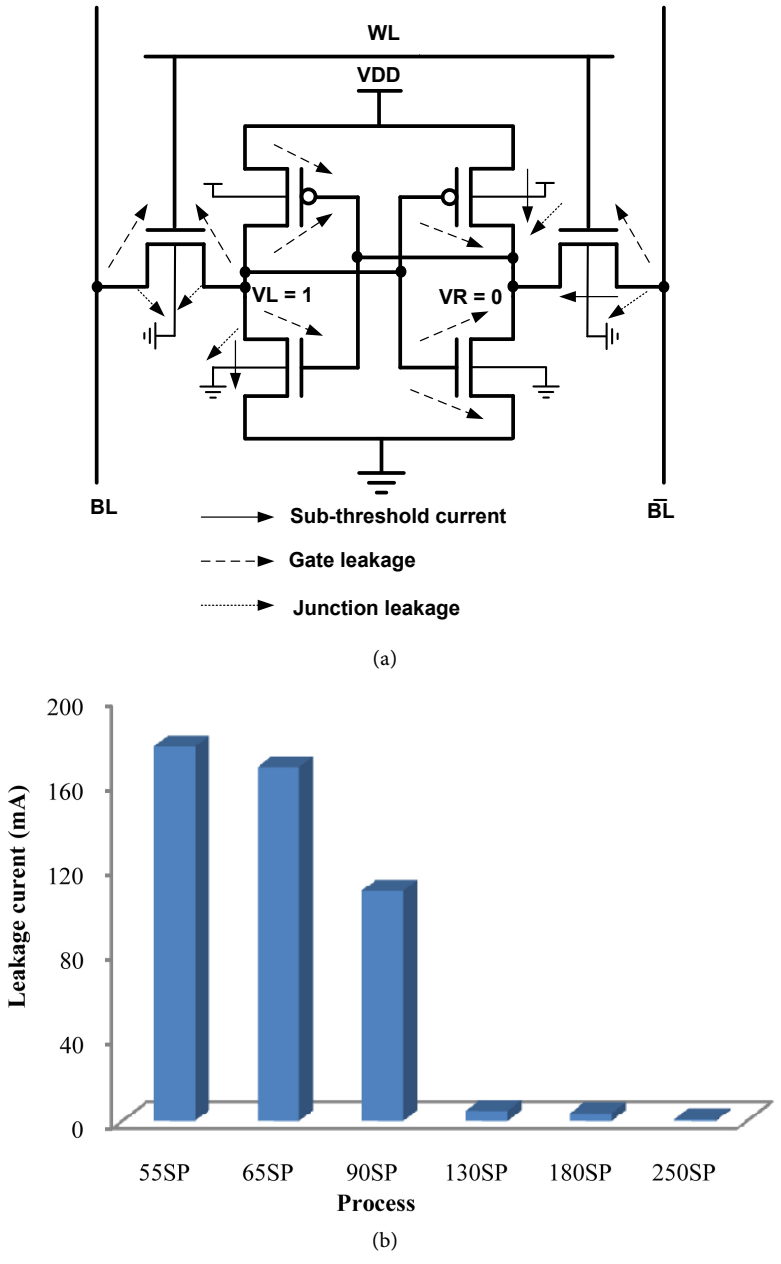


Figure 2. (a) Leakage phenomena in basic SRAM cell (b) SRAM Leakage current versus technology node [24].

leakage current exponential increased with technology scaling below 90 nm. Sub-threshold leakage arises whenever the transistor gate voltage is zero and the drain-source voltage is non-zero. Hence, leakage current can arise within the bit cell or on the bit line access paths [20] [21]. The transistor leakage in SRAM cell essentially depends on 1) the data value stored in the cell, 2) the logic data level of the word line and 3) the type of operation being performed. Bit line leakage current is a very small amount as compared to total cell leakage. However, the bit line leakage is a very important factor, as the bit line leakage can affect the constancy of the memory stored in the cell [22] [23]. The total leakage current is given by

$$\left(I_{\text{total-leak}} = I_{\text{sub\_th}} + I_{\text{gate}} + I_{\text{junction}}\right) \tag{1}$$

In order to bring the classification of leakage minimization approaches, we analyzed based on their fundamental design and mechanism. A brief summary of different leakage control schemes with their merits and demerits along with the limitations by using these schemes is presented. This paper will be helpful for researches to work towards emerging power-efficient memory designs for ultra-low power applications. The rest of the paper is organized as follows. Section 2 presents the origin of leakage current in a short-channel device. Various biasing techniques for leakage control SRAM are discussed in Section 3. Emerging power gating techniques for low power SRAM designs are presented in Section 4. Asymmetrical SRAM designs with multi-threshold transistor are described and comparisons of various low power techniques are tabulated in Section 5. Finally, the survey paper concludes in Section 6.

2. Leakage Currents

Basic leakage currents in a MOS transistor are as shown in **Figure 3**. Three types of leakage currents are presented when the device channel is in a non-conducting state, which are sub-threshold leakage current $\left(I_{\text{Sub\_th}}\right)$, gate-induced drain leakage $\left(I_{\text{GIDL}}\right)$ and punch-through leakage $\left(I_{\text{Punch}}\right)$ [25]. Two other leakage currents that are independent of the conduction of the device are gate tunneling current $\left(I_{\text{tunnel}}\right)$ and pn junction reverse bias leakage $\left(I_{\text{junction}}\right)$ due to a band to band tunneling effect [26] [27].

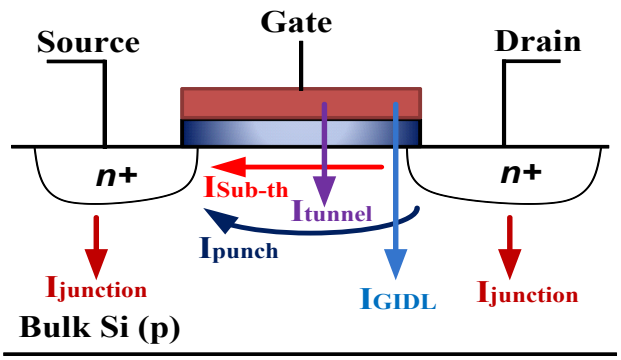


Figure 3. Leakage currents in a MOSFET.

2.1. Sub-Threshold or Weak Inversion Current

Sub-threshold or weak inversion current is present between the source and the drain terminals of the MOSFET transistor when the gate voltage is less than the threshold voltage of the device $\left(V_{GS} < V_{TH}\right)$. Weak inversion region has small minority carrier concentration and it varies along with the length of the channel. The drift current dominates in the strong inversion region and the diffusion current dominates in weak inversion region [28] [29] [30]. Let us assume that the source of the NMOS is zero $\left(V_G < V_{TH}\right)$ and the drain to source voltage is greater than 1 V. In this case, weak inversion current at V_{DS} falls completely due to the existence of reverse-biased subtract-drain pn junction [10] [31]. The NMOS transistor Gate-source voltage versus drain current has presented in Figure 4, which represents the sub-threshold and junction currents when the threshold voltage is 0.6 V. Drain current for NMOS transistor function in weak-in- version region is given by

$$I_{D(\text{weak inversion})} = I_{\text{on}} \cdot e^{(V_{GS}/V_T)} \tag{2}$$

where η is sub-threshold slope coefficient; V_T is the thermal voltage equal to q/KT; and I_{on} is $\mu_o C_{ox}\left(W/L\right)V_t^2 e^{1.8}$.

2.2. Gate-Induced Drain Leakage

Gate-induced drain leakage (GIDL) occurs due to band to band tunneling at gate-drain overlap region under the strong electric field. Electrical field increases with the decreasing the depletion layer at the surface. The GIDL is more in case of single-diffused drain as compared to double-diffused drain. At low subtract voltage the minority carrier accumulated into drain depletion region under the gate region that forms the path for the GIDL current [32] [33]. Further the GIDL current increases exponential with thinner gate oxide thickness, low-V_{TH} and the higher potential difference between gate and drain [34] [35]. A simple mathe- matical analysis is presented for the effect of gate work function in the electric

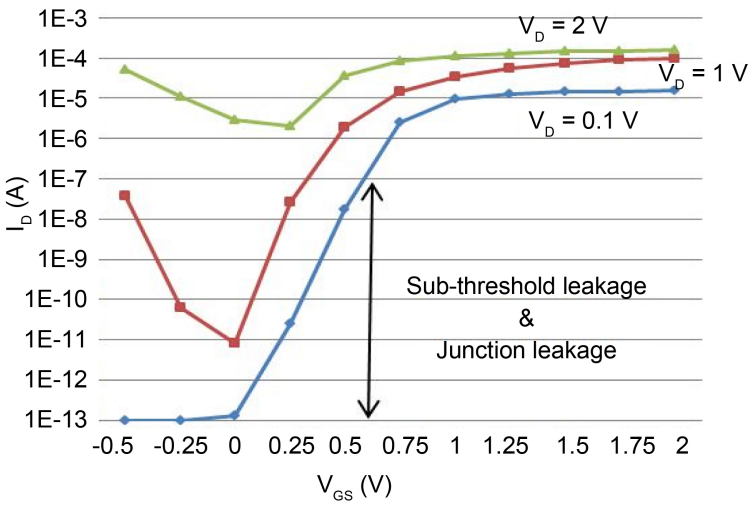


Figure 4. Gate-source voltage vs. drain current.

field at the gate-drain overlap in Equation (3).

$$E_{\text{Total}}^2 = \frac{\frac{V_{DG}}{T_{OX}}\left(1-\frac{V_{FB}-\psi_S}{V_{DG}}\right)^2 + \frac{V_{DG}^2}{\gamma h}}{T_{OX}} \tag{3}$$

Based on the tunneling theory, the I_{GIDL} current can be written as

$$I_{GIDL} = AE_{GIDL}^2 \exp\left(\frac{-B}{E_{GIDL}}\right) \tag{4}$$

where ψ_S is the potential drop across the silicon for BTBT; h is the parameter interrelated to junction depth, E_{GIDL} the electric field accountable for *GIDL* current; A and B are constants that aid in tunneling [36] [37].

2.3. Punch-Through Current

Punch-through current occurs in small-geometry MOS transistors due to the nearness of the source and drain depletion regions as there junctions spread into the short-channel (*i.e.*, when $x_{dS} + x_{dD} = L$). Since the short-channel doping concentration remains constant as a result the boundaries between the depletion regions are reduced [38] [39]. In submicron technology, the surface region was highly doped as compared to the substrate and the depletion region extended towards the substrate which rises the punch-through current below the surface [40] [41]. Punch-through current can be reduced with higher substrate doping, small oxides, modest junctions and preferably with long channels.

In short-channel devices, the potential barrier is governed by both the drain-to-source voltage V_{DS} and the gate-to-source voltage V_{GS}. When the drain voltage is increased, it decreases the potential barrier in the short channel, leading to drain-induced barrier lowering (DIBL). Carriers are injected into the channel surface from the source region independent of the gate voltage [42]. The drain and source junction widths are expressed as

$$x_{dD} = \sqrt{\left[\frac{2\varepsilon_{Si}}{qN_A}\right]\left(V_{DS} + \varnothing_{si} + V_{SB}\right)} \tag{5}$$

$$x_{ds} = \sqrt{\left[\frac{2\varepsilon_{Si}}{qN_A}\right]\left(\varnothing_{si} + V_{DB}\right)} \tag{6}$$

The sub-threshold surface diffusion current $\left(I_{\text{Sdif}}\right)$ for short channel at its saturation level $\left(\left|V_{ds}\right| > \frac{4kT}{q} \approx 0.1V\right)$ can be expressed as [43].

$$I_{\text{Sdif}} \propto Dn_i^2 e^{\left(q\Delta\varnothing_s/kT\right)} \Big/ L_{\text{eff}} \tag{7}$$

$$\Delta\varnothing_s = \Delta\varnothing_{so}\left(V_{gs}, V_{bs}\right) + m\left|V_{ds}\right| \tag{8}$$

where D is the surface diffusion constant of minority carriers; n_i is the intrinsic carrier concentration; $\Delta\varnothing_{so}$ is the surface-band-bending (a function of V_{gs}, V_{bs}) and m is a dimensionless constant.

Two other leakage currents that are independent of the conduction of the de-

vice are gate tunneling current and pn junction reverse bias leakage due to a band to band tunneling effect (I_{BTBT}) [26] [27].

2.4. Gate Tunneling Current

Gate tunneling current occurs due to the high electric field formed across the small gate oxide layer. Gate tunneling current depends on the device structure and biasing conditions. At high electric field, tunneling of electrons take place from gate to bulk and also from bulk to gate region through the gate oxide layer (*i.e* the quantum-mechanical wave function of a charged carrier [44]). Highly charged electrons can easily enter into or through the oxide layer due to small width of potential barrier. It increases the gate current [45] [46]. On the other hand, if the gate voltage is less than zero $(Vg < 0)$ the charged electrons in $n+$ poly-silicon can easily tunnel into or through the gate oxide and form a gate current. Gate tunneling current depends on the device structure and biasing conditions. Gate tunneling current in a scaled device contains a gate-to-channel current (I_{gc}) and edge direct tunneling currents (I_{gso}) and (I_{gdo}) [47] [48].

$$I_g = I_{gc} + I_{gso} + I_{gdo} \tag{9}$$

Gate tunneling current is divided into mainly two types, Flowler-Nord-heim (FN) tunneling and direct tunneling. In FN tunneling mechanism, electrons tunnel straight into the conduction band through the forbidden band gap of the oxide layer [49] [50]. The direct tunneling current form between the source-drain extension and the gate overlap. Direct tunneling occurs mainly due to the electrons and holes tunneling, the electron tunnel from the conduction band and the valence band while the holes tunnel from valence band. It is more sensitive to the gate oxide thickness [51]. The *FN* current expression represents the tunneling through the triangular potential barrier and is valid for $V_{ox} > \varnothing_{ox}$, where V_{ox} denotes the voltage drop across the oxide. The current density of *FN* tunneling is expressed as

$$J_{FN} = \frac{q^3 E_{ox}^2}{16\pi^2 h \varnothing_{ox}} \exp\left(-\frac{4\sqrt{2m}\varnothing_{ox}^{3/2}}{3hqE_{ox}}\right) \tag{10}$$

where E_{ox} is electric field across the gate oxide; $\varnothing_{ox}$ is the potential barrier height for electrons and m is the mass of an electron in the conduction band [52] [53].

2.5. Junction Leakage

Generally, body-to-drain and body-to-source junction are in reverse bias, which produces a pn junction reverse bias leakage current. In small-geometry devices, highly doped p and n regions cause a band-to-band tunneling (BTBT) leakage. The pn junction reverse bias leakage current primarily originates from minority carrier diffusion and drift current near the depletion region. Secondly, in reverse biased pn junction, the depletion region generates electron-hole pair. The reverse bias pn junction leakage current is mainly dependent on the doping concentration and depletion junction area [54] [55]. The BTBT current density is

given by

$$J_{B-B} = A\frac{EV_{\text{app}}}{E_g^{1/2}}\exp\left(-B\frac{E_g^{3/2}}{E}\right) \tag{11}$$

where m is the mass of an electron; E_g is the energy-band gap; V_{app} is the applied reverse bias; E is the electric field at the junction; q is the electronic charge; and h is $1/2\pi$ times Planck's constant.

3. Biasing Techniques

Generally the body terminal of the transistors is connected to the supply voltage (V_{DD} in the case of PMOS and GND in the case of NMOS) in order to control a threshold voltage. In the case of reverse body bias (RBB), the body voltage of PMOS is greater than the V_{DD} and the body voltage of NMOS is less than V_{GND}. This results in an increase in depletion layer width. The higher gate voltage is required to create an inversion layer by increasing the threshold voltage [56] [57] [58]. Similarly, in forward body bias (FBB) the body voltage of PMOS is less than the V_{DD} and the body voltage of NMOS is greater than V_{GND}. As a result, the depletion layer width is reduced. The smaller gate voltage creates the inversion layer thereby decreasing threshold voltage. Consequently FBB has fast transition [59] [60]. Analysis of NMOS body bias versus threshold voltage and leakage current is as shown in **Figure 5(a)** and **Figure 5(b)**. PMOS body bias versus threshold voltage and leakage current is as shown in **Figure 5(c)** and **Figure 5(d)**. These analysis shows that the FBB has lower-V_{TH}, it increase the leakage current exponential and RBB has higher-V_{TH}, it reduce the leakage current. Various biasing ideas to design high-V_{TH} PMOS and NMOS transistors given in **Table 1** and the arrows represent the sub-threshold current. In bulk MOSFETs, the threshold voltage (V_{TH}) is given by

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{\left|2\varnothing_b - V_{BS}\right|} - \sqrt{\left|2\varnothing_b\right|}\right) \tag{12}$$

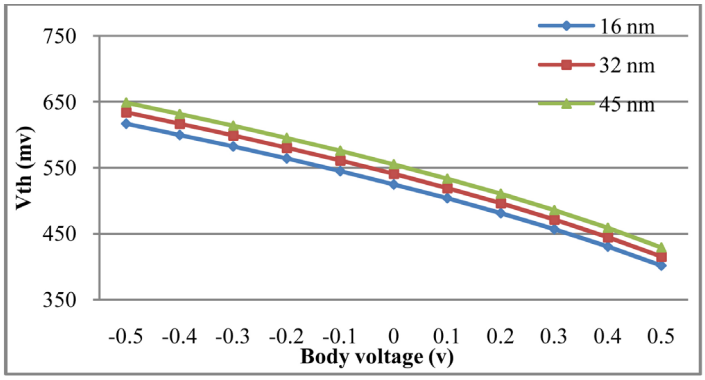
$$\gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2\varepsilon_{si}\cdot q\cdot N_A} \tag{13}$$

$$\varnothing_b = \frac{kT}{q}\ln\left(\frac{N_A}{N_i}\right) \tag{14}$$

where V_{TH0} is the threshold voltage of the device without body bias; γ is the coefficient of body effect; t_{ox} is the gate oxide thickness; ε_{ox} is the dielectric constant of the silicon dioxide; ε_{si} is the permittivity of silicon; $\varnothing_b$ is the device surface potential on strong inversion; N_A is the doping concentration density of the body; N_i is the carrier concentration in intrinsic silicon; k is Boltzmann's constant; q is the electric charge and T is the absolute temperature.

3.1. Reverse Body Bias (RBB)

Since the mid-1970s, RBB has been widely used in memory cells, in order to reduce the latch-up problem and memory data damage [62] [63]. RBB reduces the



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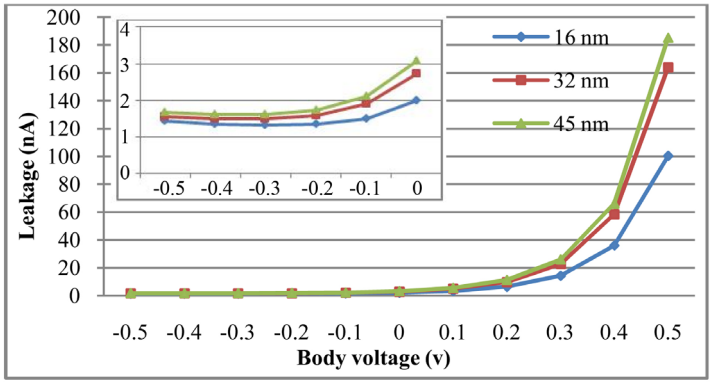

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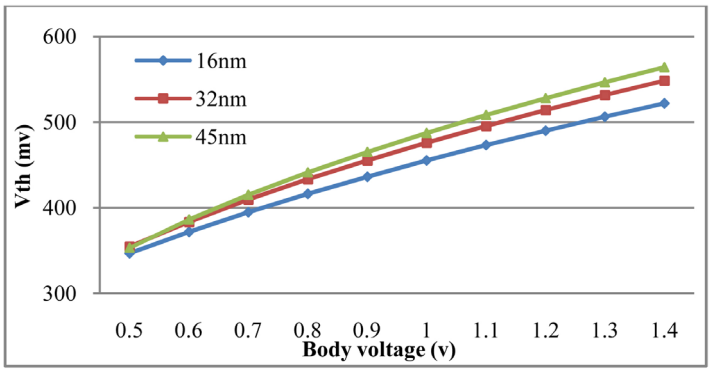

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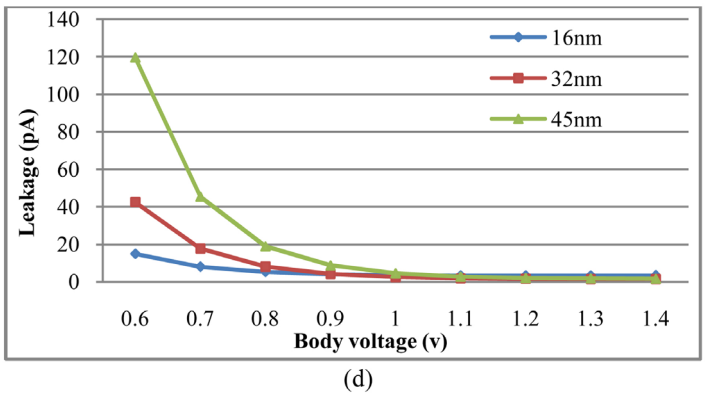
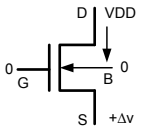
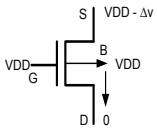
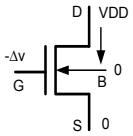
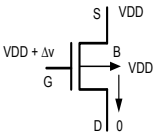
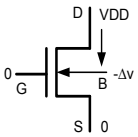
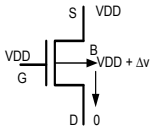
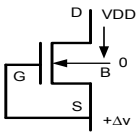
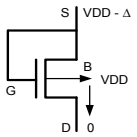
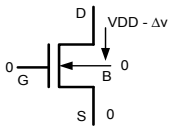
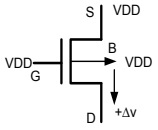


(d)

Figure 5. NMOS body voltage versus (a) Threshold voltage (b) Leakage current. PMOS body voltage versus (c) Threshold voltage (d) Leakage current.

Table 1. Biasing methods for high-V_{TH} PMOS and NMOS [61].

Control voltage (s)		NMOS	PMOS
V_{GS} reverse biasing	V_S: self-reverse biasing		
	V_G: offset gate driving		
V_{BS} reverse biasing	V_B: substrate driving		
	$V_S = V_G$ offset source driving		
V_{DS} reduction			

sub-threshold leakage while increasing the body voltage. Hence, an optimized RBB reduces the total leakage current. However, the junction leakage is influenced by substrate BTBT rather than the surface BTBT which is also called GIDL [64]. Novel techniques are required to reduce the substrate BTBT leakage in order to use the advantage of RBB. Furthermore, RBB is ineffective for leakage control in short channel devices and also for low-V_{TH} devices functions at high/room temperature [65] [66].

3.2. Forward Body Bias (FBB)

Reverse body bias has larger drain-substrate depletion layer to minimizes the short channel effects. However, threshold variation occurs across a die due to larger depletion layer. Moreover, the short channel devices have lower body coefficient (γ), and the channel potential is more affected by drain than by the body due to the DIBL. The short channel effect and DIBL are more sensitive to the low-V_{TH} transistors [67]. Hence the range of body biasing is motivated from RBB to FBB. FBB reduces the threshold voltage of high-V_{TH} devices and improves the circuit performance due to smaller switching capacitance. The FBB devices form larger junction capacitance due to reduced depletion width across the source and drain region [68] [69].

However, FBB increases the leakage current due to a source to a body junction is in forward bias. At lower-V_{TH}, the short circuit current is increase due to larger junction and gate capacitance. Hence, for optimized design operation at a maximum temperature of 110˚C, the desired forward body voltage is 450 mV, with a tolerance of ±50 mV [70].

3.3. Dual-V_{TH} Technology

Further improvements in short channel and DIBL can be achieved through dual-V_{TH} technology. A dual-V_{TH} device switches between low-V_{TH} and high-V_{TH}. The low-V_{TH} device can be formed by applying FBB and high-V_{TH} device with zero body steps. The complexity associated with a dual-V_{TH} process is reduced because it has a critical fabrication masking process. Need for additional device fabrication with various threshold voltages are eliminated [71].

3.4. VTCMOS Technique

In variable threshold CMOS (VTCMOS), a threshold voltage is controlled by the body biasing technique. Different threshold voltages can be achieved by using a self-body biasing transistor (SBT). In active mode, nearly zero body bias is used to achieve high speed. In standby mode, RBB is used to raise threshold voltage, thus minimizes the leakage current. Moreover, in active mode, a little FBB is applied to increase the performance speed while minimizing the short-channel effect. In VTCMOS, additional circuitry is required for body biasing which increases chip area [72] [73].

3.5. Clamping Diode

Lijun Zhang *et al.* proposed a source biasing technique to reduce leakage currents in SRAM cell, as shown in Figure 6. High threshold NMOS transistor M7

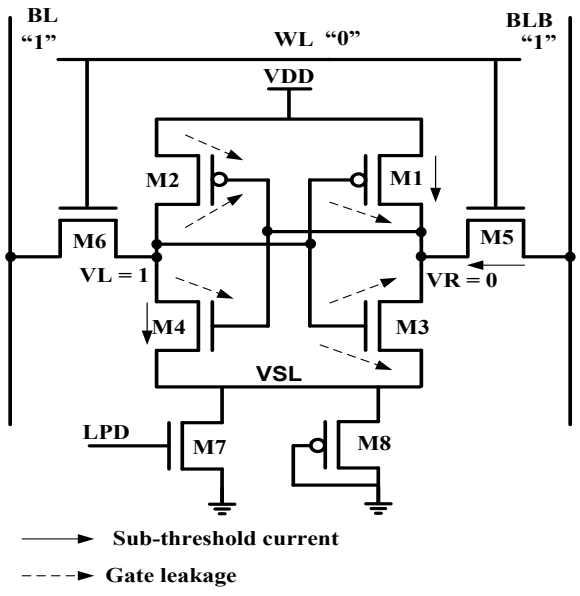


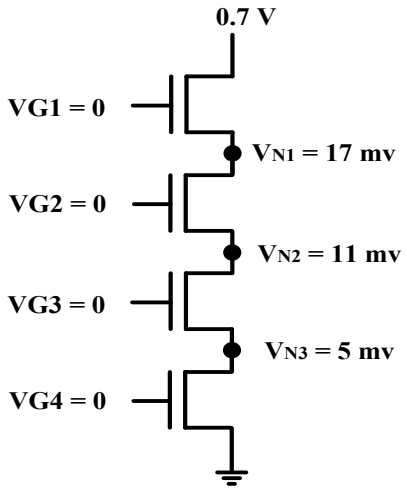
Figure 6. Clamping diode SRAM cell design.

is connected between SRAM source line (V_{SL}) and ground terminals. In active mode, M7 will turn on when gate voltage is high and its resistance is small, V_{SL} is equal to the ground and SRAM cell functions in the traditional manner. In standby mode, M7 is turned off, the source voltage V_{SL} increases which reduces the gate and sub-threshold leakage currents. The problem of floating voltage can be resolved by a clamping diode (PMOS transistor gate connected to its drain terminal) which is placed in parallel with the M7 [74].

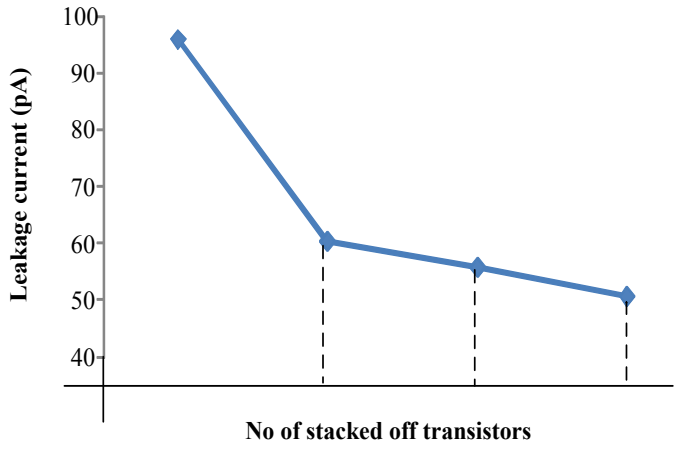
3.6. Stacking Technique

The NMOS stacking transistors are realized with 16 nm, node voltage and leakage current as shown in **Figure 7(a)** and **Figure 7(b)**. The stacking transistors provide the self-reverse biasing effect:

- Drain-to-source voltage decreases, leading to reduced DIBL current and the sub-threshold leakage current.
- Gate-to-source voltage is less than zero, thus decreasing sub-threshold current exponentially.



(a)



(a)

Figure 7. (a) Stacked transistor (b) leakage current curve.

- Substrate-to-source voltage is negative, thus increasing the threshold voltage due to body effect, resulting in a decrease in sub-threshold current.

N. K. Shukla *et al.* proposed a novel P4-SRAM cell consisting of a stacked transistor as shown in Figure 8. When the word line is low, the cell functions as conventional 6T SRAM cell. When the word line is high, transistor P3 andP4will turn off as a result, the self-reverse biasing (SRB) of series connected transistors will reduce the sub-threshold and gate leakage currents [75] [76].

4. Power Gating Techniques

Another efficient leakage reduction technique generally used in industry is power gating. In power gating scheme, the leakage currents are almost minimized by introducing the external header and footer transistors. These transistors eliminate the path exiting between V_{DD} to ground when the devices are in quiescent mode [77] [78].

4.1. Power Gating Scheme with a Sleep Transistor

To reduce the leakage mechanism in SRAM cell, M. Powell *et al.* proposed a power gating scheme with a sleep transistor connected in the ground path called Gated-V_{DD}, as shown in Figure 9. This design basic principle is to introduce an additional NMOS transistor in the leakage current path present in between the power supply to a ground [79] [80]. The additional transistor is fundamentally "gating" the cell's power supply by "switch on" in the active mode and "switch off" in an idle mode. Gated-V_{DD} scheme significantly reduces the leakage current by maintaining the performance compensation of low power supply and threshold voltage [81] [82].

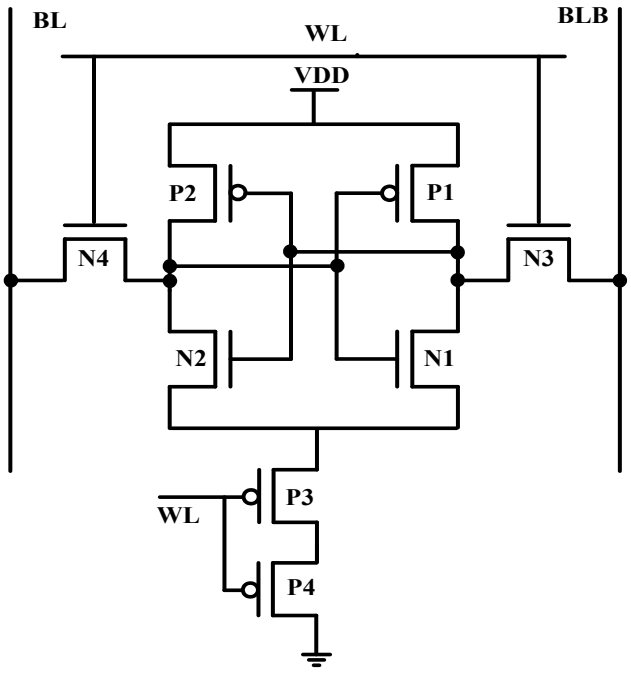


Figure 8. P4-SRAM cell design.

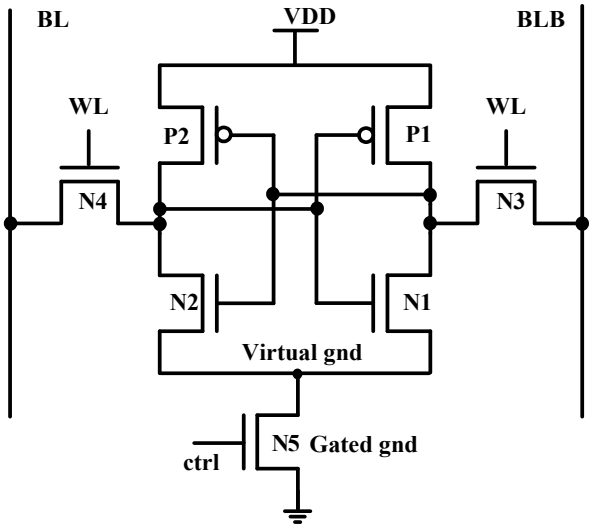


Figure 9. Gated-V_{DD} power gating scheme.

4.2. Data Retention Gated-Ground (DRG)

The drawback of the SRAM cell with power gating scheme is the determination of the stored data and the ground gated transistor increases the pull-down (PD) path resistance. To resolve this problem Amit Agarwal *et al.* proposed a data retention gated-ground (DRG) SRAM cell design to achieve low leakage power, as shown in **Figure 10**. The ground gated transistor is controlled by the external signal which is connected to the word-line. The leakage current significantly reduced through fundamentally "gating" the cell's power supply by "switch on" in the active mode and "switch off" in an idle mode [83].

4.3. *N*-Control SRAM Cell with Gated-V_{DD}

Praveen Elakkumanan *et al.* proposed an *N*-control SRAM cell with gated-V_{DD} and dual threshold voltage to achieve more reduction in leakage power dissipation, as shown in **Figure 11**. The SRAM cell is designed with low threshold transistor to attain high speed. Additional sleep transistors are designed with high-V_{TH} transistor to minimize leakage power, high-V_{TH} transistor are show with doted circles [84].

4.4. Diode-Connected PMOS Bias Transistor

Ankur Goel *et al.* proposed a power gating scheme along with post-silicon trim of the SRAM cell, as shown in **Figure 12(a)**. This technique provides many ways to trim the source voltage across SRAM cell ranging from 50 to 150 mV. Sector-based power gating has been presented which allows the leakage current reduction while SRAM is in active mode [85]. The PMOS transistor acts as a diode by connecting the source and gate terminal together. This process is termed as the self-biasing technique and it controls the virtual ground [86].

However, the self-biasing technique used in nanometre technology suffers from three problems. First, an additional self-biasing transistor (SBT) requires

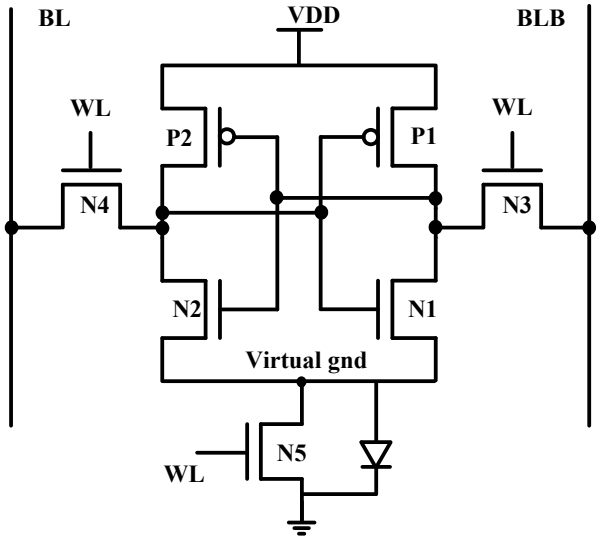


Figure 10. DRG SRAM cell design.

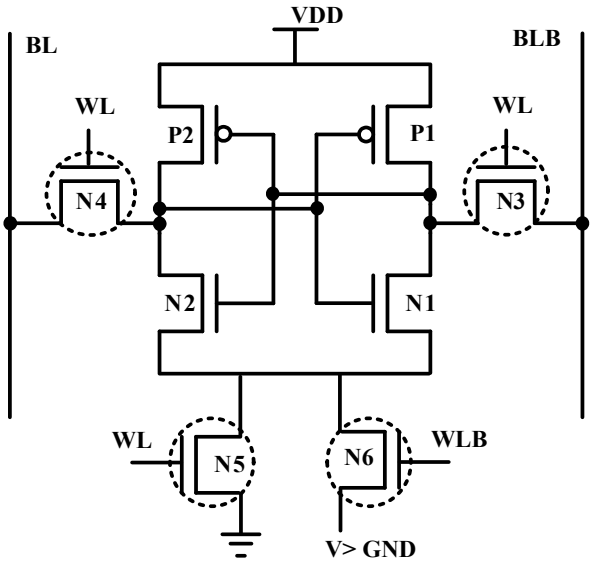


Figure 11. NC-SRAM cell design.

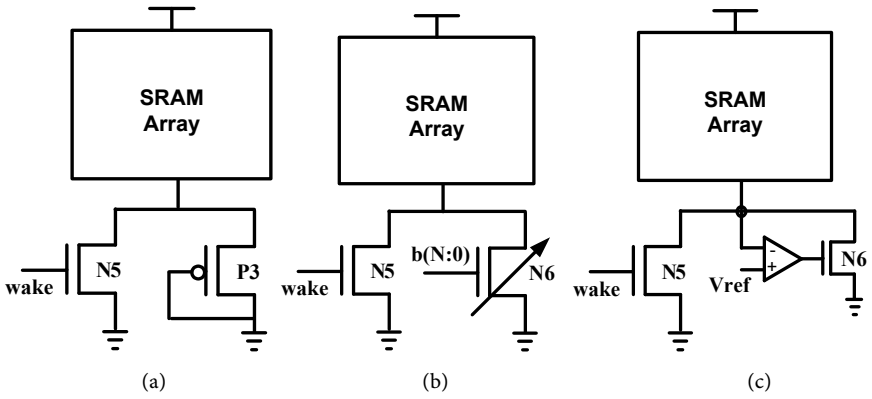


Figure 12. The SRAM cell with (a) diode-connected PMOS bias transistor (b) programmable bias transistor (c) active feedback with Op-Amp-based control.

extra area which is around 5%. Second, these schemes fail to carry out the correct mechanism for the modified source voltage. Third, increasing the virtual ground voltage has serious consequences such as negative bias temperature instability (NBTI)/positive bias temperature instability (PBTI) [87] [88] [89].

4.5. Programmable Bias Transistor

Kevin Zhang *et al.* proposed a programmable bias transistor (PBT) to control the SRAM virtual ground in standby mode, as shown in **Figure 12(b)**. PBT design is more effective in solving the post-silicon trimming issues and it has good control in a virtual ground. PBT provides two main advantages. First, the transistor biasing settings (virtual ground voltage) can be adjusted to achieve maximum leakage current reduction. Second, various biasing settings can be randomly chosen at various power supplies to provide an effective design under dissimilar voltage environments. However, they have some issues regarding the die-to-die (D2D), within die (WID) and induced temperature variations [90].

4.6. Active Feedback with Op-Amp-Based Control

To overcome the variations in a die, another efficient technique has been proposed with an active feedback op-amp, as shown in **Figure 12(c)**. A sleep transistor with active feedback op-amp bias reduces the standby power of the last level caches (LLCs) under all circumstances throughout the lifespan of the processor [91]. The main disadvantage of this technique is the DC power consumed by the op-amp that needs to be replicated along with each data. Further, this technique increases the SRAM cell area and it is noticeable in CMOS nanometre technology.

4.7. Diode and on Transistor Interchangeable Technique

Suhwan Kim *et al.* proposed a novel design which consists of "on transistor" and "power gating diode". This design is termed as "diode and on transistor interchangeable technique". This technique functions in two modes, light sleep mode and shutdown mode. In light sleep mode SRAM cell, data will be retained and voltage around SRAM memory must be greater than the minimum data retention voltage. It is also referred to as leakage saving mode which is shown in **Figure 13(a)**. In shutdown mode, SRAM memory data need not necessarily be recalled and the virtual ground level will be raised to attain enhanced leakage power saving. The shutdown mode design is as shown in **Figure 13(b)**, which has modified control logic transistor. The modified design can be operated in both light sleep and shutdown modes [92].

5. Multi-Threshold Design

Generally, SRAM cell contains six transistors with symmetrical configuration and normally they maintain same threshold voltage. MTCMOS is one of the prominent topologies to minimize the leakage power [93] [94]. By using an appropriate multi-threshold transistor result in a low leakage SRAM cell without

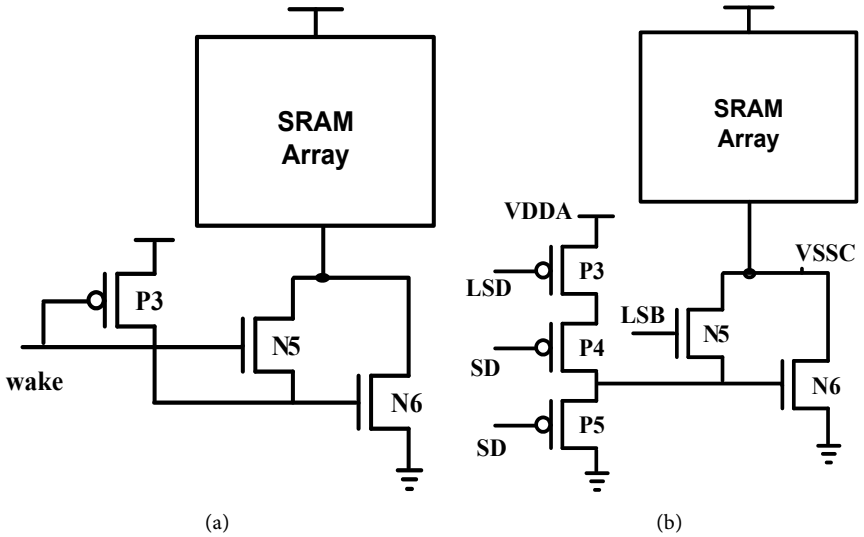


Figure 13. (a) Light sleep mode (b) Shutdown mode.

degrading the read/write performance. A suitable solution for having the low power SRAM cell with high performance and constancy is to implement asymmetrical designs [95] [96].

5.1. Asymmetrical Design

Asymmetrical cells can be designed in two different methods. The first approach is to have all original 6T-cell with different threshold voltages for selected transistors. The second approach is to add an extra transistor to the traditional 6T-cell. Asymmetrical SRAM cells designs are mainly based on the state of the cell, choose a state "0" or "1" and change the necessary transistor with high-V_{TH} transistors in order to minimize the leakage current. N. Azizi *et al.* proposed several designs of asymmetrical SRAM cells, with main focus on state "0", as it plays important role in storing the data. These architectures reduce the leakage current in the "0" state and probably they do not affect the "1" state.

5.2. Basic Asymmetric (BA)

The first design is named as Basic Asymmetric (BA) as shown in Figure 14(a). In this design N1, N4, and P2 transistors are replaced with high-V_{TH} transistors, which is shown in doted circles. This SRAM cell reduces leakage power by 70X when the cell stores "0" and maintains the same leakage in case "1" is stored. However, the read access time is reduced (the bit-line discharge time is increased w.r.t traditional cell) due to high-V_{TH} transistors (N1 and N4). P1 and P2 transistor do not affect the read access time since the bit lines are discharged through two NMOS transistors.

An asymmetrical SRAM cell transistor P1 is modified with high-V_{TH} as shown in Figure 14(b). This design reduces the leakage current by 1.6X when the cell stored data is "1" as compared to traditional design and the BA design. It reduces the leakage power reduction by 70X when the cell stores data "0". As another modification, transistor N2 is designed with high-V_{TH}, as shown in Figure 14(c).

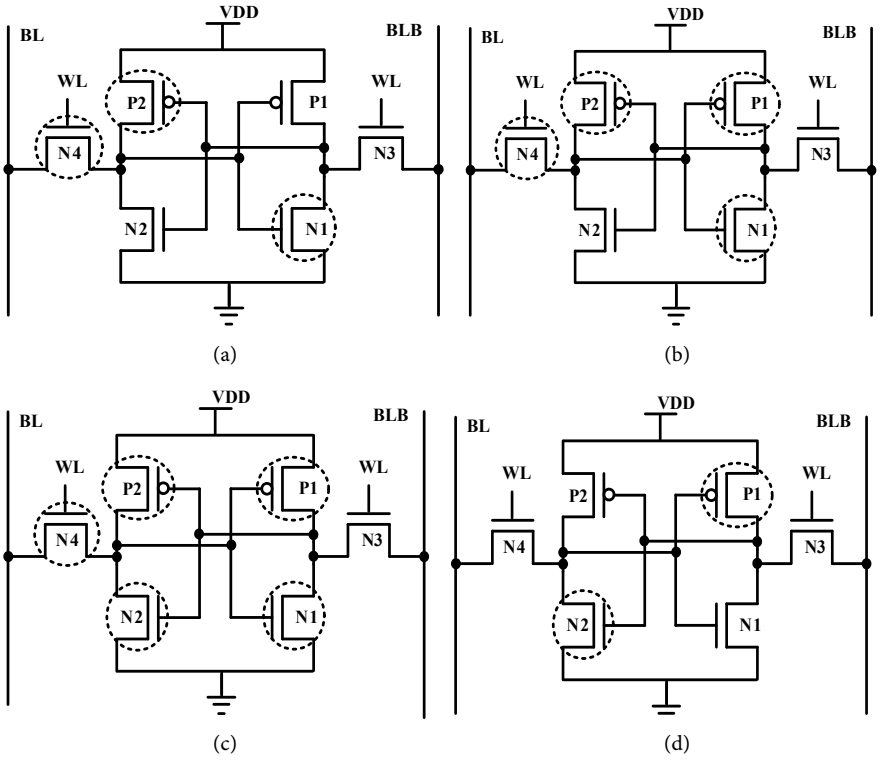


Figure 14. SRAM cell designs (a) Basic asymmetric (b) P1 is modified (c) Another modification (d) Special precharge.

Asymmetric cells have different discharge timings for bit-line and bit-line-bar. In this case, sense amplifier should match the read access time of slow side to the fast access side. This design further minimizes the leakage power by $7X$ when cell stored data "1". To reduce the read access time delay, an asymmetrical SRAM cell needs to be modified.

The special precharge SRAM cell is as shown in Figure 14(d), where only P1, N2 transistors are replaced with high-V_{TH} and the remaining with low-V_{TH} transistors. Initially bit-line is precharge to V_{DD} but in steady state bit-line needs to be kept at ground. This design attains leakage reduction $83X$ when the cell is stores data "0" and no reduction in leakage when cell stored data "1". The bit-line times decreased by $12X$ as compared to traditional cell [97] [98].

5.3. Effect of MTCMOS on RBL Sensing

A T Do *et al.* have proposed a decoupled 8T SRAM cell to achieve larger bit-line data sensing margin which is used in ultra-low power SRAM cells due to enhanced stability. The read word line performs the read operation by enabling N7 and the read bit lines are conditionally discharged according to the SRAM cell data. However, due to aggressive scaling of device parameters, the read bit-line leakage current increase which is almost comparable with the SRAM cell read current. The read bit-line data discharging depends on the cell read access current and read bit-line leakage current [99] [100]. In order to overcome these limitations, a leakage control bit-line scheme was proposed in read access path

with a high-V_{TH} and low-V_{TH} transistors which are shown in Figure 15. In the super-threshold region, high-V_{TH} transistors design achieves good *Ion* and *Ioff* current ratio. Low-V_{TH} transistor design had larger read bit-line swing along with smaller read bit-line data sensing margin due to sub-threshold leakage current [101] [102].

5.4. Bit Line Boosting Current Scheme

Bo Wang *et al.* proposed a 9T-MTCMOS SRAM cell, which consists of additional 3T read access bit-line, as shown in Figure 16(a). This design reduces the leakage current while increasing read bit-line sensing margin. A 9T SRAM cell consists of a basic 6T cell and the read access port contains 3T NMOS. All transistors in 6T-SRAM cell are designed with high-V_{TH}, which are shown in thick lines and the read access bit-line 3T NMOS are designed with low-V_{TH} to achieve very high performance through improved bit-line sensing margin. However, the cell bit line leakage is more than the cell read access current at higher temperatures [103] [104].

A. Teman *et al.* have proposed a 9T SRAM cell with a unique structure of supply feedback methodology for low voltage operation. In this 9T SRAM design, the supply voltage feedback transistor gate terminal is connected to the latch output to weaken the pull-up network of SRAM cell in a write operation, as shown in a Figure 16(b). The main advantage of this feedback is to maintaining

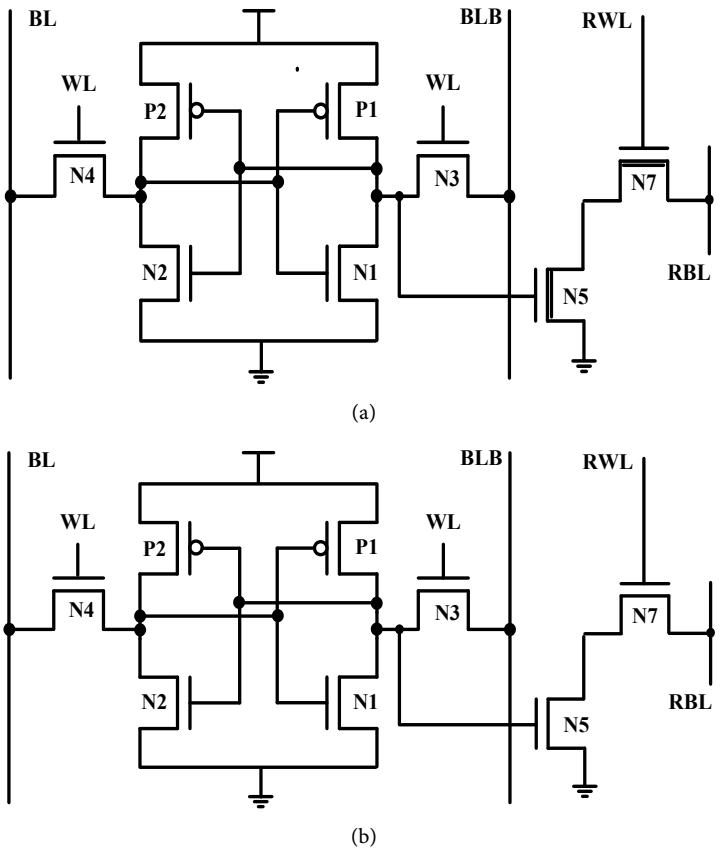


Figure 15. RBL sensing (a) high-V_{TH} (b) low-V_{TH}.

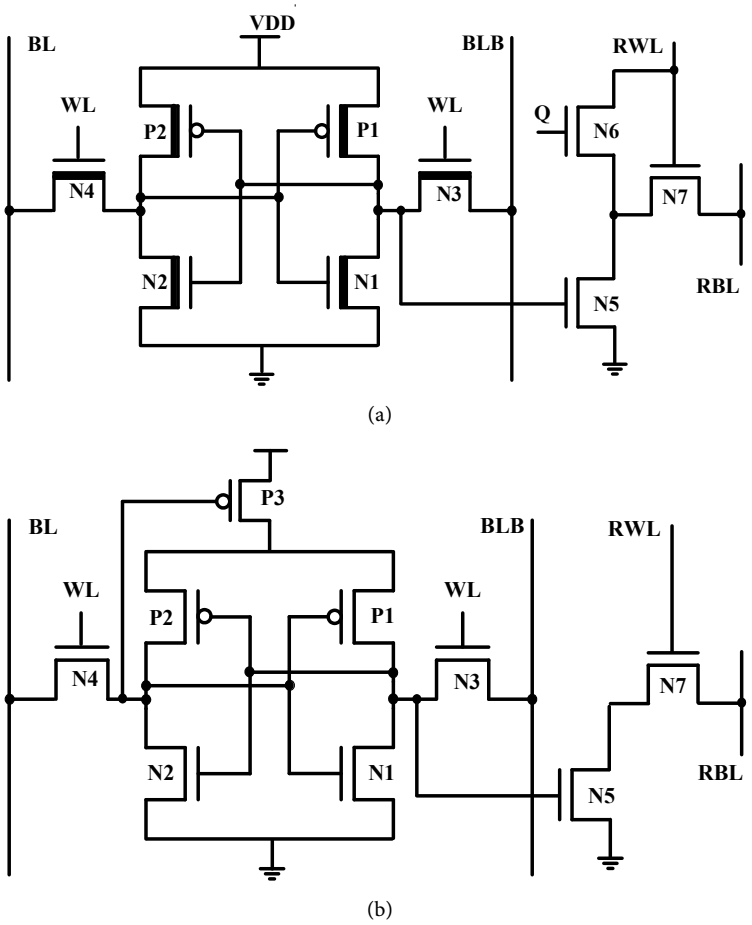


Figure 16. The SRAM cell (a) 9T MTCMOS design (b) 9F-Supply feedback design.

improved write margins and functionality, even though the PMOS transistors are stronger than the NMOS transistors [105] [106].

6. Conclusion

In this paper, the origin of leakage currents in a short-channel device has been discussed when a device is in conduction and non-conduction state. The various leakage control techniques proposed for low power SRAM cell architecture are presented. Classification of leakage minimization approaches analyzed based on their fundamental design and mechanism, such as biasing techniques, power gating techniques and multi-threshold techniques. The biasing techniques focus on changing the threshold voltage in order to control sub-threshold leakages. RBB design has reduced the leakage but it has consequences in terms of performance. Optimized FBB design can help to achieve high performance with low power dissipation. The key emphasis of power gating technique is on leakage path that exists in the circuit. Extra circuitry is added to create the virtual ground in leakage path to control the leakage currents. The multi-threshold design has the concept of asymmetrical design with a high-V_{TH} transistor in leakage path and a low-V_{TH} transistor for fast access. All these techniques have

Table 2. Comparison of various low power techniques.

Technique	*No. of MOS s*	*Merits*	*Demerits*	*Limitations*
		Biasing techniques		
Reverse body biasing [57] [58] [63] [65] [107] [108]	6T	$I_{\text{Sub-th}}$ ↓↓	I_{Junction}↑, Large transition delay	Sensitive to V_{TH} variation & GIDL
Forward body bias, [59] [60] [68] [69] [70]	6T	Small switching capacitance, speed ↑	Process complexity, Area overhead	Sensitive to SCE & DIBL
Source-biasing [61] [109] [110]	6T	$I_{\text{Sub-th}}$, I_{Gate} ↓↓	Delay penalty (τ_{PD} ↑)	Impact on soft error rate (SER)
Dual-V_{TH} [71]	6T	Improved short-channel, DIBL	Switching	Need of FBB
VTCMOS [72] [73]	6T	Low leakage, high speed	Additional circuitry need to control the threshold	Need to control the body bias
Clamping diode [74]	8T	$I_{\text{Sub-th}}$, I_{Gate} ↓	Delay penalty (τ_{PD} ↑)	Floating voltage at V_{SL}
Stacking body biasing (SRB) [75]	8T	$I_{\text{Sub-th}}$, I_{Gate} ↓	Delay increase, Area overhead	V_{TH}↑ due to body effect
		Power gating techniques		
Ground gated, sleep transistor [79] [80] [82]	8T	$I_{\text{Sub-th}}$, I_{Gate} ↓	virtual ground ↑↑, PD path resistance ↑	process-induced Vt variation, data retention problem
Data retention gated-ground [83]	7T	data retention, low leakage	Delay penalty	Need of External control signal
N-control with gated-V_{DD} [84]	8T	leakage power, high speed	Dual-threshold	Need to control virtual ground
Diode-connected [85] [88]	8T	$I_{\text{Sub-th}}$, I_{Gate} ↓	SNM ↓, sensitive to NBTI/PBTI	Data recalled, need of SBT
programmable bias transistor [90]	8T	Good control in virtual ground,	die-to-die, within die temperature variations	Need of PBT
Active feedback op-amp [91]	7T+ op-amp	Standby power ↓, die-to-die leakage ↓	DC power consumed by the op-amp, area	Need of op-amp
Light sleep mode [92]	9T	Low leakage power, data retained	performance degradation, area	Memory voltage > min. data retention voltage
Shutdown mode design [92]	11T	Low leakage power	Increased virtual ground, area	Need more no. of control inputs
		Multi-threshold design		
Basic Asymmetric [97] [98]	6T	reduces leakage power by 70x	bit-line discharge time ↑	Need of high-V_{TH}
High-V_{TH} on RBL Sensing [100]	8T	good I_{on} and I_{off} current ratios	Read access time ↑	Small prominent in near and sub-threshold region
Low-V_{TH}on RBL Sensing [100] [102]	8T	larger read bit-line swing	$I_{\text{sub-th}}$ ↑	smaller read bit-line data sensing margin
Bit-line boosting [103] [104]	9T	low leakage, read bit-line sensing margin ↑	Data dependent bit line- leakage ↑	Data effected due to Temperature variations
Supply Feedback approach [105] [106]	9T	Improved write margin & functionality	Performance degradation	Need to maintain a reasonable SNM.

the single objective of reducing the leakage in the nano-scale era. Most of these techniques focused on the sub-threshold leakage minimization. However, some of the techniques emphasize on retaining the data during the standby mode. A brief summary of different leakage control schemes with their merits and demerits along with the limitations by using these schemes is presented in Table 2. The low power SRAM cell designs presented in this paper will be helpful for researches to work towards emerging power-efficient memory designs for ultra-low power applications. We presented only three main techniques for a basic SRAM cell. Simulation analysis has been shown for basic leakage currents in a device; these are the limitations of this paper.

References

[1] Mead, C.A. (1994) Scaling of MOS Technology to Submicroometer Feature Sizes. *Analog Integrated Circuits and Signal Processing*, **6**, 9-25. https://doi.org/10.1007/BF01250732

[2] Taur, Y., Member, S., Buchanan, D.A., Chen, W.E.I., Frank, D.J., Ismail, K.E. and Wong, H. (1997) CMOS Scaling into the Nanometer Regime. *Proceedings of the IEEE*, **85**, 486-504. https://doi.org/10.1109/5.573737

[3] Breed, A.A. and Roenker, K.P. (2008) Comparison of the Scaling Characteristics of Nanoscale SOI N-Channel Multiple-Gate MOSFETs. *Analog Integrated Circuits and Signal Processing*, **56**, 135-141. https://doi.org/10.1007/s10470-007-9129-6

[4] Foty, D. (1999) Perspectives on Analytical Modeling of Small Geometry MOSFETs in SPICE for Low Voltage/Low Power CMOS Circuit Design. *Analog Integrated Circuits and Signal Processing*, **21**, 229-252. https://doi.org/10.1023/A:1008373903657

[5] Zou, L. and Larsen, T. (2012) Modeling of Substrate Leakage Currents in a High-Voltage CMOS Rectifier. *Analog Integrated Circuits and Signal Processing*, **71**, 231-236. https://doi.org/10.1007/s10470-011-9633-6

[6] Kaizerman, A., Fisher, S. and Fish, A. (2013) Subthreshold Dual Mode Logic. *IEEE Transactions on Very Large Scale Integration* (*VLSI*) *Systems*, **21**, 979-983. https://doi.org/10.1109/TVLSI.2012.2198678

[7] Bol, D., Ambroise, R., Flandre, D. and Legat, J.-D. (2009) Interests and Limitation of Technology Scaling for Subthreshold Logic. *IEEE Transactions on Very Large Scale Integration* (*VLSI*) *System,* **17**, 1508-1519. https://doi.org/10.1109/TVLSI.2008.2005413

[8] Sun, S.W. and Tsui, P.G.Y. (1995) Limitation of CMOS Supply-Voltage Scaling by MOSFET Threshold-Voltage Variation. *IEEE Journal of Solid-State Circuits*, **30**, 947-949. https://doi.org/10.1109/4.400439

[9] De, V. and Borkar, S. (1999) Technology and Design Challenges for Low Power and High Performance. *Proceeding of International Symposium on Low Power Electronics and Design*, San Diego, CA, 16-17 August 1999, 163-168. https://doi.org/10.1145/313817.313908

[10] Rao, R., Srivastava, A., Blaauw, D. and Sylvester, D. (2004) Statistical Analysis of Subthreshold Leakage Current for VLSI Circuits. *IEEE Transactions on Very Large Scale Integration* (*VLSI*) *Systems*, **12**, 131-139. https://doi.org/10.1109/TVLSI.2003.821549

[11] Ki, K. and Kim, K.Y. (2009) Statistical Timing and Leakage Power Analysis of PD-SOI Digital Circuits. *Analog Integrated Circuits and Signal Processing*, **60**, 127-136.

https://doi.org/10.1007/s10470-008-9220-7

[12] Xue, J., Li, T., Deng, Y. and Yu, Z. (2010) Full-Chip Leakage Analysis for 65 nm CMOS Technology and Beyond. *Integration, the VLSI Journal*, **43**, 353-364. https://doi.org/10.1016/j.vlsi.2010.05.002

[13] Keshavarzi, A., Roy, K., Member, S. and Hawkins, C.F. (2000) Intrinsic Leakage in Deep Submicron CMOS ICs—Measurement-Based Test Solutions. *IEEE Transactions on Very Large Scale Integration* (*VLSI*) *Systems*, **8**, 717-723. https://doi.org/10.1109/92.902266

[14] Lorenzo, R. and Chaudhury, S. (2016) Review of Circuit Level Leakage Minimization Techniques in CMOS VLSI Circuits. *IETE Technical Review*, **33**, 1-23. https://doi.org/10.1080/02564602.2016.1162116

[15] Henson, W.K., Yang, N., Kubicek, S., Vogel, E.M., Wortman, J.J., Member, S., *et al.* (2000) Analysis of Leakage Currents and Impact on Off-State Power Consumption for CMOS Technology in the 100-nm Regime. *IEEE Transactions on Electron Devices*, **47**, 1393-1400. https://doi.org/10.1109/16.848282

[16] Bikki, P. and Karuppanan, P. (2016) Analysis of Low Power and Small Swing Self-Biasing CMOS Design. *Fareast Journal of Electronics and Communication*, **3**, 245-261. https://doi.org/10.17654/ECSV3PI16245

[17] Fjeldly, T.A., Member, S. and Shur, M. (1993) Threshold Voltage Modeling and the Subthreshold Regime of Operation of Short-Channel. *IEEE Transactions on Electron Devices*, **40**, 137-145. https://doi.org/10.1109/16.249436

[18] Tsang, T.K., El-gamal, N.M., Iniewski, K., Townsend, K.A., Haslett, J.W. and Wang, Y. (2007) Current Status of CMOS Low Voltage and Low Power Wireless IC Designs. *Analog Integrated Circuits and Signal Processing*, **53**, 9-18. https://doi.org/10.1007/s10470-006-9019-3

[19] Serra-Graells, F. and Huertas, J.L. (2003) 1 V CMOS Subthreshold Log Domain PDM. *Analog Integrated Circuits and Signal Processing*, **34**, 183-187. https://doi.org/10.1023/A:1022545414777

[20] Singh, S.K. and Kaushik, B.K. (2013) A Novel Approach to Reduce Leakage Current in ULP SRAM. *IETE Technical Review*, **59**, 704-708. https://doi.org/10.4103/0377-2063.126968

[21] Prasad, G. and Anand, A. (2015) Statistical Analysis of Low-Power SRAM Cell Structure. *Analog Integrated Circuits and Signal Processing*, **82**, 349-358. https://doi.org/10.1007/s10470-014-0463-1

[22] Jovanovic, B., Brum, R.M. and Torres, L. (2014) Evaluation of Hybrid MRAM/CMOS Cells for "Normally-Off and Instant-On" Computing. *Analog Integrated Circuits and Signal Processing*, **81**, 607-621. https://doi.org/10.1007/s10470-014-0427-5

[23] Lo, C.H. and Huang, S.Y. (2011) P-P-N Based 10T SRAM Cell for Low-Leakage and Resilient Subthreshold Operation. *IEEE Journal of Solid-State Circuits*, **46**, 695-704. https://doi.org/10.1109/JSSC.2010.2102571

[24] Zhang, L.-J., Wu, C., Ma, Y.-Q., Zheng, J.-B. and Mao, L.-F. (2011) Leakage Power Reduction Techniques of 55 nm SRAM Cells. *IETE Technical Review*, **28**, 135-145. https://doi.org/10.4103/0256-4602.78105

[25] Roy, K., Mukhopadhyay, S. and Mahmoodi-Meimand, H. (2003) Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits. *Proceedings of the IEEE*, **91**, 305-327. https://doi.org/10.1109/JPROC.2002.808156

[26] Calimera, A., MacIi, A., MacIi, E. and Poncino, M. (2012) Design Techniques and

Architectures for Low-Leakage SRAMs. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **59**, 1992-2007. https://doi.org/10.1109/TCSI.2012.2185303

[27] Tanizawa, M., Ikeda, M., Kotani, N., Tsukamoto, K. and Horie, K. (1993) A Complete Substrate Current Model Including Band-to-Band Tunneling Current for Circuit Simulation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **12**, 1749-1757. https://doi.org/10.1109/43.248086

[28] Antognetti, P., Caviglia, D.D. and Profumo, E. (1982) CAD Model for Threshold and Subthreshold Conduction in MOSFET's. *IEEE Journal of Solid-State Circuits*, **17**, 454-458. https://doi.org/10.1109/JSSC.1982.1051759

[29] Narendra, S., De, V., Borkar, S., Antoniadis, D. and Chandrakasan, A. (2002) Full-Chip Sub-Threshold Leakage Power Prediction Model for Sub-0.18 um CMOS. *International Symposium on Low Power Electronincs and Design*, Monterey, CA, 12-14 August 2002, 19-23. https://doi.org/10.1145/566408.566415

[30] Pavasovic, A., Andreou, A.G. and Westgate, C.R. (1994) Characterization of Subthreshold MOS Mismatch in Transistors for VLSI Systems. *Analog Integrated Circuits and Signal Processing*, **6**, 75-85. https://doi.org/10.1007/BF01250737

[31] Chang, I.J., Park, S.P. and Roy, K. (2010) Exploring Asynchronous Design Techniques for Process-Tolerant and Energy-Efficient Subthreshold Operation. *IEEE Journal of Solid-State Circuits*, **45**, 401-410. https://doi.org/10.1109/JSSC.2009.2036764

[32] Guo, J., Liu, Y., Chou, M.H., Wang, M.T. and Shone, F. (1998) A Three-Terminal Band-Trap-Band Tunneling Model for Drain Engineering and Substrate Bias Effect on GIDL in MOSFET. *IEEE Transactions on Electron Devices*, **45**, 1518-1523. https://doi.org/10.1109/16.701483

[33] Ghodsi, R., Sharifzadeh, S. and Majjiga, J. (1998) Gate-Induced Drain-Leakage in Buried-Channel PMOS: A Limiting Factor in Development. *IEEE Electron Device Letters*, **19**, 354-356. https://doi.org/10.1109/55.709642

[34] Xu, Y., Chi, B. and Wang, Z. (2013) Gate-Leakage Compensation Scheme for Programmable SI-DAC of Modulator in Deep Sub-Micron. *Analog Integrated Circuits and Signal Processing*, **76**, 155-160. https://doi.org/10.1007/s10470-013-0073-3

[35] Rosar, M., Leroy, B. and Schweeger, G. (2000) A New Model for the Description of Gate Voltage and Temperature Dependence of Gate Induced Drain Leakage (GIDL) in the Low Electric Field Region. *IEEE Transactions on Electron Devices*, **47**, 154-159. https://doi.org/10.1109/16.817581

[36] Yuan, X., Park, J.E., Wang, J., Zhao, E., Ahlgren, D.C., Hook, T., *et al.* (2008) Gate-Induced-Drain-Leakage Current in 45-nm CMOS Technology. *IEEE Transactions on Device and Materials Reliability*, **8**, 501-508. https://doi.org/10.1109/TDMR.2008.2002350

[37] Ana, F. and Najeeb-Ud-Din (2012) Suppression of Gate Induced Drain Leakage Current (GIDL) by Gate Work Function Engineering: Analysis and Model. *Journal of Electronic Devices*, **13**, 984-996.

[38] Gupta, A.D.A.S. and Lahiri, S.K. (1990) An Aanalytical Model of Punchthrough Voltage of Short Channel MOSFETS with Nonuniformly Doped Channels. *Solid-State Electronics*, **33**, 395-400. https://doi.org/10.1016/0038-1101(90)90041-C

[39] Keshavarzi, A., Roy, K., Lafayette, W. and Hawkins, C.F. (1997) Intrinsic Leakage in Low Power Deep Submicron CMOS ICs. *International Test Conference*, 6 November 1997, 146-155. https://doi.org/10.1109/test.1997.639607

[40] Fu, K.Y. and Tsang, Y.L. (1997) On the Punchthrough Phenomenon in Submicron MOS Transistors. *IEEE Transactions on Electron Devices*, **44**, 847-855.

https://doi.org/10.1109/16.568048

[41] Fu, K.-Y. and Tsang, Y.L. (1997) Punchthrough Currents in Sub-Micron Short Channel MOS Transistors. *Solid-State Electronics*, **41**, 435-439. https://doi.org/10.1016/S0038-1101(96)00103-7

[42] Dennard, R., Gaensslen, F., Yu, W.-N., Rideout, L., Bassous, E. and Le Blanc, A. (1974) Design of Ion-Implanted Small MOSFET'S Dimensions with Very Small Physical Dimensions. *IEEE Journal of Solid State Circuits*, **9**, 257-268. https://doi.org/10.1109/JSSC.1974.1050511

[43] Barron, M.B. (1972) Low Level Currents in Insulated Gate Field Effect Transistors. *Solid-State Electronics*, **15**, 293-302. https://doi.org/10.1016/0038-1101(72)90084-6

[44] Srikantaiah, J. and DasGupta, A. (2012) Quantum Mechanical Effects in Bulk MOSFETs from a Compact Modeling Perspective: A Review. *IETE Technical Review*, **29**, 3-28. https://doi.org/10.4103/0256-4602.93119

[45] Chen, M., Huang, H., Hou, C. and Yang, K. (1998) Back-Gate Bias Enhanced Band-to-Band. *IEEE Electron Device Letters*, **19**, 134-136. https://doi.org/10.1109/55.663538

[46] Yang, N., Henson, W.K., Wortman, J.J. and Member, S. (2000) A Comparative Study of Gate Direct Tunneling and Drain Leakage Currents in N-MOSFET's with Sub-2-nm Gate Oxides. *IEEE Transactions on Electron Devices*, **47**, 1636-1644. https://doi.org/10.1109/16.853042

[47] Majkusiak, B. and Badri, M.H. (2000) Semiconductor Thickness and Back-Gate Voltage Effects on the Gate Tunnel Current in the MOS/SOI System with an Ultrathin Oxide. *IEEE Transactions on Electron Devices*, **47**, 2347-2351. https://doi.org/10.1109/16.887019

[48] Stadele, M., Tuttle, B.R. and Hess, K. (2009) Tunneling through Ultrathin SiO_2 Gate Oxides from Microscopic Models. *Journal of Applied Physics*, **89**, 348-363. https://doi.org/10.1063/1.1330764

[49] Larcher, L., Member, S., Paccagnella, A. and Ghidini, G. (2001) Gate Current in Ultrathin MOS Capacitors : A New Model of Tunnel Current. *IEEE Transactions on Electron Devices*, **48**, 271-278. https://doi.org/10.1109/16.902726

[50] Yang, K.N., Huang, H.T., Member, S., Chen, M.J., Member, S., Lin, Y.M. and Liang, M.S. (2001) Characterization and Modeling of Edge Direct Tunneling (EDT) Leakage in Ultrathin Gate Oxide MOSFETs. *IEEE Transactions on Electron Devices*, **48**, 1159-1164. https://doi.org/10.1109/16.925242

[51] Saheb, Z. and El-Masry, E.I. (2015) Modelling of Direct Tunneling Gate Leakage Current of Floating-Gate CMOS Transistor in sub 100 nm Technologies. *Analog Integrated Circuits and Signal Processing*, **84**, 67-73. https://doi.org/10.1007/s10470-015-0553-8

[52] Bowman, K.A., Member, S., Wang, L., Member, S., Tang, X., Meindl, J.D. and Fellow, L. (2001) A Circuit-Level Perspective of the Optimum Gate Oxide Thickness. *IEEE Transactions on Electron Devices*, **48**, 1800-1810. https://doi.org/10.1109/16.936710

[53] Choi, C., Member, S., Nam, K., Member, S., Yu, Z. and Member, S. (2001) Impact of Gate Direct Tunneling Current on Circuit Performance : A Simulation Study. *IEEE Transactions on Electron Devices*, **48**, 2823-2829. https://doi.org/10.1109/16.974710

[54] Murakami, Y. and Shingyouji, T. (1994) Separation and Analysis of Diffusion and Generation Components of pn Junction Leakage Current in Various Silicon Wafers. *Journal of Applied Physics*, **75**, 3548-3552. https://doi.org/10.1063/1.356091

[55] Lee, H. and Hwang, J. (1998) Accurate Extraction of Reverse Leakage Current

Components of Shallow Silicided p/sup +/-n Junction for Quarter- and Sub-Quarter-Micron MOSFET's. *IEEE Transactions on Electron Devices*, **45**, 1848-1850. https://doi.org/10.1109/16.704389

[56] Karuppanan, P., Ghosh, S., Khan, K. and Bikki, P. (2017) A Fully Differential Operational Amplifier with Slew Rate Enhancer and Adaptive Bias for Ultra Low Power. *Journal of Low Power Electronics*, **13**, 67-75.

[57] Enomoto, T., Oka, Y., Shikano, H., Harada, T. and Science, F. (2002) A Self-Controllable-Voltage-Level (SVL) Circuit for Low-Power, High-Speed CMOS Circuits.

[58] Enomoto, T., Oka, Y. and Shikano, H. (2003) A Self-Controllable Voltage Level (SVL) Circuit and Its Low-Power High-Speed CMOS Circuit Applications. *IEEE Journal of Solid-State Circuits*, **38**, 1220-1226. https://doi.org/10.1109/JSSC.2003.813248

[59] Deshmukh, J. and Khare, K. (2012) Dynamic SVL and Body Bias for Low Leakage Power and High Performance in CMOS Digital Circuits. *International Journal of Electronics*, **99**, 1717-1728. https://doi.org/10.1080/00207217.2012.692634

[60] Narendra, S., Keshavarzi, A., Bloechel, B.A., Borkar, S. and De, V. (2003) Forward Body Bias for Microprocessors in 130-nm Technology Generation and beyond. *IEEE Journal of Solid-State Circuits*, **38**, 696-701. https://doi.org/10.1109/JSSC.2003.810054

[61] Nakagome, Y., Horiguchi, M., Kawahara, T. and Itoh, K. (2003) Review and Future Prospects of Low-Voltage RAM Circuits. *IBM Journal of Research and Development*, **47**, 525-552. https://doi.org/10.1147/rd.475.0525

[62] Tsuguo, K. and Sakurai, T. (1994) Self-Adjusting Threshold-Voltage Scheme (SATS) for Low Voltage High Speed Operation. *Custom Integrated Circuit Conference*, San Diego, 1-4 May 1994, 271-274.

[63] Kawahara, T., Horiguchi, M., Kawajiri, Y., Kitsukawa, G., Kure, T. and Aoki, M. (1993) Subthreshold Current Reduction for Decoded-Driver by Self-Reverse Biasing. *IEEE Journal of Solid-State Circuits*, **28**, 1136-1144. https://doi.org/10.1109/4.245594

[64] Horiguchi, M., Sakata, T. and Itoh, K. (1993) Switched-Source-Impedance CMOS Circuit for Low Standby Subthreshold Current Giga-Scale LSI's. *IEEE Journal of Solid-State Circuits*, **28**, 1131-1135. https://doi.org/10.1109/4.245593

[65] Bikki, P. and Karuppanan, P. (2017) Analysis of Low Power Feedthrough Logic with Leakage Control Technique. Accepted at the 4th International IEEE Conference (ICPCES-2017), MNNIT-Allahabad.

[66] Keshavarzi, A., Narendra, S., Borkar, S., Hawkind, C., Roy, K. and De, V. (1999) Technology Scaling Behavior of Optimum Reverse Body Bias for Standby Leakage Power Reduction in CMOS IC's. *International Symposium on Low Power Electronics and Design*, San Diego, 16-17 August 1999, 252-254. https://doi.org/10.1145/313817.313937

[67] Islam, A. and Hasan, M. (2012) Variability Aware Low Leakage Reliable SRAM Cell Design Technique. *Microelectronics Reliability*, **52**, 1247-1252. https://doi.org/10.1016/j.microrel.2012.01.003

[68] Shimazaki, Y., Zlatanovici, R. and Nikoli, B. (2003) A 9uW 50 MHz 32b Adder Using a Self-Adjested Forward Bosy Bias in SOCs. *IEEE International ASIC/SOC Conference*, Rochester, 25-28 September 2002, 418-419.

[69] Kim, C.H.I., Kim, J.J., Mukhopadhyay, S. and Roy, K. (2005) A Forward Body-Biased Low-Leakage SRAM Cache: Device, Circuit and Architecture Considerations.

IEEE Transactions on Very Large Scale Integration Systems, **13**, 349-357. https://doi.org/10.1109/TVLSI.2004.842903

[70] Kim, C.H., Kim, J.-J., Mukhopadhyay, S. and Roy, K. (2003) A Forward Body-Biased-Low-Leakage SRAM Cache: Device and Architecture Considerations. *Proceedings of the International Symposium on Low Power Electronics and Design*, Seoul, 25-27 August 2003, 6-9. https://doi.org/10.1145/871506.871511

[71] Keshavarzi, A., Ma, S., Narendra, S., Bloechel, B., Mistry, K., Ghani, T. and De, V. (2001) Effectiveness of Reverse Body Bias for Leakage Control in Scaled Dual Vt CMOS ICs. *Proceedings of the International Symposium on Low Power Electronics and Design*, California, 6-7 August 2001, 207-212. https://doi.org/10.1145/383082.383135

[72] Kuroda, T. and Sakurai, T. (1996) A 0.9-V, 150-MHz, 10-mW, 4 mm2, 2-D Discrete Cosine Transform Core Processor with Variable Threshold-Voltage (VT) Scheme. *IEEE Journal of Solid-State Circuits*, **31**, 191-201. https://doi.org/10.1109/JSSC.1996.542322

[73] Mizuno, H., Ishibashi, K. and Shimura, T. (1999) An 18-uA Standby Current 1.8-V, 200-MHz Microprocessor with Self-Substrate-Biased Data-Retention Mode. *IEEE Journal of Solid-State Circuits*, **34**, 1492-1500. https://doi.org/10.1109/4.799853

[74] Zhang, L., Wu, C., Mao, L.-F. and Zheng, J. (2012) Integrated SRAM Compiler with Clamping Diode to Reduce Leakage and Dynamic Power in Nano-CMOS Process. *Micro & Nano Letters*, **7**, 171-173. https://doi.org/10.1049/mnl.2011.0680

[75] Shukla, N.K. and Pattanaik, M. (2011) Design and Analysis of a Novel Low-Power SRAM Bit-Cell Structure at Deep-Sub-Micron CMOS Technology for Mobile Multimedia Applications. *International Journal of Advanced Computer Science and Applications*, **2**, 43-49.

[76] Neema, V., Chouhan, S.S. and Tokekar, S. (2013) Novel Circuit Technique for Reduction of Leakage Current in Series/Parallel PMOS/NMOS Transistor Stack. *IETE Journal of Research*, **56**, 6-10.

[77] Xu, H., Vemuri, R. and Jone, W.-B. (2011) Dynamic Characteristics of Power Gating During Mode Transition. *IEEE Transactions on Very Large Scale Integration Systems*, **19**, 237-249. https://doi.org/10.1109/TVLSI.2009.2033699

[78] Kim, K.K., Kim, Y. and Choi, K. (2011) Hybrid CMOS and CNFET Power Gating in Ultralow Voltage Design. *IEEE Transactions on Nanotechnology*, **10**, 1439-1448. https://doi.org/10.1109/TNANO.2011.2168236

[79] Powell, M., Falsafi, B., Roy, K. and Vijaykumar, T.N. (2000) Gated-Vdd: A Circuit Technique to Reduce Leakage in Deep-Submicron Cache Memories. *ISLPED'00: Proceedings of the* 2000 *International Symposium on Low Power Electronics and Design*, Rapallo, 25-27 July 2000, 90-95. https://doi.org/10.1145/344166.344526

[80] Powell, M., Yang, S.H., Falsafi, B., Roy, K. and Vijaykumar, T.N. (2001) Reducing Leakage in a High-Performance Deep-Submicron Instruction Cache. *IEEE Transactions on Very Large Scale Integration Systems*, **9**, 77-89. https://doi.org/10.1109/92.920821

[81] Ye, Y., Borkar, S. and De, V. (1998) A New Technique for Standby Leakage Reduction in High-Performance Circuits. 1998 *Symposium on VLSI Circuits*, Honolulu, 11-13 June 1998, 69-70.

[82] Agarwal, A., Li, H. and Roy, K. (2003) A Single-Vt Low-Leakage Gated-Ground Cache for Deep Submicron. *IEEE Journal of Solid-State Circuits*, **38**, 319-328. https://doi.org/10.1109/JSSC.2002.807414

[83] Agarwal, A., Li, H. and Roy, K. (2002) DRG-Cache: A Data Retention Gated-

Ground Cache for Low Power. *Proceedings of the Design Automation Conference*, New Orleans, 10-14 June 2002, 473-478. https://doi.org/10.1145/513918.514037

[84] Elakkumanan, P., Narasimhan, A. and Sridhar, R. (2003) NC-SRAM—A Low-Leakage Memory Circuit for Ultra Deep Submicron Designs. *Proceedings of IEEE International SOC Conference*, Portland, 17-20 September 2003, 3-6. https://doi.org/10.1109/soc.2003.1241450

[85] Goel, A., Sharma, R.K. and Gupta, A. (2014) Area Efficient Diode and on Transistor Inter-Changeable Power Gating Scheme with Trim Options for SRAM Design in Nano-Complementary Metal Oxide Semiconductor Technology. *IET Circuits, Devices & Systems*, **8**, 100-106. https://doi.org/10.1049/iet-cds.2013.0205

[86] Bhavnagarwala, A.J., Kosonocky, S.V., Immediato, M., Knebel, D. and Haen, A.M. (2003) A Pico-Joule Class, 1 GHz, 32 kB 64 b DSP SRAM with Self Reversed Bias. 2003 *Symposium on VLSI Circuits*, Kyoto, 12-14 June 2003, 251-252.

[87] Min, I. and Kanda, K. (2003) Row-by-Row Dynamic Source-Line Voltage Control (RRDSV) Scheme for Two orders of Magnitude Leakage SRAM's Current Reduction of Sub-1-V-Vdd. 2003 *International Symposium on Low Power Electronics and Design*, Seoul, 25-27 August 2003, 66-71.

[88] Devices, M., Yang, H., Member, S., Hwang, W. and Chuang, C. (2011) Impacts of NBTI/PBTI and Contact Resistance on Power-Gated SRAM with High-. *IEEE Transactions on Very Large Scale Integration Systems*, **19**, 1192-1204. https://doi.org/10.1109/TVLSI.2010.2049038

[89] Xie, L., Liu, J. and Wang, Y. (2014) A Low Power CMOS Voltage Reference Generator with Temperature and Process Compensation. *Analog Integrated Circuits and Signal Processing*, **81**, 313-324. https://doi.org/10.1007/s10470-014-0360-7

[90] Zhang, K., Bhattacharya, U., Chen, Z., Hamzaoglu, F., Murray, D., Vallepalli, N. and Bohr, M. (2005) SRAM Design on 65-nm CMOS Technology with Dynamic Sleep Transistor for Leakage Reduction. *IEEE Journal of Solid-State Circuits*, **40**, 895-900. https://doi.org/10.1109/JSSC.2004.842846

[91] Khellah, M., Somasekhar, D., Ye, Y., Kim, N.S., Howard, J., Ruhl, G. and De, V. (2007) A 256-Kb dual-Vcc SRAM Building Block in 65-nm CMOS Process with Actively Clamped Sleep Transistor. *IEEE Journal of Solid-State Circuits*, **42**, 233-241. https://doi.org/10.1109/JSSC.2006.888357

[92] Goel, A., Evans, D., Stephani, R., Reddy, V., Rai, D., Chary, V. and Sathisha, N. (2012) An Area Efficient Diode and on Transistor Interchangeable Power Gating Scheme with Trim Options for Low Power SRAMs. *Proceedings of the IEEE International Conference on VLSI Design*, Hyderabad, 7-11 January 2012, 80-84. https://doi.org/10.1109/vlsid.2012.50

[93] Itoh, K., Nakagome, Y. and Sasaki, K. (1995) Trends in Low-Power RAM Circuit Technologies. *Proceedings of the IEEE*, **83**, 524-543. https://doi.org/10.1109/5.371965

[94] Mutoh, S., Douseki, T., Matsuya, Y., Aoki, T., Shigematsu, S. and Yamada, J. (1995) 1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS. *IEEE Journal of Solid-State Circuits*, **30**, 847-854. https://doi.org/10.1109/4.400426

[95] Bikki, P. and Karuppanan, P. (2016) Analysis of Low Power and High Performance Multi-Vth Dual Mode Logic Design. Presented at the 11th International IEEE Conference (ICIIS-2016), IIT-Roorkee.

[96] Bhavnagarwala, A.J., Tang, X. and Meindl, J.D. (2001) The Impact of Intrinsic Device Fluctuations on CMOS SRAM Cell Stability. *IEEE Journal of Solid-State Circuits*, **36**, 658-665. https://doi.org/10.1109/4.913744

[97] Azizi, N., Member, S., Najm, F.N., Moshovos, A. and Member, A. (2003) Low-Leakage Asymmetric-Cell SRAM. *IEEE Transactions on Very Large Scale Integration Systems*, **11**, 701-715. https://doi.org/10.1109/TVLSI.2003.816139

[98] Azizi, N. and Moshovos, A. (2002) Asymmetric-Cell Caches: Exploiting Bit Value Biases to Reduce Leakage Power in Deep-Submicron, High-Performance Caches. TR-01-01-02, ECE Dept., Univ. of Toronto, Toronto, 1-14. http://www.eecg.toronto.edu/~moshovos/research/asram-tr.pdf

[99] Calhoun, B.H. and Chandrakasan, A.P. (2007) A 256-kb 65-nm Sub-Threshold SRAM Design for Ultra-Low-Voltage Operation. *IEEE Journal of Solid-State Circuits*, **42**, 680-688. https://doi.org/10.1109/JSSC.2006.891726

[100] Do, A.T., Nguyen, T.Q., Yeo, K.S. and Kim, T.T. (2013) Sensing Margin Enhancement Techniques for Ultra-Low-Voltage SRAMs Utilizing a Bitline-Boosting Current and Equalized Bitline Leakage. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **59**, 868-872. https://doi.org/10.1109/TCSII.2012.2231014

[101] Chen, S.H., Lin, Y.L. and Chao, M.C.T. (2013) Power-Up Sequence Control for MTCMOS Designs. *IEEE Transactions on Very Large Scale Integration Systems*, **21**, 413-423. https://doi.org/10.1109/TVLSI.2012.2187689

[102] Kim, T.H., Liu, J. and Kim, C.H. (2009) A Voltage Scalable 0.26 V, 64 kb 8T SRAM with Vmin Lowering Techniques and Deep Sleep Mode. *IEEE Journal of Solid-State Circuits*, **44**, 1785-1795. https://doi.org/10.1109/JSSC.2009.2020201

[103] Alvandpour, A., Somasekhar, D., Krishnamurthy, R., De, V., Borkar, S. and Svensson, C. (2003) Bitline Leakage Equalization for Sub-100nm Caches. *European Solid-State Circuits Conference*, Estoril, 16-18 September 2003, 401-404. https://doi.org/10.1109/esscirc.2003.1257157

[104] Wang, B., Nguyen, T.Q., Do, A.T., Zhou, J., Je, M. and Kim, T.T.H. (2015) Design of an Ultra-Low Voltage 9T SRAM with Equalized Bitline Leakage and CAM-Assisted Energy Efficiency Improvement. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **62**, 441-448. https://doi.org/10.1109/TCSI.2014.2360760

[105] Teman, A., Pergament, L., Cohen, O. and Fish, A. (2011) A 250 mV 8 kb 40 nm Ultra-Low Power 9T Supply Feedback SRAM (SF-SRAM). *IEEE Journal of Solid-State Circuits*, **46**, 2713-2726. https://doi.org/10.1109/JSSC.2011.2164009

[106] Mezhibovsky, J., Teman, A. and Fish, A. (2011) Low Voltage SRAMs and the Scalability of the 9T Supply Feedback SRAM. *International System on Chip Conference*, Taipei, 26-28 September 2011, 136-141.

[107] Kawaguchi, H., Itaka, Y. and Sakurai, T. (1998) Dynamic Leakage Cut-Off Scheme for Low-Voltage SRAM's. 1998 *Symposium on VLSI Circuits*, Honolulu, 11-13 June 1998, 140-141. https://doi.org/10.1109/vlsic.1998.688035

[108] Kim, C.H. and Roy, K. (2002) Dynamic Vt SRAM: A Leakage Tolerant Cache Memory for Low Voltage Microprocessors. *Proceedings of the International Symposium on Low Power Electronics and Design*, California, 12-14 August 2002, 251-254. https://doi.org/10.1145/566408.566473

[109] Yamauchi, H., Iwata, T., Akamatsu, H., Matsuzawa, A. and Introduction, I. (1996) A 0.8V/100MHz/sub-5mW-Operated Mega-Bit SRAM Cell Architecture with Charge-Recycle Offset-Source Driving (OSD) Scheme. 1996 *Symposium on VLSI Circuits*, Honolulu, 13-15 June 1996, 126-127.

[110] Osada, K., Saitoh, Y., Ibe, E. and Ishibashi, K. (2003) 16.7fA/Cell Tunnel-Leakage-Suppressed 16Mb SRAM for Handling Cosmic-Ray-Induced Multi-Errors. *IEEE International Solid-State Circuits Conference*, San Franciso, 13 February 2003, 168-169.

Abbreviations

BTBT	Band-to-band tunneling
BL	Bit line
BLB	Bit line bar
CMOS	Complementary metal oxide semiconductor
DIBL	Drain-induced barrier lowering
DRG	Data retention gated-ground
D2D	Die to die
FBB	Forward body biasing
GIDL	Gate-induced drain leakage
I_{BTBT}	Band to band tunneling effect
I_{gc}	Gate-to-channel current
I_{GIDL}	Gate-induced drain leakage
I_{Punch}	Punch-through leakage
I_{Sdif}	Sub-threshold surface diffusion current
$I_{\text{Sub-th}}$	Sub-threshold leakage current
Low-V_{TH}	Low threshold voltage
NBTI	Negative bias temperature instability
PBTI	Positive bias temperature instability
PBT	Programmable bias transistor
PD	Pull-down
RBB	Reverse body bias
RBL	Read word line
SBT	Self-biasing transistor
SCE	short-channel effect
SNM	Signal to noise margin
SRAM	Static random access memory
SRB	Self-reverse biasing
VTCMOS	Variable threshold CMOS
V_{SL}	Virtual source line