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Indirect Output Voltage Control in Negative Output Elementary Super Lift Luo Converter Using PIC plus FLC in Discontinuous Conduction Mode

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Abstract

In this paper, the design of a proportional integral controller (PIC) plus fuzzy logic controller (FLC) for the negative output elementary super lift Luo converter (NOESLLC) operated in discontinuous conduction mode (DCM) is presented. In spite of the many benefits *viz.* the high voltage transfer gain, the high efficiency, and the reduced inductor current and the capacitor voltage ripples, it natured with non-minimum phase. This characteristic makes the control of NOESLLC cumbersome. Any attempt of direct controlling the output voltage may erupt to instability. To overcome this problem, indirect regulation of the output voltage based on the two-loop controller is devised. The savvy in the inductor current control improves the dynamic response of the output voltage. The FLC is designed for the outer (voltage) loop while the inner (current) loop is controlled by the PIC. For the developed −19.6 V NOESLLC, the dynamic performances for different perturbations (line, load and component variations) are obtained for PIC plus FLC and compared with PIC plus PIC. The study of two cases is performed at various operating regions by developing the MATLAB/Simulink model.

Keywords

Negative Output Elementary Super Lift Luo Converter (NOESLLC), Discontinuous Conduction Mode (DCM), Fuzzy Logic Controller (FLC), Proportional-Integral Controller (PIC)

1. Introduction

The voltage lift (VL) technique is a relatively new technique to employ in dc-dc converter topologies. In the topologies discussed hitherto, the parasitic elements dissuade the output voltage and power transfer efficiency of dc-dc converters, while the VL technique can lead to improvement [1] [2]. After enduring investigation, this technique has been lucratively applied for dc-dc converters. For instance, the positive output Luo converters and negative output Luo converters are series of relatively new dc-dc step-up (boost) converters, which were developed by incorporating the VL technique. The negative output converters perform positive to negative dc-dc voltage-increasing conversion with high power density, high efficiency and cheap topology in simple structure. They are different from other existing dc-dc step-up converters and possess many advantages, including a high output voltage with small ripples. Therefore, these converters will be widely used in computer peripheral equipment, liquid crystal display (LCD), organic light-emitting diode (OLED), active-matrix LCD (AMLCD) etc. and industrial applications, especially for high output voltage projects [3]. The conventional converters may not suit for these applications as they employ a switching-boost converter with several off-chip components to generate the required negative voltages. In contrary, the converter scheme needs to achieve high performance with a minimum number of off-chip components and be capable of generating a wide range of negative voltages by varying the reference voltage.

The negative output elementary super lift Luo converter (NOESLLC) is a one of the attractive dc-dc converter and possesses the features *viz.* high voltage transfer gain (in geometric progression), an excellent efficiency, a suppressed inductor/capacitor ripples [4] [5]. As other dc-dc converters, the NOESLLC can also be operated in the continuous conduction mode (CCM) and discontinuous conduction mode (DCM). In CCM, the inductor current of the converter never falls to zero; a right half plane zero (RHPZ) is unavoidable. The DCM does not have RHPZ, improves system stability, avoids the reverse recovery problem of the diode and also becomes more suitable for low power application [6] [7].

A novel negative output converter (negative-output KY buck-boost converter) has been presented [8]. Development of proportional integral derivative (PID) and fuzzy logic controllers for paralleled negative output Luo converters has been detailed and performance tested using MATLAB software [9]. The design and construction of a multivariable fuzzy controller (MFLC) for the control of a dc-dc buck converter has been presented [10]. The developed off-the-shelf hardware-based MFLC system can be used to model the variable switching structure of the buck converter. The MFLC design criterion is based on the error in output voltage and the change of error in the output voltage as inputs of the controller, and the changes in the duty cycle ratio as output of the controller. The stability of the dc-dc converters, particularly for the negative impedance induced instabilities, has been addressed [11].

The introduced pulse adjustment technique is a digital control technique to control dc-dc converters loaded by constant power loads. This novel digital control treats con-

verter as a digital system and regulates output voltage with the help of two predefined state variables. A genetic algorithm (GA) tuned proportional integral controller (PIC) has been devised for NOESLLC [12]. Due to the time-varying and switching nature of the NOESLLC, its dynamic behavior becomes highly non-linear. Conventional controllers are incapable of providing good dynamic performance for such a converter and hence double controller based system is required [13]. This paper proposes a proportional integral controller (PIC) plus fuzzy logic controller (FLC) for the −19.6 V output NOESLLC working in DCM. The FLC is designed for the outer (voltage) loop while the inner (current) loop is controlled by the PIC. The transient performance of the proposed controller is validated for different perturbations (line, load and component variations) and compared with PIC plus PIC. The methodologies adapted are MATLAB-Simulink simulation.

2. Analysis of DCM Operation of NOESLLC

2.1. Operation of NOESLLC

The power circuit of NOESLLC is shown in **Figure 1(a)**, and the state/mode 1 (switch Q ON) and 2 (Q OFF) operations are respectively presented in **Figure 1(b)** and **Figure 1(c)**. The state 3 (DCM) is indicated in **Figure 1(d)** while the inductor current is pictured in **Figure 1(e)**. The capacitor voltage can be assumed as constant as the common selection of capacitor is much higher than the minimum demanded value.

In the **Figure 1(e)**, T is the switching time period and d is the duty cycle. During the period $\left[(d+d')T \le t \le T\right]$, the current through the inductor is zero; switch is in OFF state, and diodes D1 and D2 are in OFF state as shown in **Figure 1(d)** [1]-[3]. From the **Figure 1(e)**, the condition of DCM is expressed as

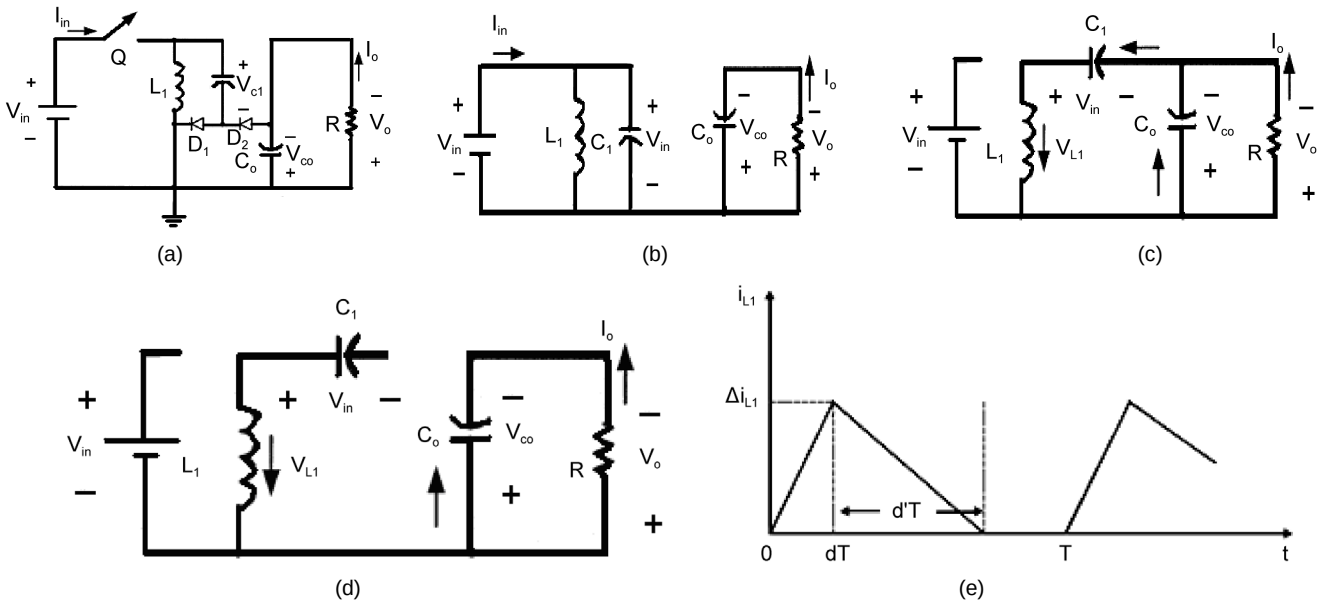


Figure 1. The NOESLLC (a) circuit topology, (b) state 1 operation, and (c) state 2 operation, (d) equivalent circuit during turn-off mode (DCM operation) and (e) discontinuous inductor current waveform.

$$d + d' < 1 \tag{1}$$

During $0 \le t \le \mathrm{d}T$, i_{L1} increases with slope V_{in}/L_1 and during $dT \le t \le (d+d')T$, i_{L1} decreases with slope $-(V_o - V_{in})/L_1$. Hence,

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} dT = \frac{V_o - V_{in}}{L_1} d'T \tag{2}$$

The above Equation (2) can be simplified as

$$V_{in} d = (V_o - V_{in}) d' \tag{3}$$

In the steady state condition, the average capacitor current is zero. Considering the current in C_o in **Figure 1(b)**, **Figure 1(c)** and **Figure 1(d)**, the following relations are obtained;

$$d'T\left(\frac{1}{2}\Delta i_{L_1} - I_o\right) = dTI_o + (1-d-d')TI_o = (1-d')TI_o \tag{4}$$

Using $\Delta i_{L_1} = \frac{V_{in}}{L_1} dT$ from (2), and substituting $I_o = \frac{V_o}{R}$ and $T = \frac{1}{f}$ in (4) results in (5)

$$\frac{1}{2}\frac{V_{in} d' d}{f L_1} = \frac{V_o}{R_o} \tag{5}$$

Combining (3) and (5) becomes

$$d' = \frac{dV_{in}}{V_o - V_{in}} = \frac{2 f L_1 V_o}{V_{in} dR} \tag{6}$$

Next, defining the voltage transfer gain $G = V_o/V_{in}$ in Equation (6) gives

$$d' = \frac{d}{G-1} = \frac{2 f L_1 G}{d R} \tag{7}$$

Therefore,

$$G^2 - G - \frac{d^2 R}{2 L_1 f} = 0 \tag{8}$$

Solving the Equation (8), expresses the voltage transfer gain as follows.

$$G = \frac{1}{2}\left(1 + \sqrt{1 + 2d^2 \frac{R}{L_1 f}}\right) \tag{9}$$

2.2. Condition of DCM and Validation

The condition of DCM is expressed in (1). Substitution of (7) in (1) gives,

$$d + \frac{d}{G-1} < 1 \Rightarrow \frac{d}{G-1} < 1-d \Rightarrow \frac{G-1}{d} > \frac{1}{1-d} \Rightarrow G-1 > \frac{d}{1-d} \Rightarrow G > \frac{1}{1-d} \tag{10}$$

Substitution of (9) into (10) engraves as (11)

$$\left(1+\sqrt{1+2d^2\frac{R}{L_1 f}}\right)>\frac{2}{1-d}\Rightarrow 1+2d^2\frac{R}{L_1 f}>\left(\frac{2}{1-d}-1\right)^2=\left(\frac{1+d}{1-d}\right)^2$$
$$\Rightarrow 2d^2\frac{R}{L_1 f}>\left(\frac{1+d}{1-d}\right)^2-1=\frac{4d}{(1-d)^2}\Rightarrow\frac{R}{L_1 f}>\frac{2}{d(1-d)^2} \quad (11)$$

The Equation (11) is the condition for DCM in the NOESLLC. This equation can be verified from the variation ratio of inductor current in CCM.

$$\xi=\frac{\Delta i_{L_1/2}}{i_{L_1}}=d(1-d)^2\frac{R}{2fL_1} \quad (12)$$

where, $\xi<1$ in the CCM and $\xi>1$ in the DCM. Then the DCM condition is

$$d(1-d)^2\frac{R}{2fL_1}>1\Rightarrow\frac{R}{L_1 f}>\frac{2}{d(1-d)^2} \quad (13)$$

The Equation (13) agrees with Equation (11)

$$\frac{R}{L_1 f}<g(d) \quad (14)$$

where, $g(d)=\frac{d(1-d)^2}{2}$ for which $0 < d < 1$. The maximum range of $g(d)$ is derived as

$$g'(d)=\frac{1}{2}\left(3d^2-4d+1\right)=0\Rightarrow d=\frac{1}{3}\Rightarrow g_{\max}(d)=g\left(\frac{1}{3}\right)=\frac{2}{27} \quad (15)$$

Equation (15) can be depicted graphically as shown in Figure 2, where, $d_1 < d < d_2$ corresponds to the DCM. But, if $\frac{L_1 f}{R}>\frac{2}{27}$, then the NOESLLC operates in the CCM. The derivation of variation ratio of the capacitor voltages can be expressed as (16).

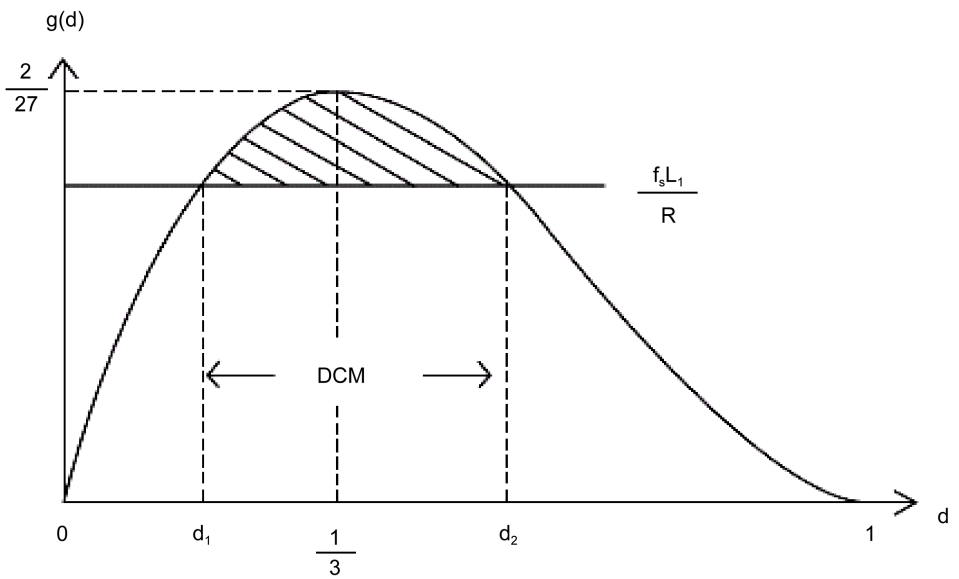


Figure 2. Graphical analysis of Equation (15).

$$\Delta V_o = \frac{\Delta Q}{C_o} = \frac{I_o dT + I_o(1-d-d')T}{C_o} = \frac{I_o(1-d')T}{C_o} = \frac{V_o(1-d')}{RfC_o} \tag{16}$$

$$\varepsilon = \frac{\Delta V_O/2}{V_o} = \frac{(1-d')}{2RfC_o}$$

where,

$$1-d' = \frac{\Delta Q}{C_o} = 1 - \frac{2L_1 fG}{dR} = 1 - \frac{L_1 f}{dR}\left(1+\sqrt{1+2d^2\frac{R}{L_1 f}}\right) \tag{17}$$

2.3. Design of NOESLLC Circuit Elements in DCM

Using the above model equations, the detailed design and specifications of NOESLLC circuit is obtained and recorded in Table 1.

3. Design of Control Methodology

This section studies the DCM operation of NOESLLC with two different combinations of double controllers. The considered PIC plus PIC and PIC plus FLC controller combinations with the proposed scheme of control is illustrated in Figure 3. The double controller combination assumes an inner current loop with PIC to guide the inductor current and an outer voltage control loop utilizes either FLC or PIC. The voltage controller sets the mean value reference inductor current value for the inner current loop. The inputs to the outer loop controller are reference voltage and actual measured voltage. The measured current is compared with the reference current and the resulting current error is fed to the inner loop controller. The scaled control command is fed to the defined hysteresis band to generate the switching pulse for Q.

Table 1. Specifications of the NOESLLC (application in digital camera).

Parameters name	Symbol	Value
Input voltage	V_{in}	10 V
Output voltage	V_o	−19.6 V
Inductor	L_1	45 μH
Capacitors	C_1, C_o	4.7 μF, 22 μF
Nominal switching frequency	f	100 kHz
Load resistance	R	416.16.
Average input current	I_{in}	0.11 A
Efficiency	η	82.5%
Average output current	I_o	−0.047 A
Duty ratio	d	0.2
	D'	0.21
Peak to peak capacitor ripple	ΔV_o	−0.01 V

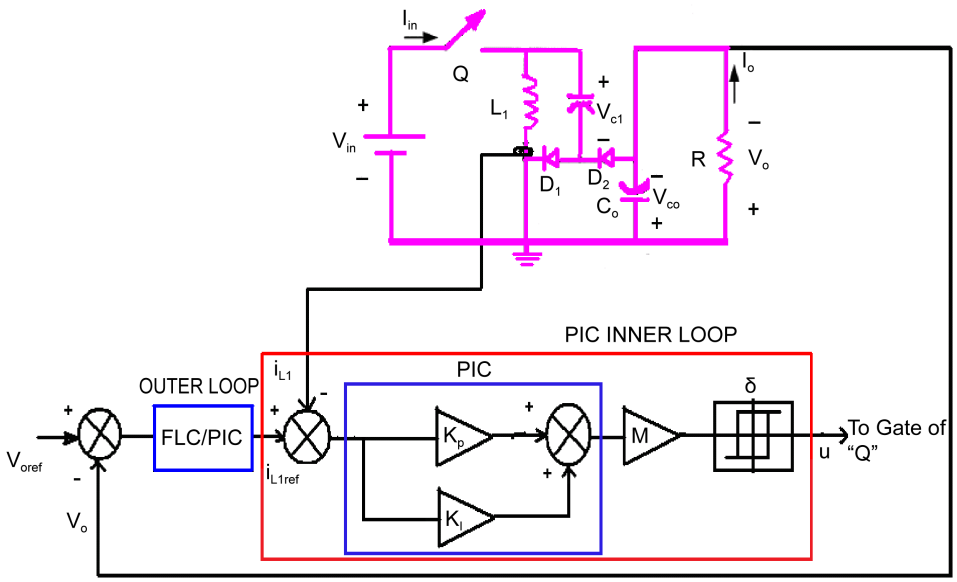


Figure 3. Proposed PIC plus FLC/PIC for NOESLLC in DCM.

4. Simulation Study and Results

This section deals about the simulation study and results of NOESLLC in DCM using PIC plus FLC/PIC. The NOESLLC in DCM performance is verified at various conditions *viz.* start-up transient, line variation, load variation, and also circuit components variations. The MATLAB/SIMULINK simulation models are performed on the NOESLLC in DCM with specifications listed in Table 1.

4.1. Start-Up Region

Figure 4 shows the simulated output voltage results of NOESLLC in DCM using the PIC plus FLC and PIC plus PIC in start-up transient region with nominal input voltage. From these figure, it is evident that the output voltage of the NOESLLC in DCM has overshoots = −0.02 V, settling time of 0.0038 s, and little steady state error around −0.12 V using PIC plus FLC. But the same converter with PIC plus PIC causes peak overshoots of −2.6 V and settling time of 6.25 ms during start-up transient region.

4.2. Line Variation

Figure 5 shows the simulated output voltage and inductor current results of NOESLLC in DCM using the PIC plus FLC and PIC plus PIC for input voltage change from 10V to 13 V at time of 0.05 s with R = 416.6 Ω. From the Figures 5(a)-(c), it is clearly focused that the output voltage of the NOESLLC in DCM has overshoots = −0.018 V, settling time of 0.0035 s, and steady state error around −0.12 V using PIC plus FLC, whereas the NOESLLC in DCM with PIC plus PIC has produced peak overshoots of −1.95 V and settling time of 6.25 ms during line disturbance region. Figure 5(c) indicates that the inductor current of NOESLLC in DCM with controllers has produced null overshoots and settling time in line variation.

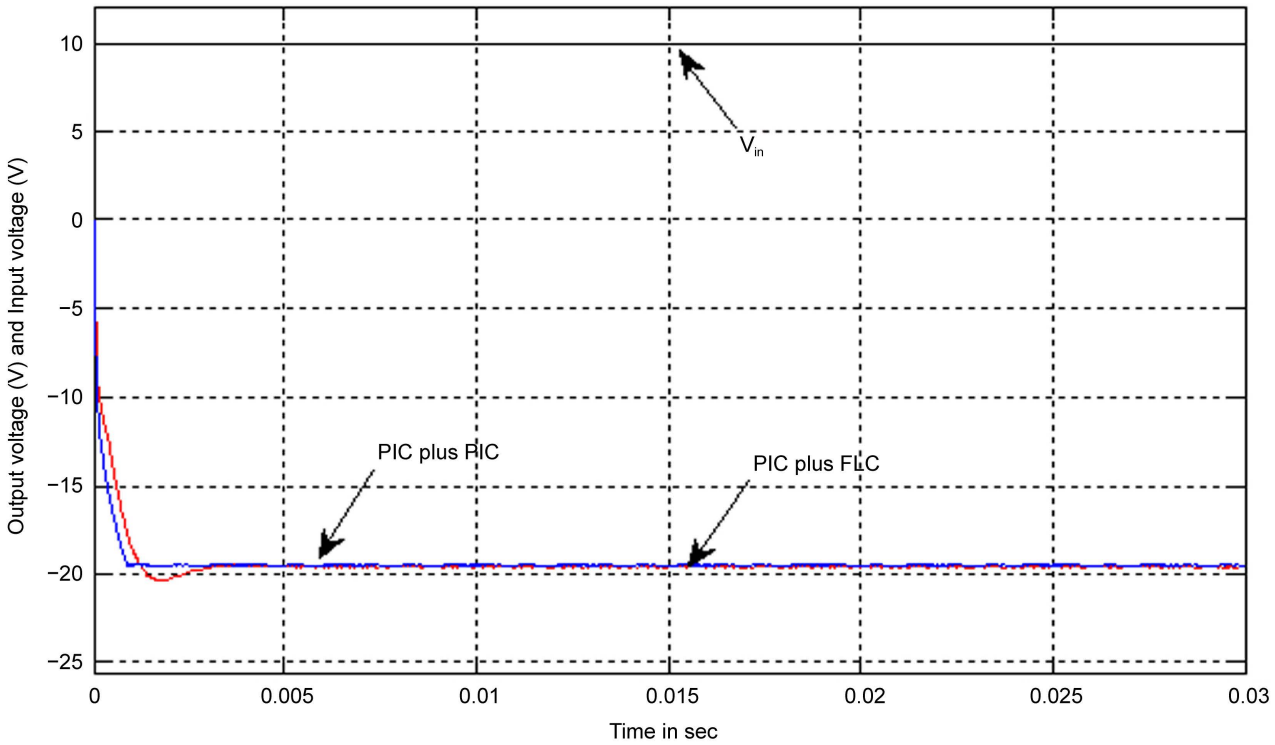
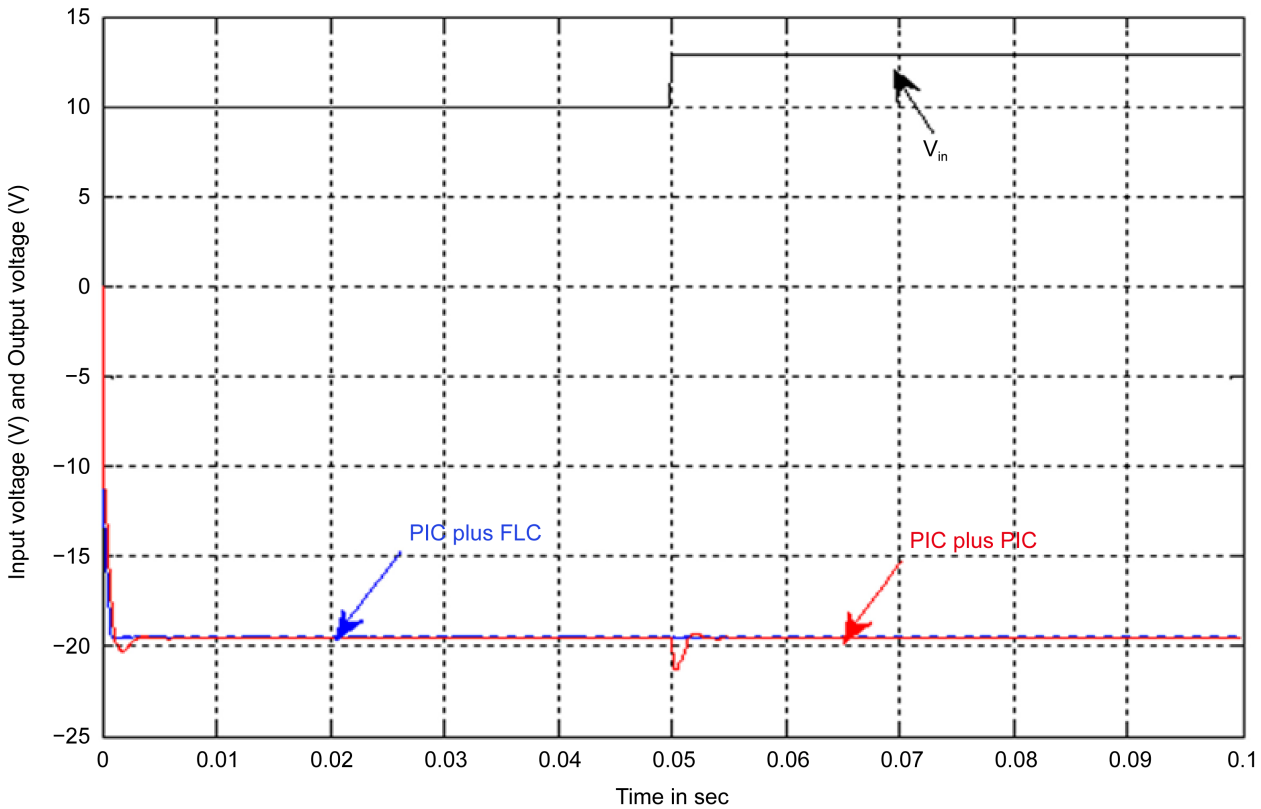
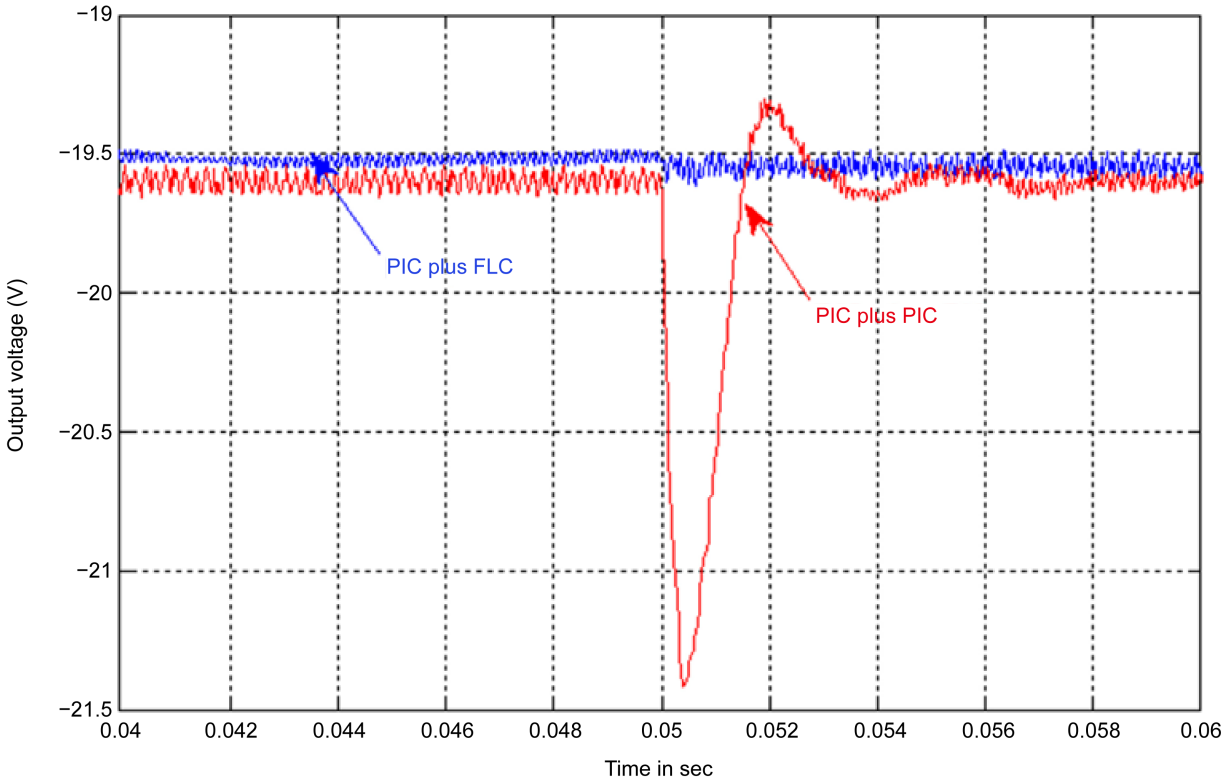


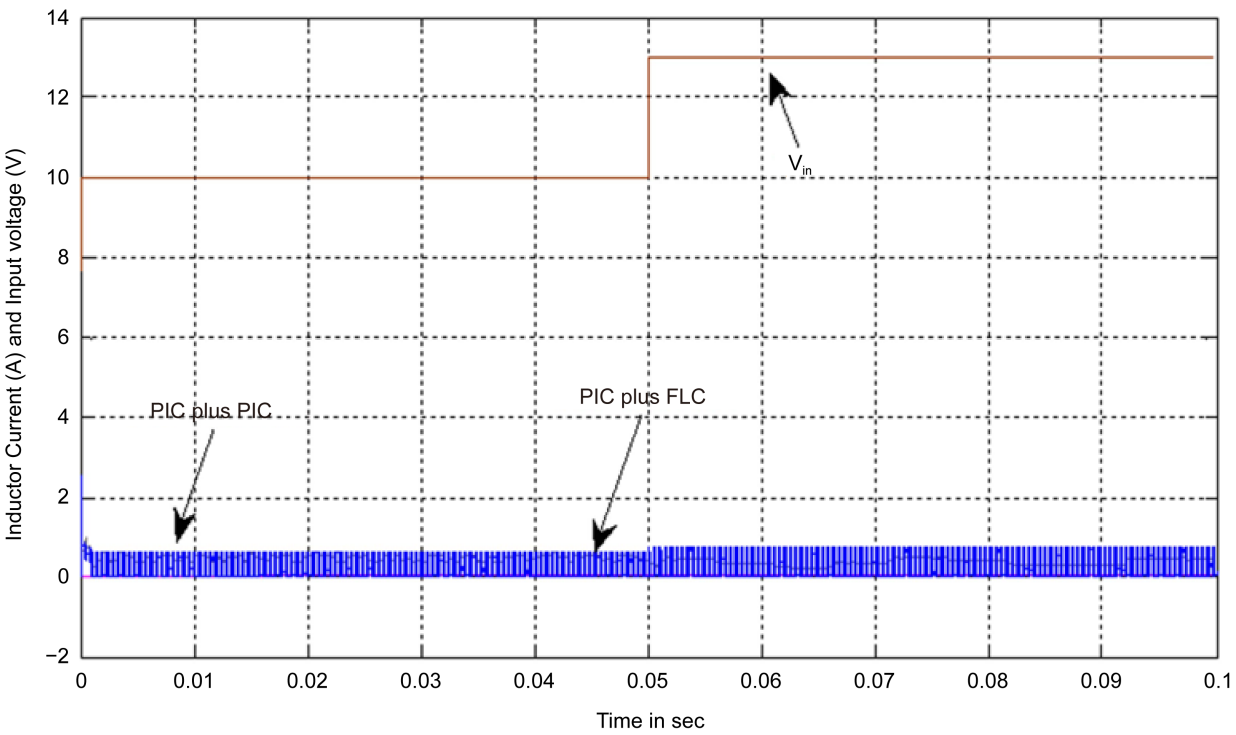
Figure 4. Simulated start up output voltage responses with rated input voltage.



(a)



(b)



(c)

Figure 5. Response with PIC plus FLC and PIC plus PIC for input step change from 10 V to 13 V at time of 0.05 s with R = 416.6 Ω, (a) output voltage (b) zoomed view of output voltage, and (c) inductor current.

Figure 6 shows the simulated output voltage and inductor current results of NOESLLC in DCM using the PIC plus FLC and PIC plus PIC for input voltage change from 10 V to 7 V at time of 0.05 s with R = 416.6 Ω.

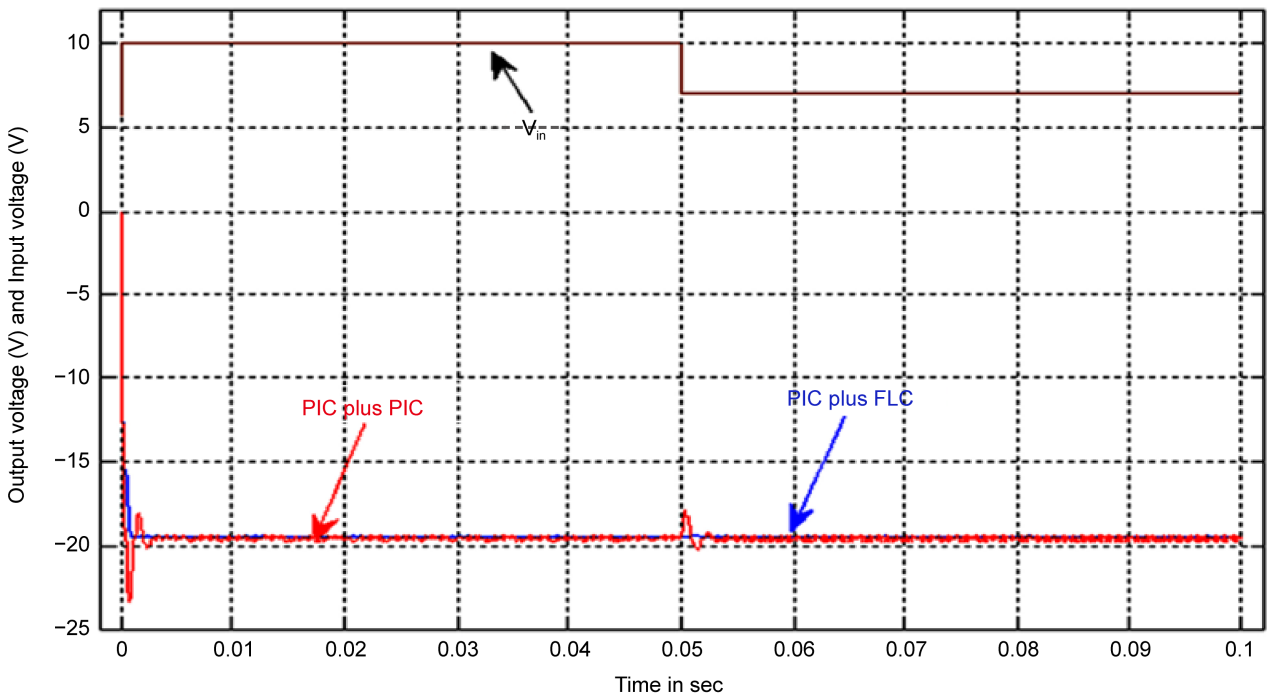
From the Figures 6(a)-(c), it is clearly focused that the output voltage of the NOESLLC in DCM has overshoots = −0.021 V, settling time of 0.0032 s, and steady state error around −0.12 V using PIC plus FLC, while the NOESLLC in DCM with PIC plus PIC has produced peak overshoots of −2.12 V and settling time of 6.22 ms during line disturbance region. Figure 6(c) indicates that the inductor current of NOESLLC in DCM with controllers has produced null overshoots and settling time in line variation.

4.3. Load Variation

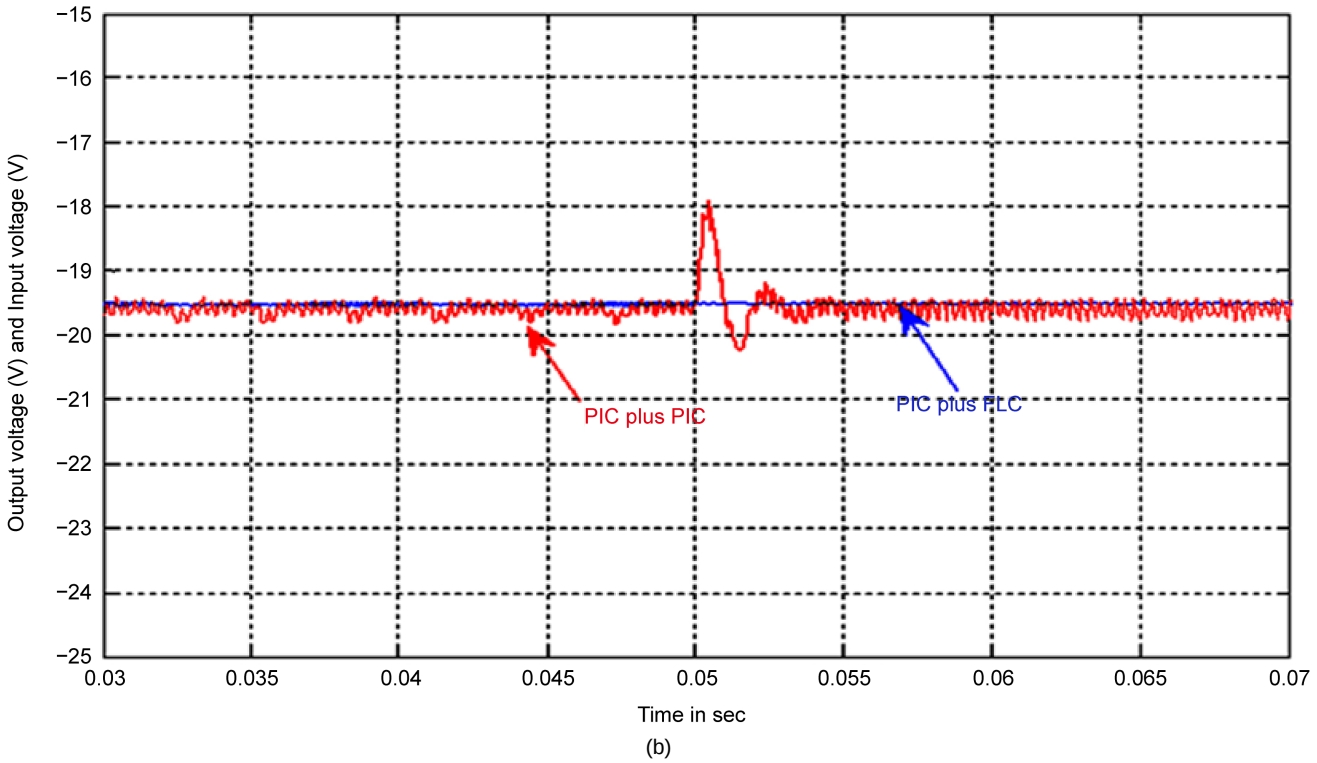
Figure 7 shows the simulated output voltage, output current, and inductor current results of NOESLLC in DCM using the PIC plus FLC and PIC plus PIC for load resistance change 416.6 Ω to 316.6 Ω at time of 0.05 s with input voltage of 10 V.

From the Figure 7(a), and Figure 7(b), it is clearly focused that the output voltage of the NOESLLC in DCM has overshoots = −0.02 V, settling time of 0.0034 s, and steady state error around −0.1 V using PIC plus FLC, while the NOESLLC in DCM with PIC plus PIC has produced peak overshoots of −5.12 V and settling time of 0.53 ms during load disturbance region. Figure 7(c) indicates that the inductor current and output current of NOESLLC in DCM with controllers has produced null overshoots and settling time in load variation.

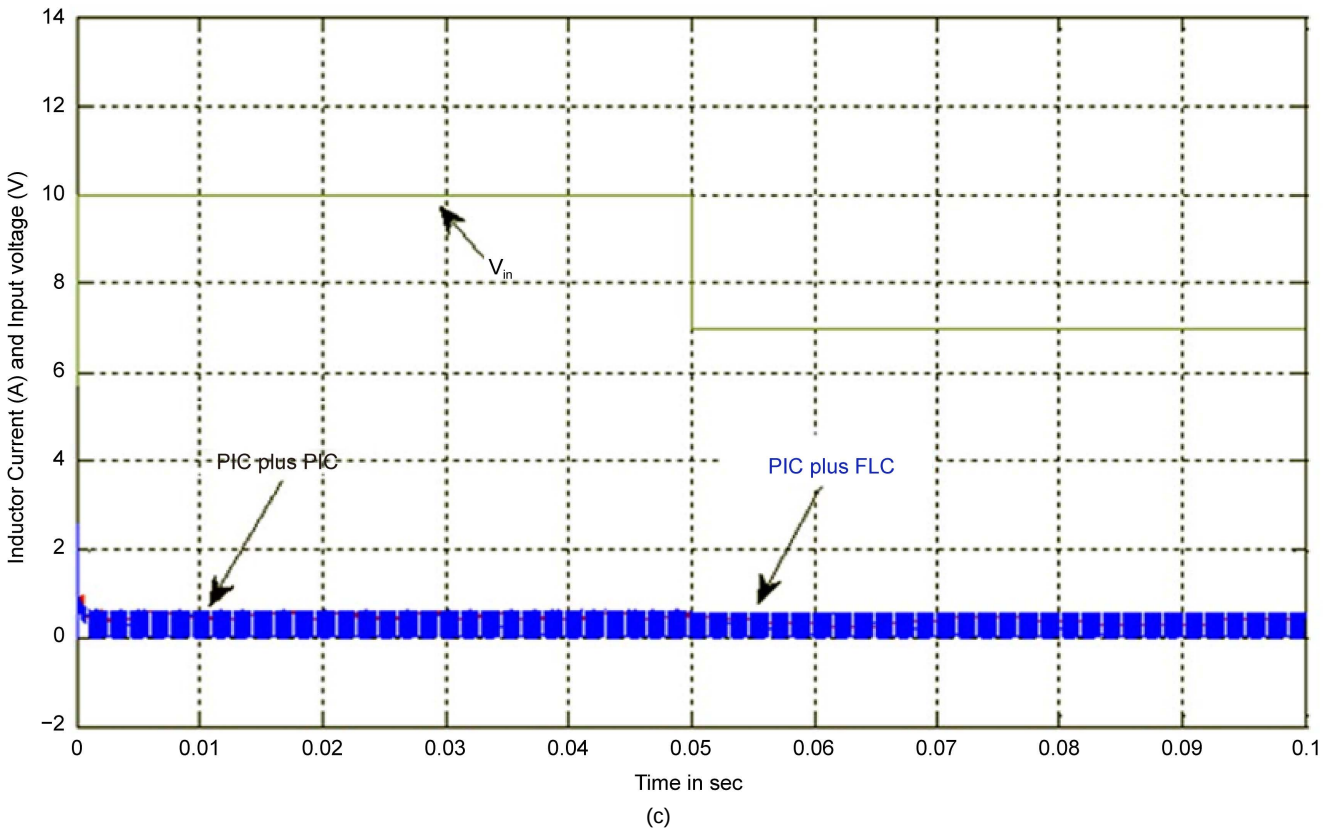
Figure 8 shows the simulated output voltage, output current, and inductor current results of NOESLLC in DCM using the PIC plus FLC and PIC plus PIC for load



(a)

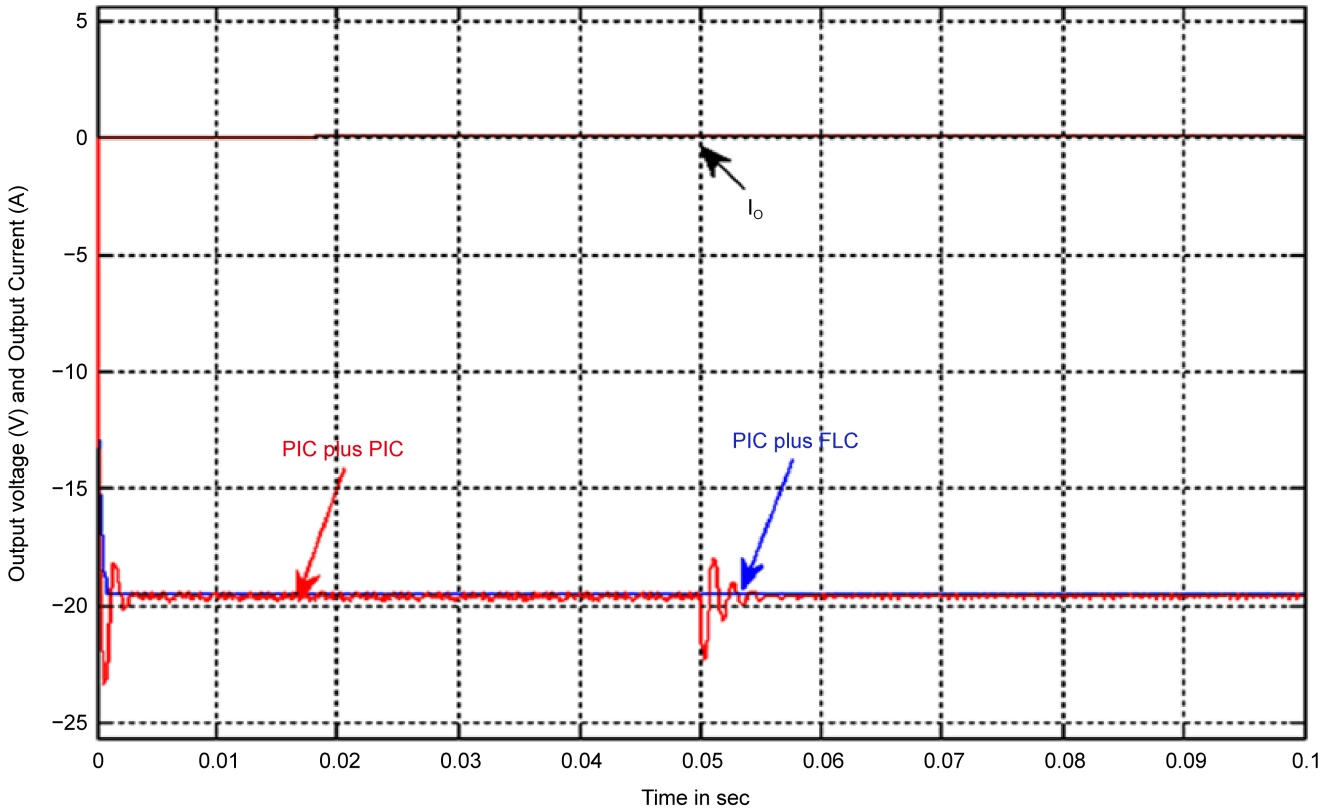


(b)

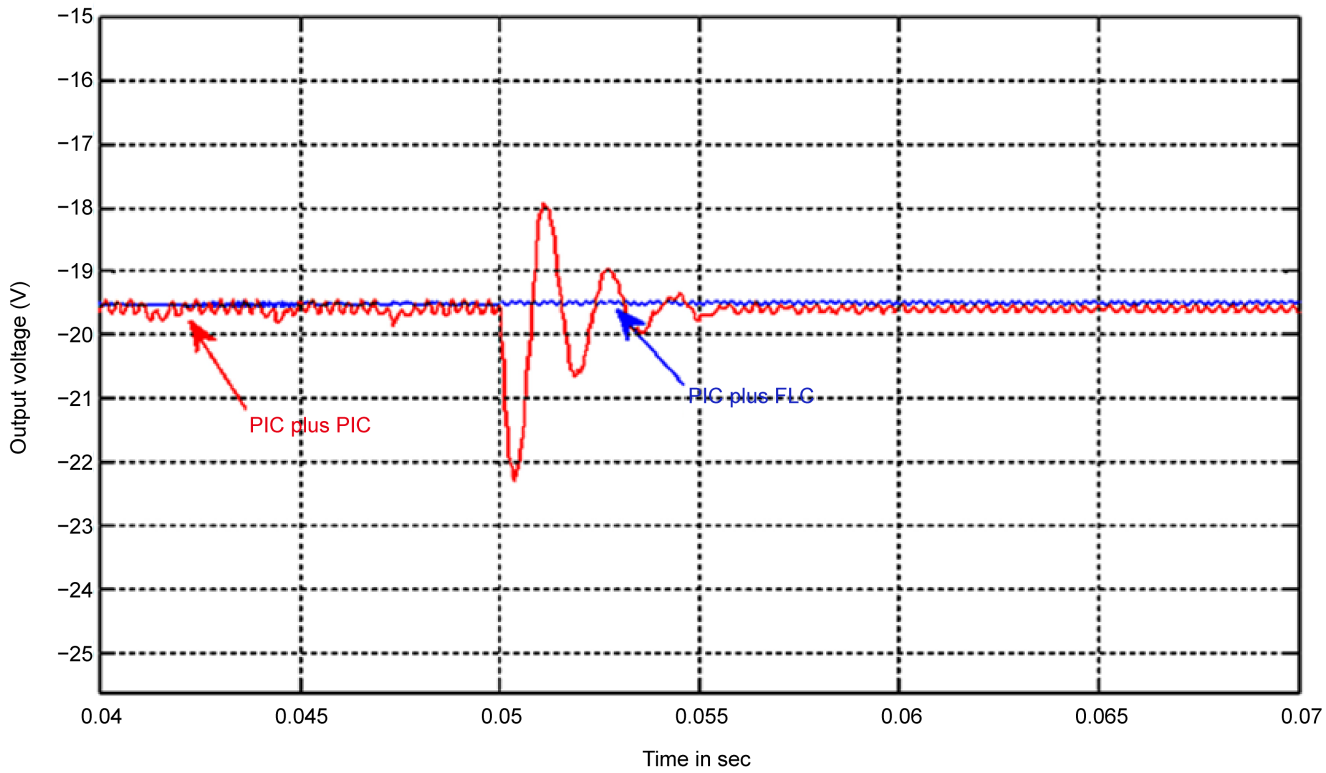


(c)

Figure 6. Response with PIC plus FLC and PIC plus PIC for input step change from 10 V to 07 V at time of 0.05 s with R = 416.6 Ω, (a) output voltage (b) zoomed view of output voltage, and (c) inductor current.


Output voltage (V) and Output Current (A)
Time in sec
I_O
PIC plus PIC
PIC plus FLC
5
0
−5
−10
−15
−20
−25
0
0.01
0.02
0.03
0.04
0.05
0.06
0.07
0.08
0.09
0.1

(a)


Output voltage (V)
Time in sec
PIC plus PIC
PIC plus FLC
−15
−16
−17
−18
−19
−20
−21
−22
−23
−24
−25
0.04
0.045
0.05
0.055
0.06
0.065
0.07

(b)

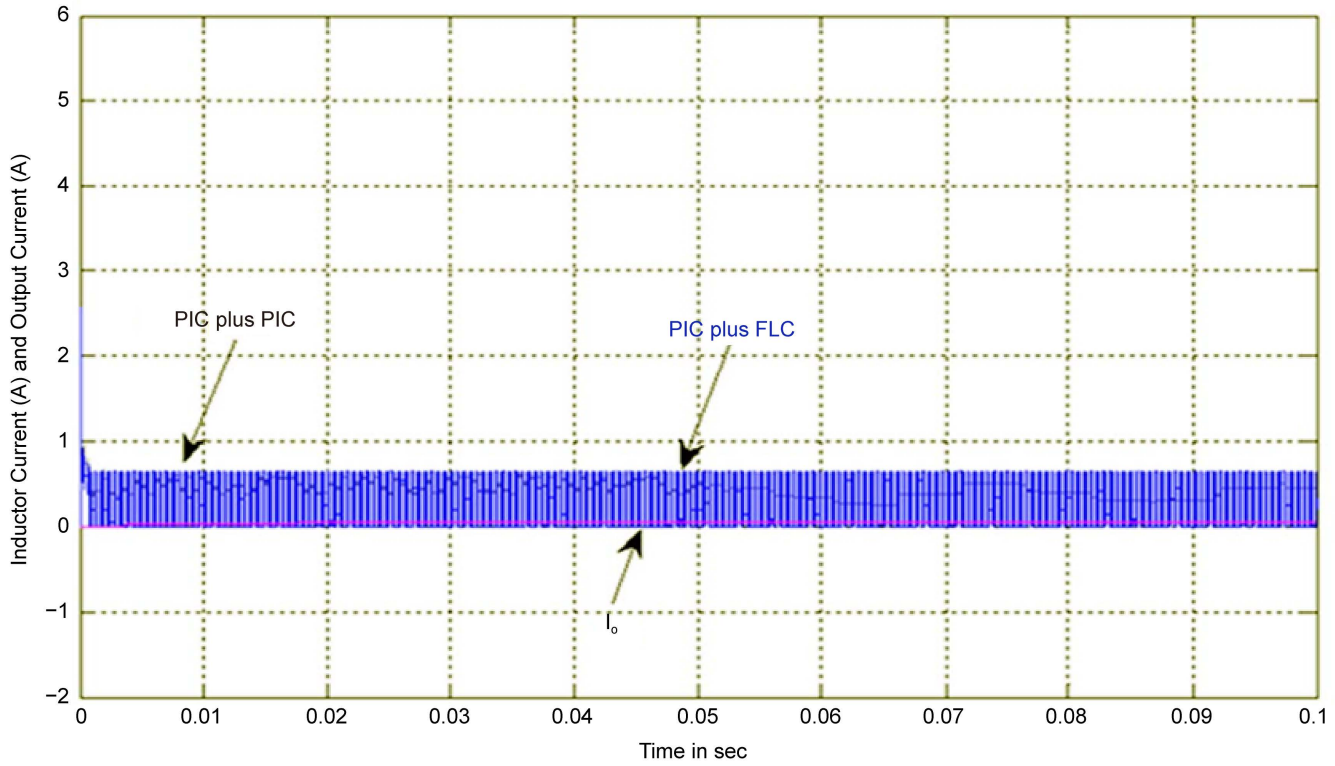
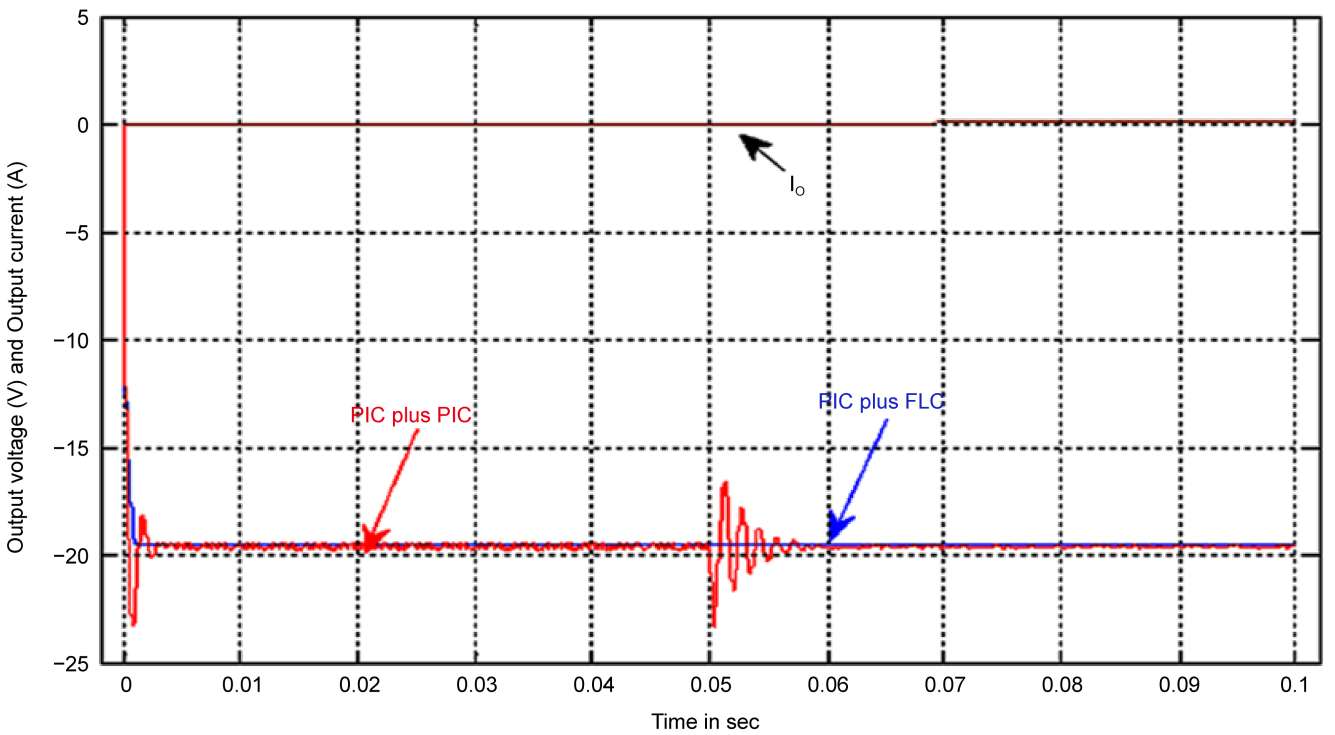
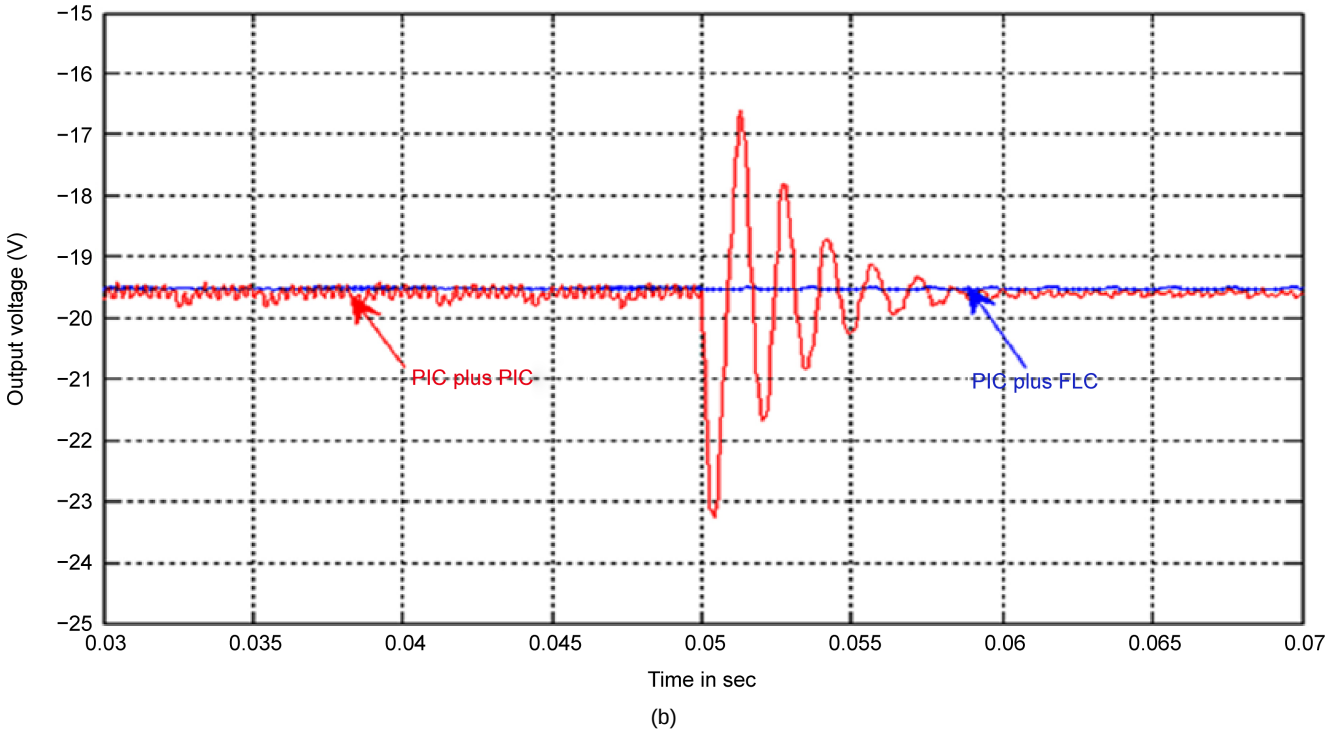
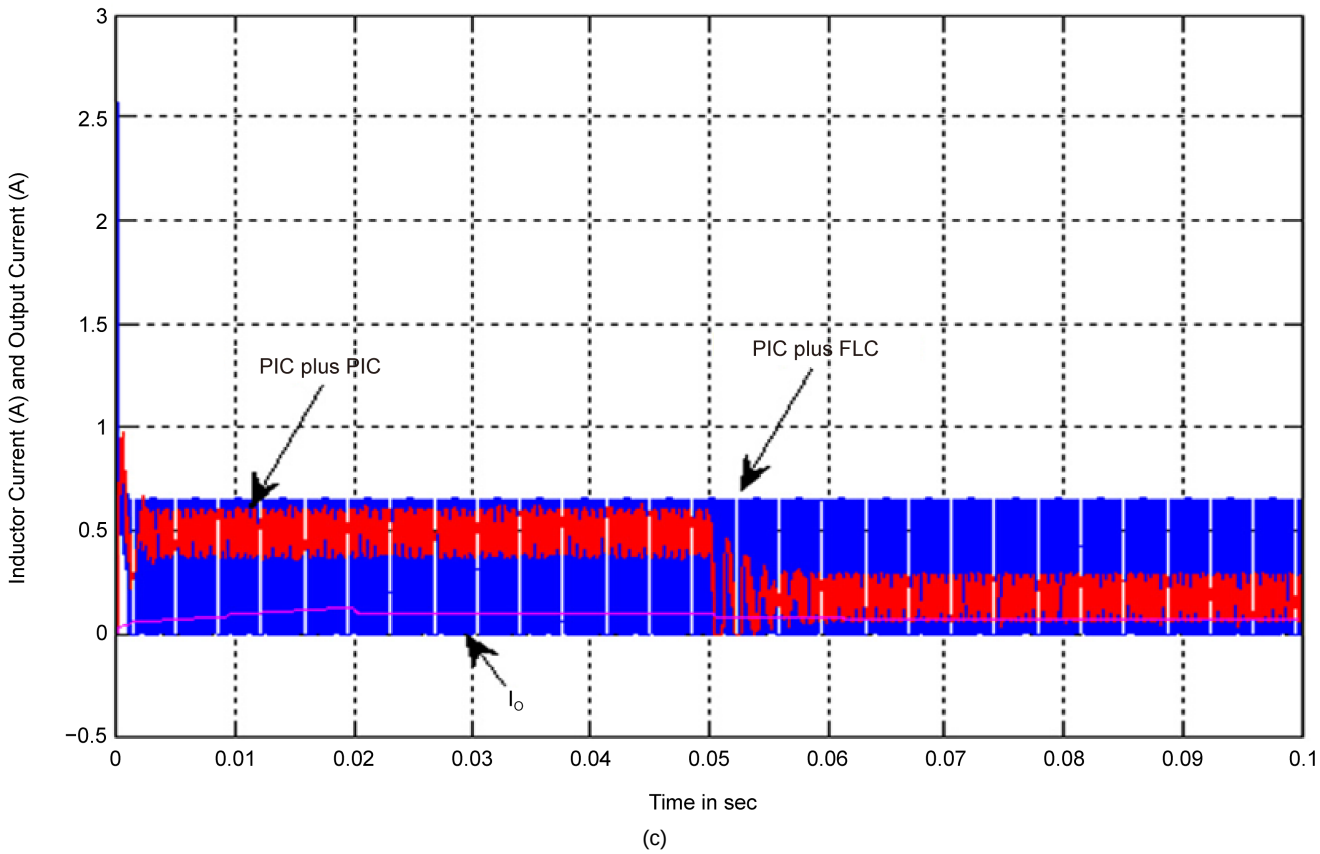


Figure 7. Response with PIC plus FLC and PIC plus PIC for load resistance change from 416.6 ohm to 316.6 ohm at time of 0.05 s with input voltage of 10 v: (a) Output voltage; (b) Zoomed view of output voltage; and (c) Inductor current.





(b)



(c)

Figure 8. Response with PIC plus FLC and PIC plus PIC for load resistance change from 416.6 ohm to 516.6 ohm at time of 0.05 s with input voltage of 10 V, (a) output voltage, (b) zoomed view of the output voltage, and (c) inductor current.

resistance change 416.6 ohm to 516.6 ohm at time of 0.05 s with input voltage of 10 V. From the Figures 8(a)-(c), it is clearly focused that the output voltage of the NOESLLC in DCM overshoots = −0.018 V, settling time of 0.0038 s, and steady state error around −0.12 V using PIC plus FLC, while the NOESLLC in DCM with PIC plus PIC has produced peak overshoots of −0.385 V and settling time of 0.12 ms during load disturbance region. Figure 8(c) indicates that the inductor current and output current of NOESLLC in DCM with controllers has produced null overshoots and settling time in load variation.

Figure 9 provides the simulated instantaneous output voltage, gate pulse and the inductor current of the NOESLLC in DCM during steady state region using a PIC plus FLC. It is evident from the figure that the output voltage ripple is very small about −0.018 V and the peak to peak inductor ripple current is 0.6 A/0.61 A for the average switching frequency of 100 kHz closer to theoretical designed value listed in Table 1 and also it indicates that to keep the inductor current for the NOESLLC discontinuous.

4.4. Circuit Components Variations

Figure 10(a) and Figure 10(b) show the simulated results of output voltage of NOESLLC in DCM using both controllers in circuit components variation (*i.e.* inductor vary from 45 μH to 90 μH and output capacitor vary from 22 μF to 32 μF). From these results, it is understood that PIC plus PIC exhibits more overshoots while the PIC plus FLC has no over shoot.

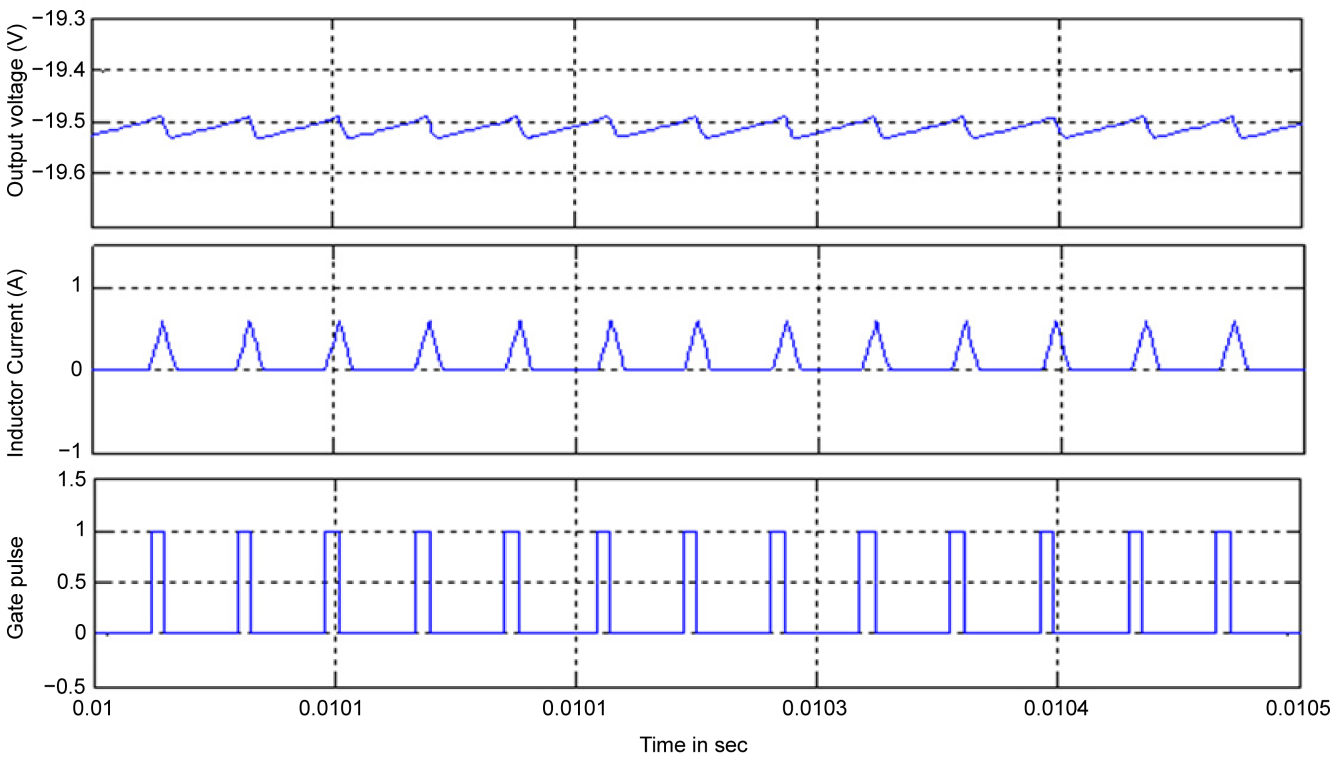


Figure 9. Simulated response of output voltage and inductor current i_{L1} in steady state condition using PIC plus FLC.

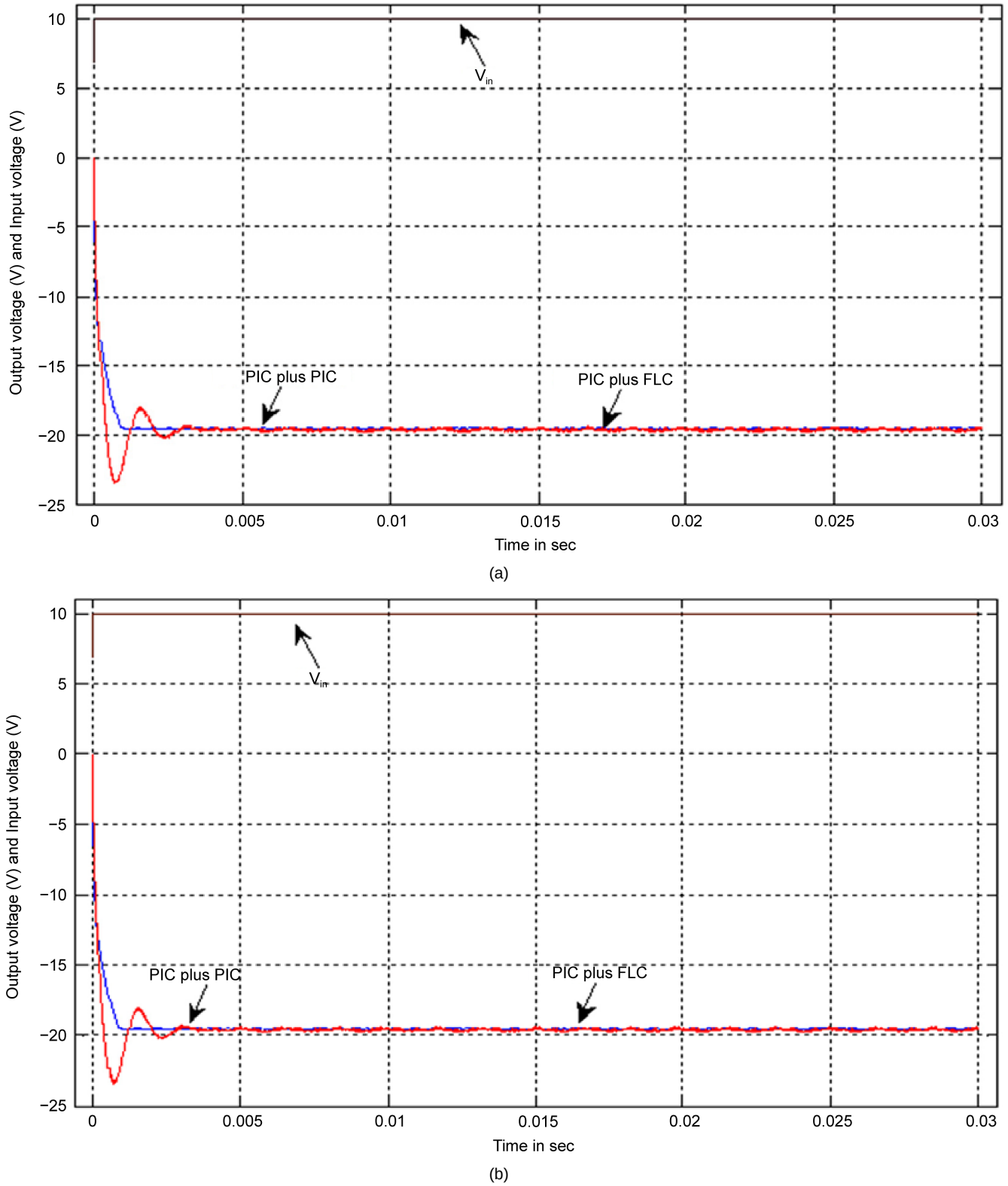


Figure 10. Circuit components variations and performance of NOESLLC in DCM: (a) Simulation output voltage when inductor variation from 45 μH to 90 μH using both controller schemes; (b) Simulation responses of output voltage when capacitor variation from 22 μF to 32 μF using both controller schemes.

Figure 11 shows the simulation results of average input current, inductor current, input voltage, output current, output voltage and efficiency of NOESLLC in DCM using PIC plus FLC. From these results, it is found that the numerical values of average input current of 0.15 A, inductor current of 0.5 A, input voltage of 10 V, output voltage of −19.6 V, average output current of −0.045 A and efficiency of 81.5% of NOESLLC in DCM using PIC plus FLC.

The time domain performance analysis of NOESLLC in DCM using both controllers is listed in Table 2. From this table, it is evident that NOESLLC in DCM using PIC plus FLC has good performance over the PIC plus PIC. Finally, the NOESLLC in DCM using PIC plus FLC has performed well in all working conditions. The membership functions for output voltage error are indicated in Figure 12. The surface view of the designed FLC is shown in Figure 13.

5. Conclusion

In this article, the analysis, design, inductor current and output voltage regulation of

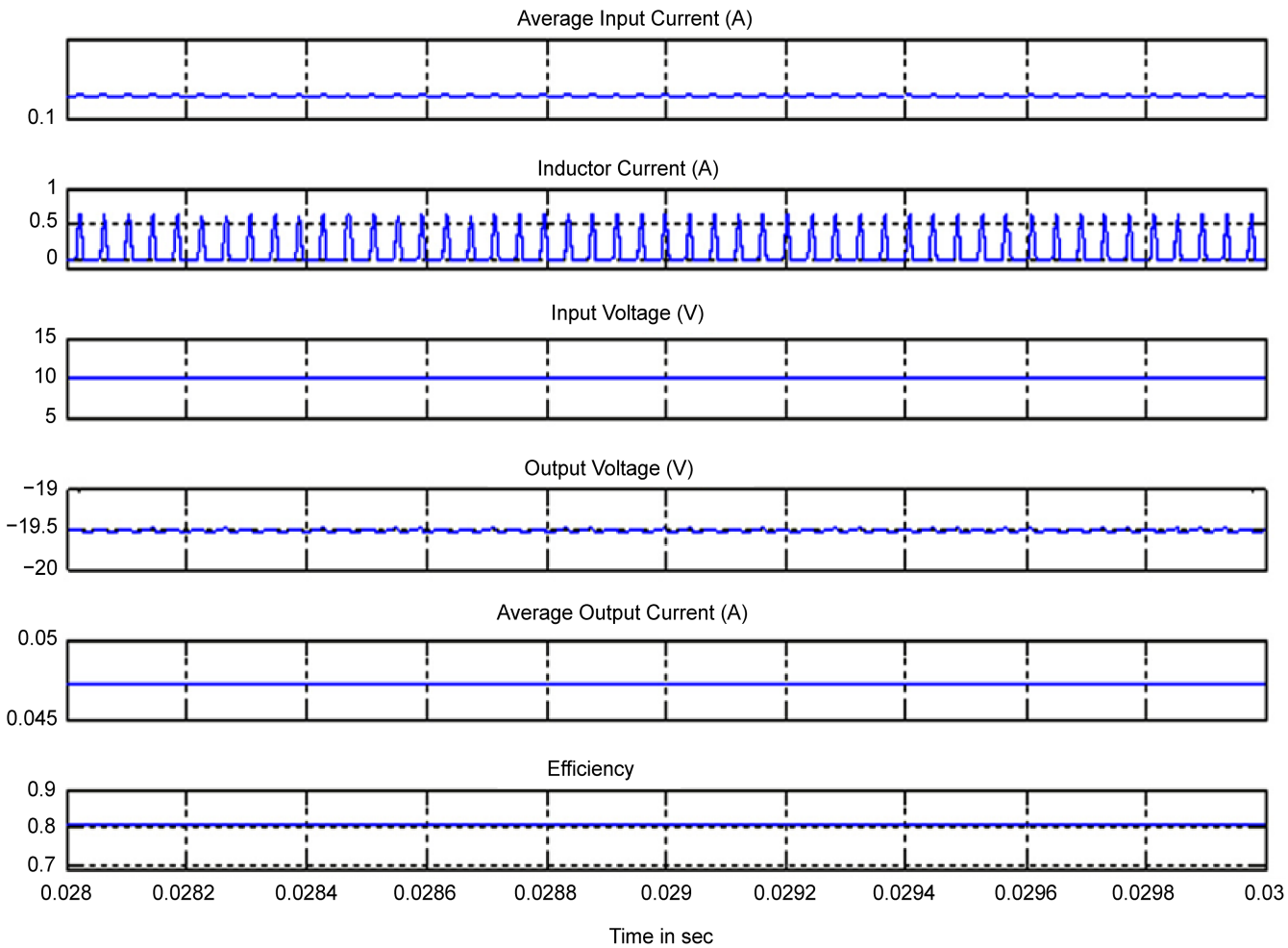


Figure 11. Performance of NOESLLC in DCM-average input current, inductor current, input voltage, output current, output voltage and efficiency.

Table 2. Performance comparison of PIC plus FLC and PIC plus PIC.

Results	Controllers	Start up Region		Line variations (10 V to 13 V and 10 V to 07 V)		Load variations (416.6 Ω to 316.6 Ω and 416.6 Ω to 516.6 Ω)	
		Maximum Overshoots (V)	Settling Time (ms)	Maximum Overshoots (V)	Settling Time (s)	Maximum Overshoots (V)	Settling Time (s)
Simulation	PIC plus FLC	−0.018	0.0035	−0.021	0.0032	−0.02	0.0034
	PIC plus PIC	−2.6	6.25 ms	−1.95	6.24 ms	−5.12	0.53 ms

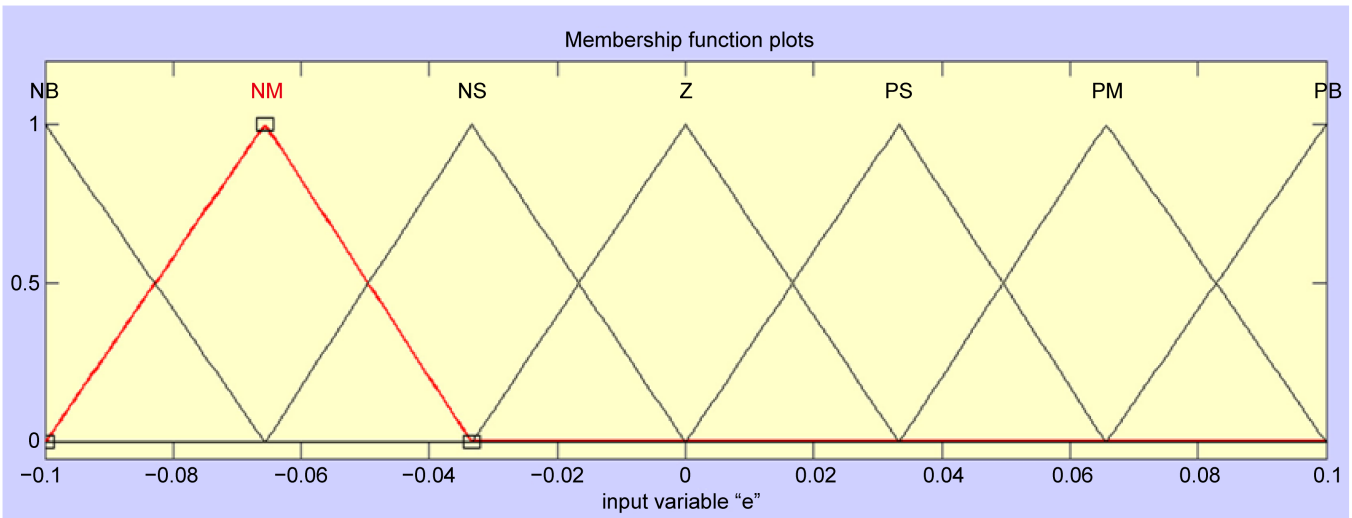


Figure 12. Membership function of error voltage.

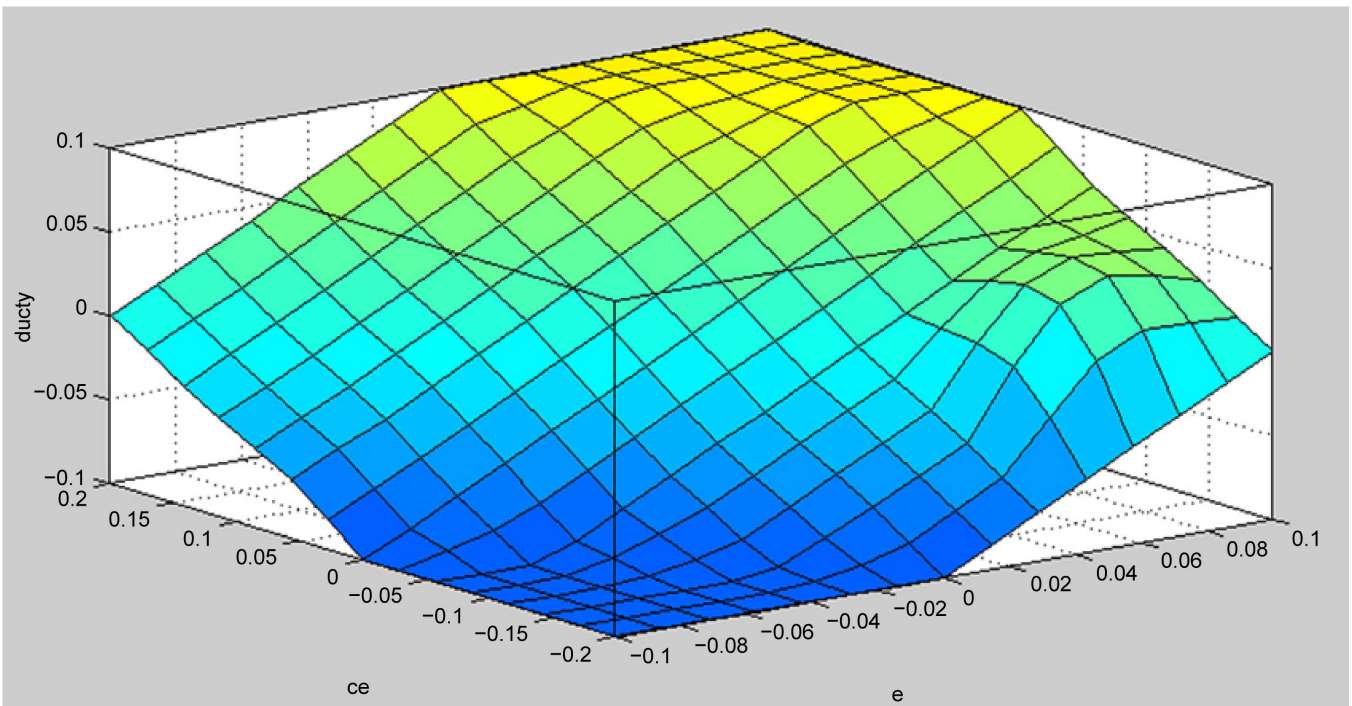


Figure 13. Surface view.

the NOESLLC operated in DCM using a variable frequency based PIC plus FLC/PIC have been successfully exhibited. The non-minimum phase behavior of the dc-dc converters results in the instable control system. In such cases the indirect regulation of the output voltage is helpful. The two-loop controller is triumph in controlling the system with improved dynamic performance. The developed PIC plus FLC regulates the output voltage of the −19.6 V NOESLLC for all possible perturbations (line, load and component variations). The merits of the designed controller are compared with PIC plus PIC using MATLAB/Simulink simulation study. There evidenced a drastic decease in peak overshoot and settling time of the start-up when PIC plus FLC is used. Similar improvement is also noticed in line and load variations.

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