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Canonic Realizations of Voltage-Controlled Floating Inductors Using CFOAs and Analog Multipliers

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Abstract

New voltage-controlled floating inductors employing CFOAs and an analog multiplier have been presented which have the attractive features of using a canonic number of passive components (only two resistors and a capacitor) and not requiring any component-matching conditions and design constraints for the intended type of inductance realization. The workability and applications of the new circuits have been demonstrated by SPICE simulation and hardware experimental results based upon AD844-type CFOAs and AD633-type/MPY534 type analog multipliers.

Keywords

Voltage Controlled Inductors, Floating Inductors, Inductance Simulation, Current Feedback Op-Amps, Analog Multipliers, Analog Circuits

1. Introduction

Voltage-controlled-resistors and a variety of other voltage-controlled impedances are useful elements in the realization of electronically-controllable filters and oscillators and have been investigated in past using a variety of active elements such as op-amps, operational transconductance amplifiers, operational mirrored amplifiers, current conveyors and current feedback op-amps, for instance, see [1]-[13] and the references cited therein.

A recent paper [14] published in this Journal has presented two configurations for realizing voltage-controlled floating inductance (VC-FI) realization using thee/four Current feedback op-amps (CFOA) along with an analog multiplier. The first circuit of [14] employs four CFOAs, three resistors, a grounded capacitor and an analog multiplier and has been shown[1] to realize lossless VC-FI providing inductance value proportional to an external control voltage V_c. On the other hand, the second circuit of [14] employs one multiplier and as many passive components as in the former circuit, but uses one less CFOA to realize a lossless VC-FI inversely proportional to V_c. The circuits proposed in [14] however, suffer from two drawbacks: (i) employment of *non-canonic* number of resistors (three) and (ii) requirement of certain conditions/constraints to realize the intended type of FIs.

The purpose of this article is to present four new circuits which, in contrast to the circuits of [14] quoted above, employ a *canonic* number of resistors (only two) and, unlike the quoted circuits of [14], do not require any component-matching/realization conditions.

2. Canonic Realizations of Lossless Voltage-Controlled Floating Inductors

The proposed circuits, which employ canonic number of only two resistors and a grounded capacitor (GC) for realizing lossless VC-FIs, are shown in **Figure 1** and **Figure 2** respectively. The proposed circuits are obtained by appropriate embedding[2] of an analog divider (as in the circuits of **Figure 1**) and analog multiplier (as in the circuits of **Figure 2**) into appropriate lossless floating inductance circuits [17] [18]. By a straight forward analysis, assuming the CFOAs to be characterized by $i_y = 0$, $v_x = v_y$, $i_z = i_x$

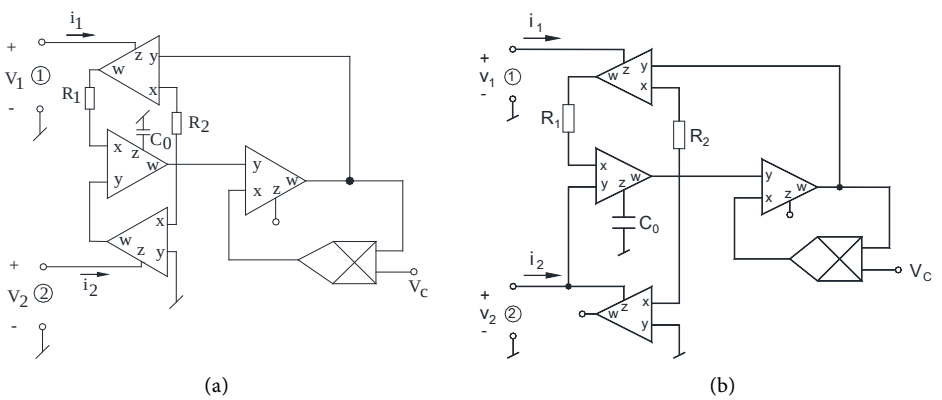


Figure 1. Proposed circuits for realizing VC-FI proportional to VC.

[1]For the correction of some discrepancies in the analysis in the quoted circuits of [14] and an anomaly in the citation of an earlier work therein, see Appendix 1.

[2]The techniques of embedding analog dividers and analog multipliers (as in the circuits of **Figure 1**, **Figure 2** and **Figure 5** here which have their origin in the earlier works of [15]-[18]) to create op-amp-AM-based voltage-controlled-resistors have been taught by the first author (RS) in the course on Linear Integrated Circuits since 1990 and these *unpublished* ideas have been adopted by and circulated amongst the academic fraternity at numerous institutions freely.

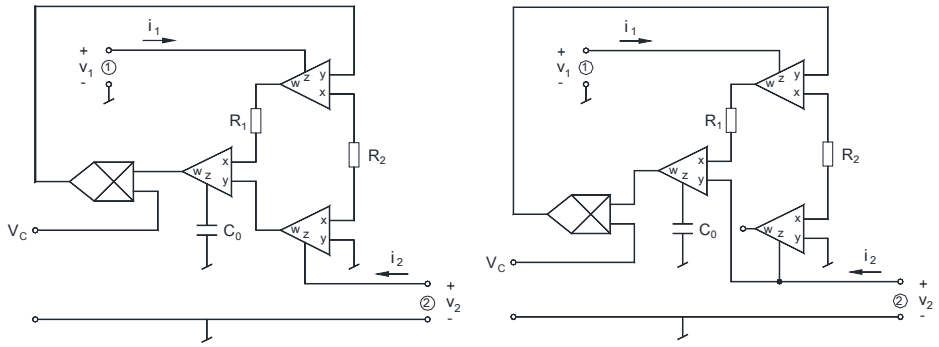


Figure 2. Proposed circuits for realizing VC-FI inversely proportional to VC.

and $v_w = v_z$, both the circuits of **Figure 1** are found to be characterized by the following short-circuit admittance matrix:

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \left(\frac{V_{ref}}{V_c}\right)\left(\frac{1}{sC_0R_1R_2}\right)\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{1}$$

Thus, the circuits realize an equivalent floating inductance $L_{eq} = C_0R_1R_2\left(V_c/V_{ref}\right)$. Note that, in contrast to the circuit of **Figure 2(a)** of [14] which requires matching of two resistors therein namely, $R_2 = R_3$ to realize the intended type of VC-FI, the circuits of **Figure 1** here do not require any design constraints/conditions to be fulfilled to realize a VC-FI.

Consider now the circuits of **Figure 2**. By straight forward analysis, these two circuits are characterized by the following equation:

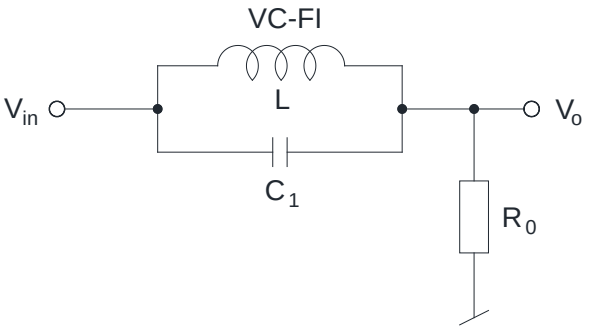
$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \left(\frac{V_c}{V_{ref}}\right)\left(\frac{1}{sC_0R_1R_2}\right)\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{2}$$

These circuits, therefore, realize an equivalent VC-FI of value $L_{eq} = C_0R_1R_2\left(V_{ref}/V_c\right)$. In this case also, it must be pointed out that while the circuit of **Figure 3(a)** of [14] requires two conditions namely $R_2 \gg R_1$ and $\left(R_1 + R_2 = R_3\right)$, no such conditions or constraints are needed in the new proposed circuits of **Figure 2**.

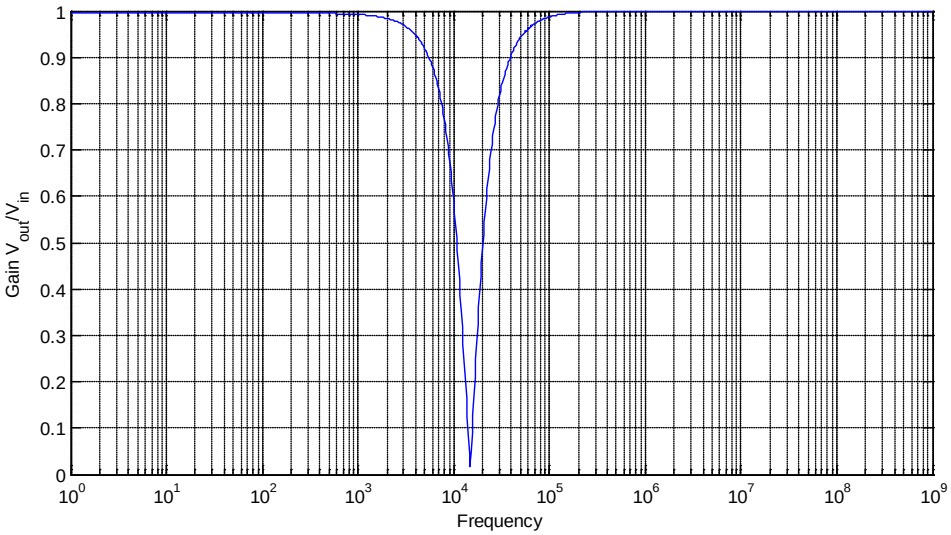
Lastly, it must also be noticed that in contrast to the circuits of **Figure 2(a)** and **Figure 3(a)** of [14] both of which require three resistors, the proposed new circuits require a bare minimum of only two resistors!

3. Applications of the Proposed VC-FIs, SPICE Simulation and Experimental Results

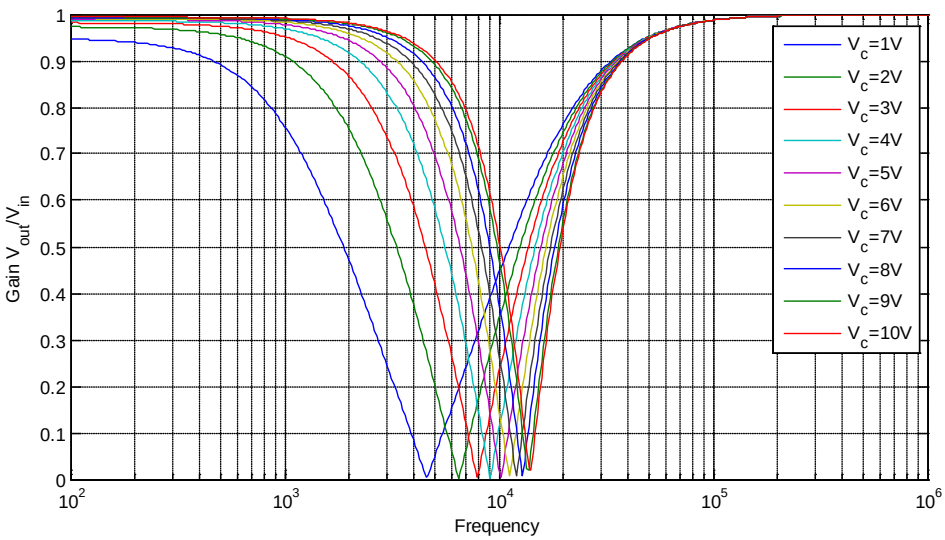
To check the workability of the proposed circuits, all the VC-FIs were tested by utilizing them in the realization of a second-order voltage-controllable notch filter as shown in **Figure 3(a)**. The frequency response of the notch filter employing the VC-FI of **Figure 1(a)** and designed to obtain a notch frequency of 15.9 kHz is shown in **Figure 3(b)**. **Figure 3(c)** shows the variability of the notch frequency with respect to the control voltage V_c for the notch filter when it was realized by using the VC-FI of **Figure 2(a)**.



(a)



(b)



(c)

Figure 3. SPICE simulation results: (a) A voltage-controllable notch filter; (b) Frequency response of the notch filter realized by using the VC-FI of **Figure 1(a)**; and (c) Variation of notch frequency with control voltage (V_c) with the notch filter realized using the VC-FI of **Figure 2(a)**.

In the simulations, AD844 type CFOAs were used which were biased with ±12 V DC power supplies. The simulation results of **Figure 3(b)** and **Figure 3(c)** are seen to be in close agreement with the theoretical results.

For verifying the practical validity of the proposed VC-FI formulations, we present here the results of the hardware implementation of a voltage-controlled band reject filter (shown in **Figure 4(a)**) wherein the VC-FI was implemented with the configuration of **Figure 2(b)**. AD844 type CFOAs biased with ±12 volts and MPY534 type analog multipliers biased with ±12 V were used along with the following component values: R_1 = 1 k Ω, R_2 = 1 k Ω, C_1 = 1.0 nF, R_0 = 680 Ω to obtain f_0 = 5.2 kHz and bandwidth = 5.58 kHz. V_c was varied from 1 to 10 volts to vary the center frequency. An exemplary frequency response for V_c = 1 volt is shown in **Figure 4(b)** whereas the variability of f_0 with respect to V_c has been shown in **Figure 4(c)**.

The SPICE simulation results of **Figure 3** and the experimental results of **Figure 4**, thus, confirm the feasibility of the proposed formulations.

4. Concluding Remarks

Four new lossless VC-FIs are introduced which employ a canonical number of passive components (namely, only one GC and two resistors) and realize the intended type of floating inductances without any conditions/design constraints. This is in contrast to the recently reported circuits of [14] for the same purposes which suffer from the drawback of employing a non-canonical number of resistors (three) and requirement of component matching/design constraint to be fulfilled.

The workability of the new circuits as VC-FIs and the variability of the inductance value through an external control voltage V_c were demonstrated by SPICE simulation results of a notch filter, as well as through experimental results of another voltage-controlled notch filter.

It is expected that the proposed new circuits may find applications in situations requiring voltage-controlled inductors.

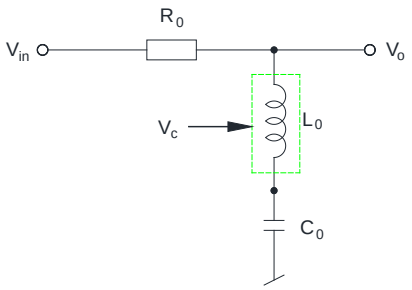
Lastly, it may be mentioned that the realization of many other grounded/floating, positive/negative and generalized linear voltage controlled impedances, based upon the ideas contained in [15]-[18] are possible; for instance, see the two configurations of **Figure 5** both of which realize VC-floating generalized impedance converters/inverters having equivalent floating impedance values given by:

$$Z_{1-2} = \left(\frac{V_{ref}}{V_c}\right)\frac{Z_1 Z_3 Z_5}{Z_2 Z_4} \tag{3}$$

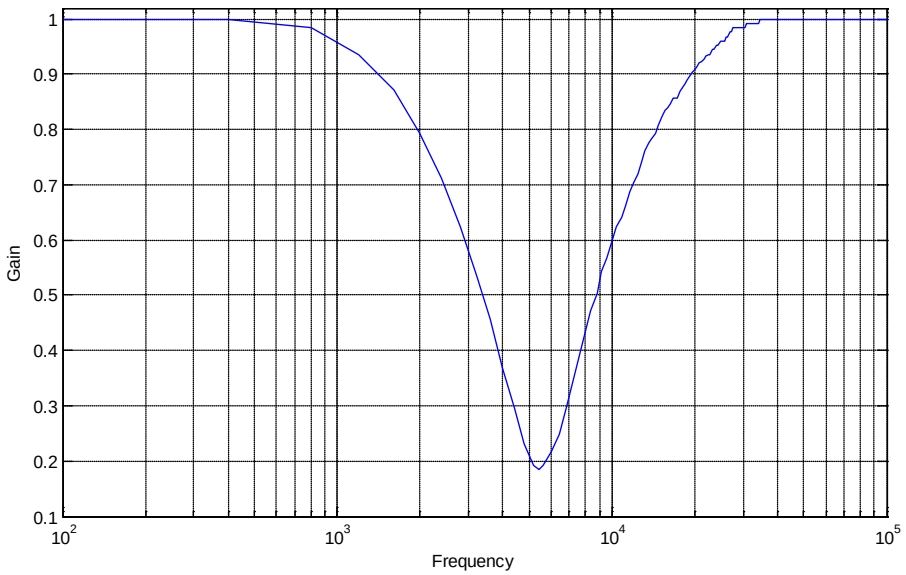
and

$$Z_{1-2} = \left(\frac{V_c}{V_{ref}}\right)\frac{Z_1 Z_3 Z_5}{Z_2 Z_4} \tag{4}$$

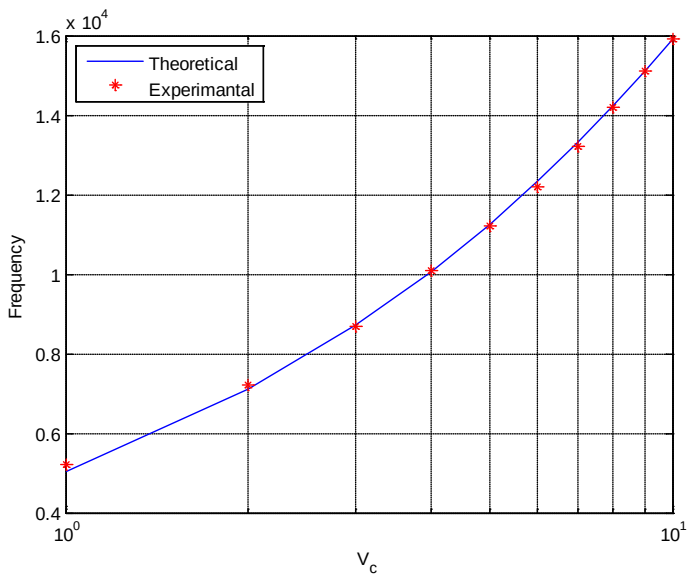
respectively. The circuits of **Figure 1** and **Figure 2** can also be generalized similarly by replacing R_1, R_2 and C_0 by impedances Z_1, Z_2 and Z_3 respectively.



(a)



(b)



(c)

Figure 4. Experimental results of (a) the band reject filter using the VC-FI of **Figure 2(b)**; (b) experimentaly measured frequency response; (c) variation of the centre frequency with the controlled voltage.

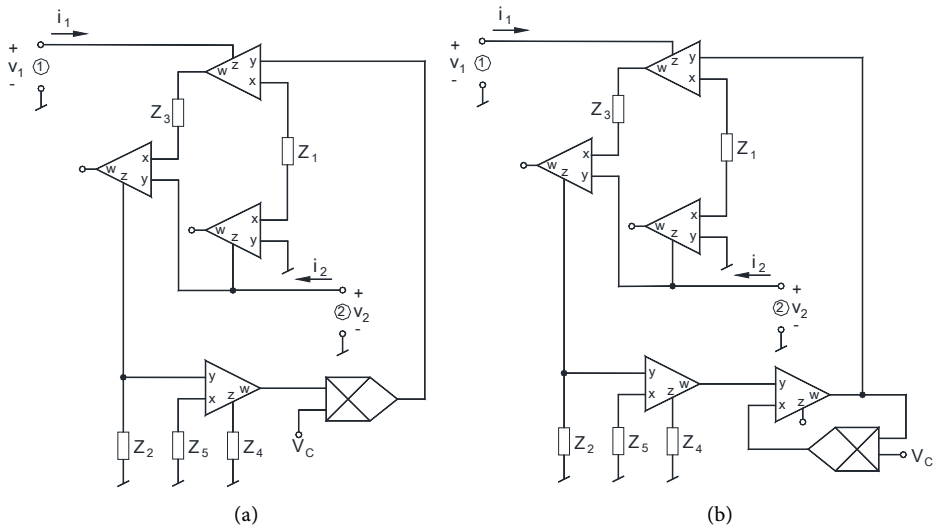


Figure 5. Two exemplary circuits realizing voltage-controlled floating generalized *impedance inverters/converters*.

Furthermore, the negative floating impedances are realizable from the configurations of **Figure 1**, **Figure 2** and **Figure 5**, by the simple artifice of interchanging some connections in the manner outlined earlier in [16] and [18], while various types of grounded positive/negative voltage controlled impedances are realizable by shorting port 2 to ground (thereby also leading to a reduced number of CFOAs in each case).

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Appendix 1: Some Appraisals

In the context of the analysis and citations of references in [14], the following are worth pointing out for the benefit of the readers of this Journal.

1) The analysis of Section 2 at pages 192-193 of [14] is clumsy. It is well-known (for instance, see [19] [20]) that a 2-port representing floating impedance Z_{eq} is correctly characterized by either the following y-matrix [19]:

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \left(\frac{1}{Z_{eq}} \right) \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$$

or *equivalently*, by the following transmission matrix [20]:

$$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} 1 & Z_{eq} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} v_2 \\ -i_2 \end{bmatrix}$$

Thus, a straight forward analysis of the circuit of **Figure 2(a)** of [14] yield its correct y-matrix as:

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \left(\frac{V_{ref}}{V_c} \right) \left(\frac{1}{sCR_1} \right) \begin{bmatrix} 1/R_2 & -1/R_2 \\ -1/R_3 & 1/R_3 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$$

Therefore, the circuit of **Figure 2(a)** of [14] will realize a lossless VC-FI subject to fulfillment of the condition $R_2 = R_3$.

On the other hand, the circuit of **Figure 3(a)** of [14] has a similar y-matrix with $L_{eq} = CR_1R_3V_{ref}/V_c$ the condition of realization being $R_1 = R_2$. Therefore, the conditions $R_2 \gg R_1$ and $(R_1 + R_2) = R_3$ as given by the authors at page 193 of [14] for their circuit of **Figure 3(a)** are unnecessary.

2) While comparing their propositions of **Figure 2(a)** and **Figure 3(a)**, the authors of [14] have cited an *unpublished work*[3] as reference 17, which is extremely surprising since this unpublished reference is not an open literature and was, therefore, definitely not available to the authors of [14]. In fact, this unpublished work[3] was quoted in the acknowledgement of reference [16] of this communication as reference 26. It is, therefore, obvious that the authors of the quoted paper [14] could have known the existence of this unpublished work (quoted as reference 17 in their paper [14]) only from the published paper [16] which curiously has not been cited by them! In view of this, reference 17 of [14] in fact, should be reference [16] of the present paper.

3) Making a Hartley oscillator using an ideal op-amp is anomalous since inductor L_1, due to being connected directly from the output of the ideal op-amp to ground, will not appear in any open loop transfer function (or loop gain) or the characteristic equation of the circuit. A resolution to this anomaly has recently been provided in [21].

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