

# Capacitor Pattern H-Bridge Multilevel Inverter (CPHMLI) Using Phase Diposition Pulse Width Modulation for Grid Applications

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## Abstract

This work presents an implementation of an innovative single phase multilevel inverter using capacitors with reduced switches. The proposed Capacitor pattern H-bridge Multilevel Inverter (CPHMLI) topology consists of a proper number of Capacitor connected with switches and power sources. The advanced switching control supplied by Pulse Width Modulation (PDPWM) to attain mixed staircase switching state. The charging and discharging mode are achieved by calculating the voltage error at the load. Furthermore, to accomplish the higher voltage levels at the output with less number of semiconductor switches and simple commutation designed using CPHMLI topology. To prove the performance and effectiveness of the proposed approach, a set of experiments performed under various load conditions using MATLAB tool.

## Keywords

Switched Capacitor Multilevel Inverter, Phase Diposition Pulse Width Modulation, Capacitor Pattern Based Multilevel Inverter, Total Harmonic Distortion, Cascaded H-Bridge, 17-Level Inverter

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## 1. Introduction

In recent years, the amount of power equipment is increasing rapidly. Nowadays, multilevel converters have

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been increasingly used in high-power medium-voltage drive applications. Multilevel Inverter (MLI) has a distinctive arrangement that allows reaching high voltage and power levels without the use of transformers. They are specially suited for applications like renewable energy systems, electric vehicles (EVs) and other innovative power electronic utilities in medium and high power applications which need low THD. There are three types of multilevel inverters: diode clamped, flying capacitors, and cascaded H-bridge multilevel inverter which are mainly based on symmetric and asymmetric value of dc power supplies. Although each topology has its own advantages, drawbacks of each topology limit their applications. Although these converters have a lot of advantages over the classic inverters, using aforementioned conventional topologies needs more number of required power switches, power supplies and large capacitor banks. Furthermore voltage of the capacitors tends to be discharged theoretically and therefore charge balancing control processing is necessary.

Cascaded Multilevel Inverters (CMLI) are formed by the series connection of two or more single-phase H-bridge inverters. The multilevel converters which gained popularity in high power applications due to their low switch leg voltage stress and modularity. CMLI introduces the idea of using separate DC sources to produce an AC voltage waveform. Each H-bridge inverter is connected to its own DC source  $V_{dc}$ . By cascading the AC outputs of each H-bridge inverter, an AC voltage waveform is produced. The proposed converters can generate staircase voltage waveform at the output with high quality and desired spectrum. The desired output voltage is synthesized by appropriate switching of several dc voltage links which leads to decrease voltage stresses on switches and total harmonic distortion than previous multilevel converters.

## 2. Previous Research

Numerous related research works are already existed in literature which based on multilevel converter of the system. Some of them are reviewed here.

The conventional types of MLI configurations using reviews are discussed. The multilevel inverters are categorized into diode clamped (DCMLI) [1], flying capacitors (FCMLI) and cascade H-bridge topologies (CHB) [2]. Many new topologies/source configurations are being proposed to serve high power applications [3]. A single-phase five-level topology for DC-AC conversion for distributed energy resources-based induction motor based grid applications. With a view to reduce power switch count, recently a new topology is introduced in [4].

Although in [5], the topology was extensively compared with the classical cascaded H-bridge (CHB) topology in terms of number of power switches, power rating of switches and switching losses, no mathematical formulations were presented. Further, a generalized structure of this topology is presented in [6] with mathematical formulations; still the treatment is restricted to symmetrical input DC sources only. It also presented comparative analysis against the CHB topology [7] based on number of power switches, number of switches conducting simultaneously and overall costs.

Nowadays, many researchers have presented numerous developed structures of MLIs with less number of key components such as number of required switches, gate drivers, power supplies and so on discussed [8]. Furthermore voltage of the capacitors tends to be discharged theoretically and therefore charge balancing control processing is necessary. The important schemes of a cascade boost switched-capacitors multilevel inverters (SCMLIs) in [9].

The duty cycle of dc bus capacitors for FCMLIs by using the existing redundancy switching states (RSSs) [10]. A triplen harmonic compensatory method [11] based on fundamental switching strategy to extend the range of modulation index for three phase utility of 7-level CHB topology.

Level phase-shift modulation approach [12] to obviate the discharging problem in a capacitor-based 7-level CHB topology supplied by one dc voltage source for main unit and one floating capacitor for auxiliary unit. The switched-capacitors multilevel inverters (SCMLIs) contain several capacitors and switches which can connect dc power supply to ac output and are able to decrease the burden of power supply to achieve higher number of voltage levels [13]. Nevertheless, to attain the greater number of output voltage levels with less number of power semiconductors and simple commutation, a new type of SCMLIs have been emerged using the series/parallel switching strategy (SCISPC) [14].

The distinctive features of these types of inverters are that they can increase the flexibility of systems by switching between several capacitors in series or parallel modes and therefore can transfer more input power to the output. A new family of cascade and hybrid SCISPC [15] topologies which have a modular structure and generate more output voltage levels with least of switches. But such structures have used the full H-bridge units with isolated dc voltage sources to change the polarity of output voltage waveform which makes more conduct-

ing loss through the current path components and increases the number of power switches.

The output voltage of a power inverter is to be a pure sinusoidal waveform with minimum distortion. But for the practical inverters, the output voltage is a series of rectangular waveforms. The major issues for the control of the power inverters are to get suitable modulation methods and to control the output rectangular waveforms to synthesize the desired waveforms. Therefore, a modulation control method is required to get a desired output voltage level and to eliminate higher order harmonics as much as possible. Hence the proposed method focussed on new cascaded H-bridge multilevel inverter topology with various modulation techniques has been discussed.

### 3. Proposed Capacitor Pattern H-Bridge Multilevel Inverter Topology (CPHMLI)

**Figure 1** shows circuit topology of the proposed Capacitor pattern H-bridge Multilevel Inverter (CPHMLI). The circuit consists of two dc power supply, two capacitor, two passive power diode and eight active power switches. Photovoltaic (PV) cells and batteries can be used as a power supply in this structure. The Charging operations for capacitor C depend on Switches and which are connected in series and parallel arrangement. As it can be inspected, when the switch becomes ON, the capacitor C is charged to and when the switch turns off, the diode becomes reverse biased and capacitor is discharged. In this mode, the power supply energy and stored energy of C are transferred to the output.

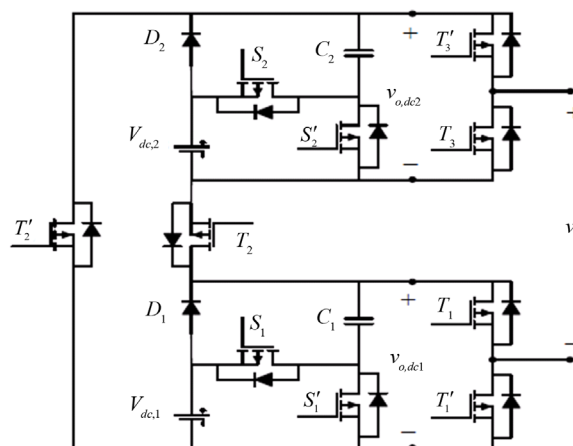
Now by considering the proposed structure (**Figure 1**) shows the number of required switches, capacitor and diodes. From this structure the switches are triggered as complementary operation with each other's and should not to be ON simultaneously. Also this structure can work on symmetric and asymmetric value of dc voltage source. In symmetric structure, all of the dc sources are equal and that are different in asymmetric topology.

The Capacitor pattern H-bridge Multilevel Inverter (CPHMLI) based modulation algorithm proposed to remove the voltage oscillation for variable phase inverter circuits. The main aim is to reduce the number of switching commutations to have total control over the voltage swings. The amplitude of the low-frequency switching voltage oscillations increases under certain nonlinear loads. So that the situation causes the system becomes unstable due to voltage variations. The proposed topology based control strategies able to control the switching voltage oscillations than previous converters and n-level diode-clamped converters.

This work belongs to contribute the following features based on advanced modulation control strategy. The proposed inverter topology ultimately controls the voltage, thus removing the low-frequency switching voltage oscillations of multiphase converters under any unbalanced and nonlinear loads. The proposed PDPWM approach eliminates the sophisticated vector diagrams analysis with many vectors when the number of phases increases. Hence, the algorithm used as a recursive method that makes it extensible to n-phase converters in future. Additionally, it adds the new features of directly controlled closed-loop algorithm that does not involve any linear controllers.

### 4. Working Methodology

The controller monitors the level of input voltage  $V_{in}$  at each duty cycle and triggers one of the switch to flow



**Figure 1.** Proposed CPHMLI-Multilevel inverter structure.

the input voltage and this makes set of capacitors to be charged with the help of diode conduction state. By reading the input voltage  $V_{in}$ , the controller estimates the switching loss and choose the optimal circuit to be triggered based on the voltage value present in the capacitors present in the selected circuit. The controller maintains number of possible circuits as patterns and for each of the pattern the controller computes the possible output voltage  $V_{out}$ . Based on the output voltage could be generated a single switch is selected and the circuit is triggered to conduct the voltage and produce efficient output voltage.

In this work, the number of required capacitors in each of proposed CPHMLI units is optimized from the view point of maximum produced output voltage levels for proposed CPHMLI with minimum number of IGBTs. This optimization is done based on asymmetric value of dc sources according to Equation (1). In general, the number of output voltage levels for proposed CPHMLI is obtained by:

$$N_{level} = (N_{levelsub})^m \quad (1)$$

where  $N$  Sublevels is the number of output voltage levels for proposed CPHMLI which is calculated by Equation (2). Then equation of (1) can be rewritten as:

$$N_{level} = (2^{n+2} + 2^{2n+1} + 1)^m \quad (2)$$

On the other hand, the relation of in terms of (number of required IGBTs for proposed CSMLI) and is equalized to Equation (2):  $N_{IGBT}$  and  $m$  as

$$m = \frac{N_{IGBT}}{N_{IGBTsub}} \quad (3)$$

Also with inserting Equation (1) into Equation (3) and Equation (2):

$$N_{level} = (2^{n+2} + 2^{2n+1} + 1)^{\frac{N_{IGBT}}{(6n+4)}} \quad (4)$$

In order to obtain the optimal number of capacitor from each of CPHMLIs, the variation of against for specific number of  $N_{IGBT}$ .

**Table 1** shows the possible operating modes based on charging and discharging states for both capacitors about 17 states. The charging states for both capacitors (states number of 5, 6, 8, 10, 12 and 13) and discharging states for one capacitor and charging states for another one or vice versa (other remaining states). In this **Table 1**, C and D refer to charging and discharging modes for capacitors, respectively. In order to generate more number of output voltage levels with optimum number of components, all of the capacitors should be charged by binary asymmetrical algorithm, according to this table. Also from this table it is obvious that, proposed topology is able to generate different positive output voltage levels by self-balancing ability.

In this case, all of the switches are driven by fundamental switching frequency whereas the sinusoidal reference voltage is compared with some available dc voltage levels and create the related gate switching pulses. The most advantage of this switching method is referred to low switching frequency which yields to reduction of switching loss. Details of fundamental switching modulation strategy are not objective of this paper.

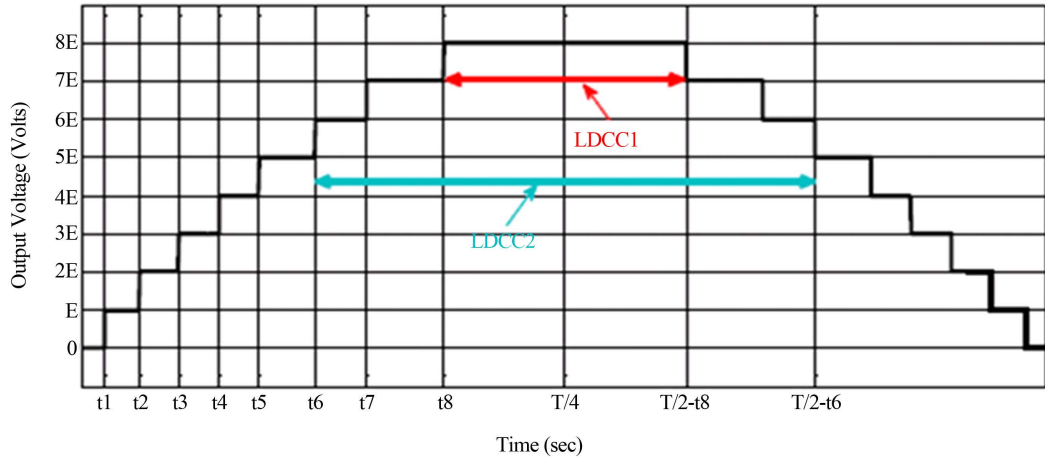
In addition from **Table 1**, it is clear that, to generate each of output voltage levels, only five switches are being involved in the current path. At this stage, to determine the capacitance of and, two assumptions are considered which one is related to output sinusoidal load current with phase difference between output voltage and current and the other is contribute to same duration in each step of staircase output voltage.

Thus, the maximum discharging amount of each capacitor can be defined as Equation (5) in one half cycles:

$$Q_{Ci} = \int_{t_f}^T \frac{1}{4} I_{out} \sin(2\pi f_s t - \phi) dt \quad i = 1, 2 \quad (5)$$

where,  $T$  is the period of one cycle,  $f_s$  is the frequency of output voltage and  $I$  is the amplitude of load current, respectively. On the other hand, in proposed 17-level inverter, this time interval varies for  $T_s$  based on longest discharging cycle (LDC) of each capacitors. According to **Table 1** the switching pulses are illustrated by **Figure 2**.

Thus, with considering the as maximum allowable voltage ripple, the optimum value of capacitors by



**Figure 2.** Output voltage waveform of 17-level inverter positive half cycle.

**Table 1.** Switching operation for CPHMLI topology.

Switching states	ON Switches	$V_0$	$C_1$	$C_2$
1	$T'_1, T_2, T'_3, S_1, S_2$	$4V_{dc} + V_{c,1} + V_{c,2}$	D	D
2	$T'_1, T_2, T'_3, S'_1, S_2$	$4V_{dc} + V_{c,2}$	C	D
3	$T_1, T_2, T'_3, S'_1, S_2$	$3V_{dc} + V_{c,2}$	C	D
4	$T'_1, T_2, T'_3, S_1, S'_2$	$4V_{dc} + V_{c,1}$	D	C
5	$T'_1, T_2, T'_3, S'_1, S'_2$	$4V_{dc}$	C	C
6	$T_1, T_2, T'_3, S'_1, S'_2$	$3V_{dc}$	C	C
7	$T'_1, T_2, T_3, S_1, S'_2$	$V_{dc} + V_{c,1}$	D	C
8	$T'_1, T_2, T_3, S'_1, S'_2$	$V_{dc}$	C	C
9	$T_1, T_2, T_3, S'_1, S'_2$	0	C	C
10	$T'_1, T'_2, T'_3, S'_1, S'_2$	$-V_{dc}$	C	C
11	$T_1, T'_2, T'_3, S_1, S'_2$	$-V_{dc} - V_{c,1}$	D	C
12	$T'_1, T'_2, T'_3, S'_1, S'_2$	$-3V_{dc}$	C	C
13	$T_1, T'_2, T'_3, S'_1, S'_2$	$-4V_{dc}$	C	C
14	$T_1, T'_2, T_3, S_1, S'_2$	$-4V_{dc} - V_{c,1}$	D	C
15	$T'_1, T'_2, T_3, S'_1, S_2$	$-3V_{dc} - V_{c,2}$	C	D
16	$T_1, T'_2, T_3, S'_1, S_2$	$-4V_{dc} - V_{c,2}$	C	D
17	$T_1, T'_2, T_3, S_1, S_2$	$-4V_{dc} - V_{c,1} - V_{c,2}$	D	D

$$C_{opt,i} \geq \frac{Q_{Ci}}{kV_{in}} \quad (i = 1, 2) \quad (6)$$

### 5. Capacitor Pattern Based Pulse Generation

The proper duty cycle selected using capacitor pattern based pulse triggering for the proposed inverter topology. The pattern is generated based on the duty cycle according to the switch being triggered, the method identifies set of patterns which are triggered to get charged and set of capacitors gets discharged. The pattern generator

identifies the capacitors at each pattern which gets charged at the specific selection of switch and their new voltage value will be updated to the pattern set.

*Pseudo Code:*

*Input: capacitor Pattern Set Cs, pulse Pattern Ps.*

*Output: Step output voltage*

*Begin*

*Identify the Switch being selected.*

*Compute possible capacitors gets charged  $cs = \sum \text{Capacitor}(Cs) \Delta \text{Voltage}$*

*for each capacitor Ci from CS*

*compute possible step up voltage value  $Sv = \text{Voltage}(Ci) + Vin$*

*for each pattern Pi of PS*

*if  $Pi \in Ci$  then*

*$Pi(Ci) = Sv.$*

*end*

*end*

*End.*

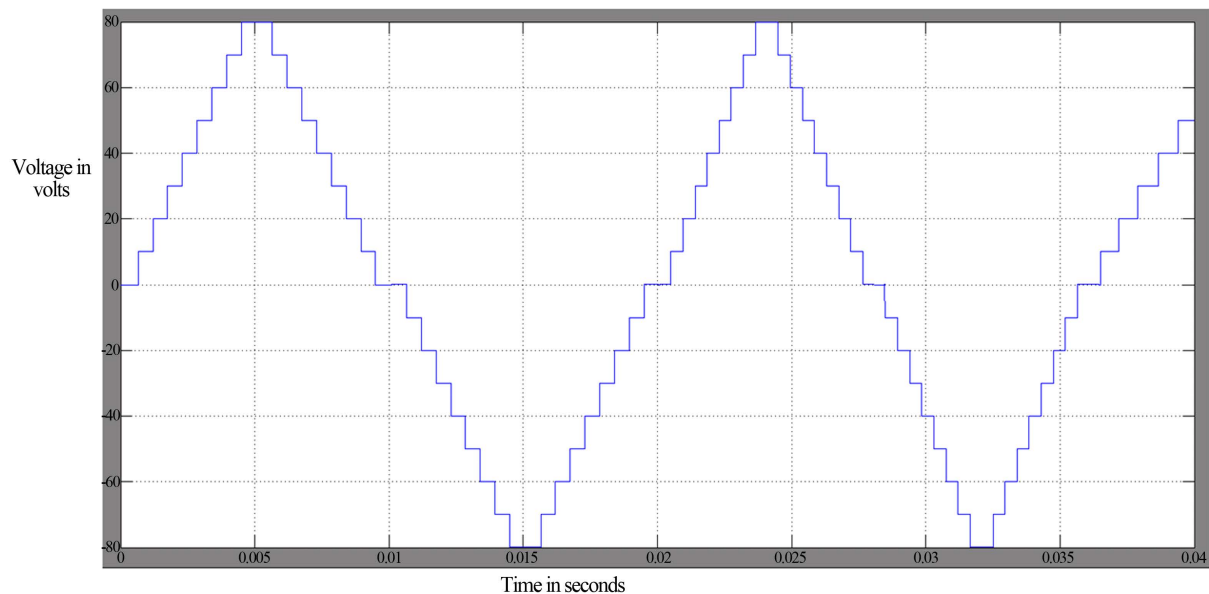
*End.*

## 6. Results and Discussion

The proposed capacitor pattern based hybrid multilevel inverter has been implemented and simulated using Matlab. The THD and efficiency of the proposed CPHMLI has been evaluated with number of duty cycles and has produced efficient Staircase output voltage.

**Figure 3** shows the waveform generated using the mat lab simulation for output voltage, and it shows clearly that the output voltage has 17 level step output values. The graph has been generated by connecting the supply voltage with the CPHMLI circuit where the supply voltage is generated from renewable energy and stored in a battery.

**Figure 4** shows the wave form of switching pulses for few step level which shows the various duty cycle of the proposed model. The graph has been generated by varying the duty cycle for each pattern of capacitor. The switches are connected in a H-bridge manner to get the proposer staircase AC output voltage. At the same time, The Diode and capacitance are connected parallel to the circuit which provides efficient output with increased voltage.



**Figure 3.** Simulation results for Proposed CPHMLI inverter for 17 level.

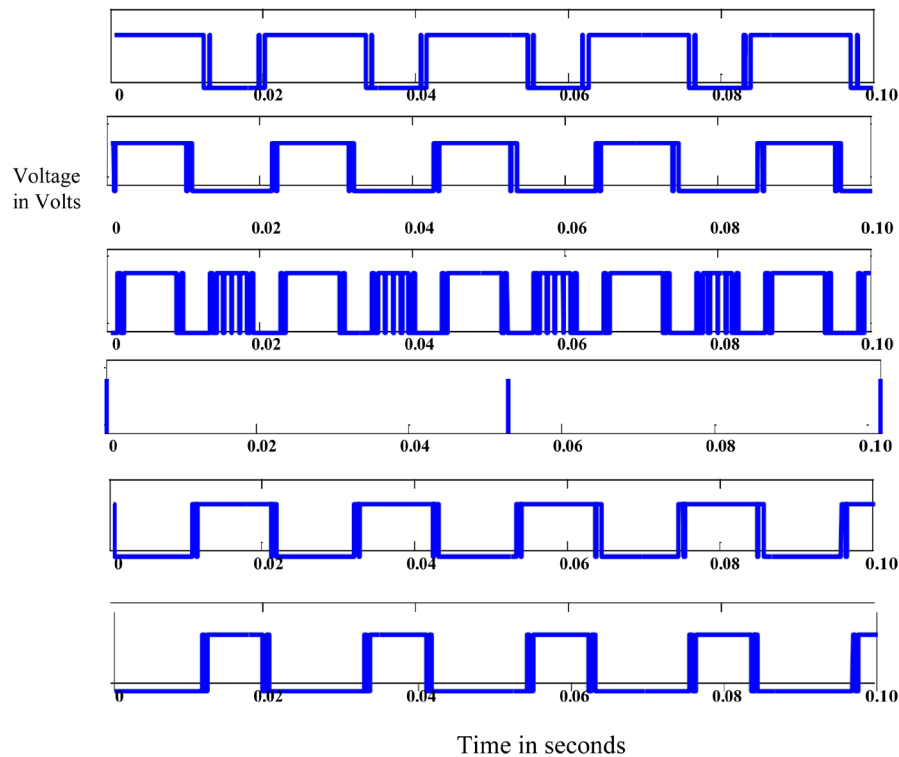


Figure 4. Switching pulses of the 17-level inverter using PDPWM scheme.

### Topology Comparison

Table 2 shows the required component comparison between Cascaded multilevel inverter, cascaded H-bridge multilevel inverter and proposed CPHMLI topology. The proposed topology requires very less number of IGBT switches, Diodes, capacitors and dc input voltage than the other methods. Therefore the proposed CPHMLI topology consists of ten switches, two diodes, two input dc voltage source and two capacitors to achieve 17 level step output voltage.

From the simulink environment FFT analyzer evaluates the different THD for various values of modulation Index  $m_a$ . These evaluated values for different modulation techniques are listed in Table 3. From The measured values PDPWM produces very low harmonic distortion of 12.05% with respect to the modulation index of 1 for seventeen level step output voltages. Hence the proposed topology provides the low harmonics and higher efficiency for medium voltage high power applications. Table 3 shows the output line voltage THD obtained for the different level inverters at various values of  $m_a$  for the three techniques.

From Graph 1, it is clear that the proposed CPHMLI inverter has Less Total harmonic distortion for various modulation index values such as  $M = 1, 0.8, 0.6, 0.4$  than the others proposed earlier.

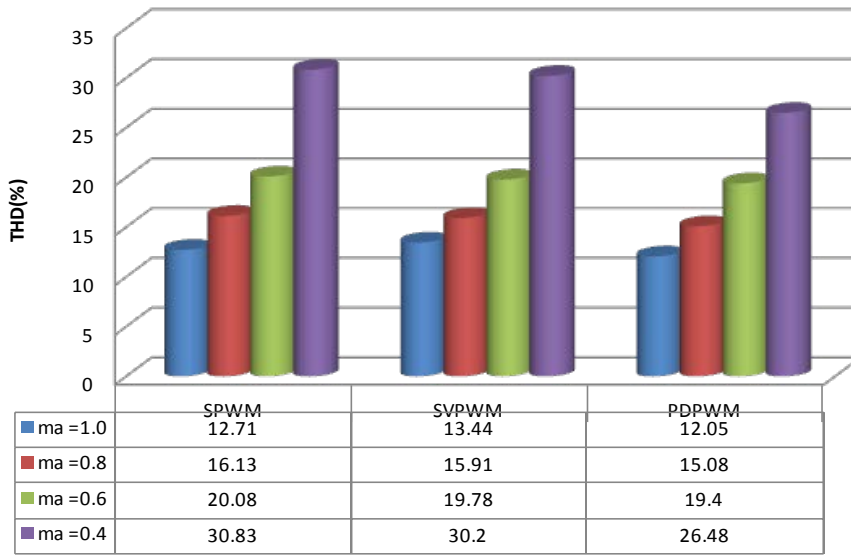
Table 4 shows the comparison of different multilevel inverter with proposed multilevel inverter using proposed controller system. The efficiency of the proposed model has been evaluated and tabulated.

Graph 2 shows that the proposed method has more efficiency compare to other two methodologies for 17-level cascaded H-bridge multilevel inverter topology and the same input values. Hence the proposed topology provides the low harmonics of 8.5% and higher efficiency of 95% for medium voltage high power applications.

### 7. Conclusion

This work proposed a novel schematic design and circuit for Capacitor pattern H-bridge Multilevel Inverter (CPHMLI) topology to reduce the distortions in output voltage. The proposed capacitor pattern based H-bridge Multilevel Inverter topology design in photovoltaic system was simulated with MATLAB/SIMULINK software. The proposed model reduces the required components and harmonic losses with the help of maintaining various

### Performance Comparisons



Graph 1. Performance comparison of THD for various Modulation index.

Table 2. Number of used Components between different inverter topology.

Sl. No.	Parameters	MLI	CASCADED H-BRIDGE MLI (CHMLI)	CAPACITOR PATTERN BASED CASCADED H-BRIDGE MLI(CPHMLI)
1	$N_{IGBT}$	12	12	10
2	$N_{diode}$	2	2	2
3	$N_{Capacitor} = N_{dc}$	2	2	2
4	$V_{block}$	$20V_{dc}$	$24V_{dc}$	$20V_{dc}$
5	$N_{Currentpath,max}$	6	6	5

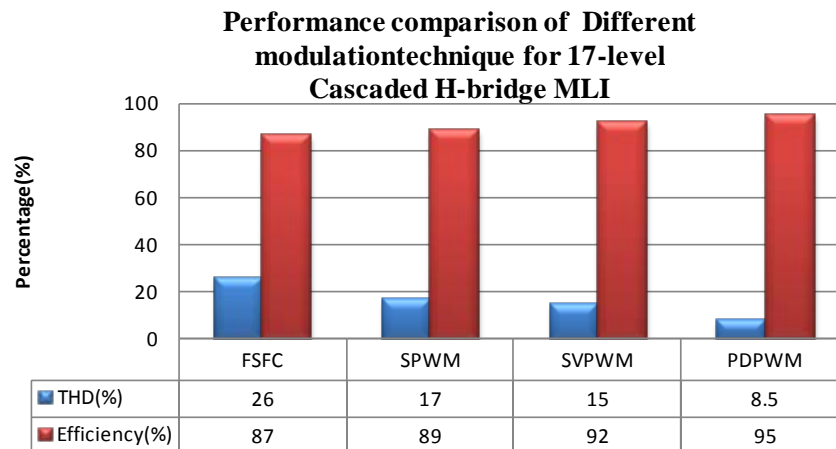
Table 3. Comparison of Modulation techniques (THD & Modulation index ma).

Step Level	Modulation Techniques used	THD (%)			
		$m_a = 1.0$	$m_a = 0.8$	$m_a = 0.6$	$m_a = 0.4$
17	SPWM	12.71	16.13	20.08	30.83
17	SVPWM	13.44	15.91	19.78	30.2
17	Capacitor Pattern based Phase Diposition PWM (PDPWM)	12.05	15.08	19.4	26.48

Table 4. Performance of various modulation technique based Inverter.

Sl. No.	Step Level	Modulation Techniques used	THD (%)	Output Power Efficiency (%)
1	17	Fundamental switching frequency control (FSFC)	26	87
2	17	SPWM	17	89
3	17	SVPWM	15	92
4	17	Capacitor Pattern based Phase Diposition PWM (PDPWM)	8.5	95





**Graph 2.** Comparison of different CHMLI system.

capacitor patterns which are discharged and list of capacitors which are gets charged at each duty cycle and at each switch condition. At each duty cycle the controller identifies the capacitors being charged and discharged according to the switch conditions. Also, the controller performs voltage approximation to identify the output voltage for each pattern. The proposed design reduces the voltage oscillations by adapting the capacitor as auxiliary circuit. The proposed schematic is hard wired to evaluate the performance and has produced efficient results. The proposed design has produced very good results and the output voltage and current produced are high. The efficiency produced by the design has been evaluated as 95% with low THD of 8.5% which is a successful output. The proposed design could be further improved by adapting more strategic voltage control algorithms and designs.

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