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Design and Analysing the Various Parameters of CMOS Circuit's under Bi-Triggering Method Using Cadence Tools

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Abstract

Reducing the power and energy required by the device/circuit to operate is the main aim of this paper. Here the new design is implemented to reduce the power consumption of the device using the triggering pulses. The proposed triggering method uses a complementary MOS transistor (pMOS and nMOS) as a voltage divider and ground leakage suppressor (*i.e.*); these designs are named as Trig01 and Trig10 designs. In Trig01 design the pair of CMOS is placed in the voltage divider part; similarly in Trig10 design the pair of CMOS is placed at the ground leakage suppressor part. Standard CMOS gates like NOT, NAND, NOR, EX-OR etc. are designed with these technologies and these gates are designed with 180 nm technology file in the cadence tool suite; compared to the normal CMOS gates, the Bi-Trig gate contains 4 inputs and 2 outputs. The two extra inputs are used as Bi-Trig control signaling inputs. There are 2 control inputs and thus $2^2 = 4$ combination of controlling is done (*i.e.*); both pMOS and nMOS are ON, both pMOS and nMOS are OFF, pMOS ON and nMOS OFF and pMOS ON and nMOS ON. Depending on the usage of the circuit, the mode of operation is switched to any one of the combination. If the output of the circuit is not used anywhere in the total block, that specified circuit can be switched into idle mode by means of switched OFF both the pMOS and nMOS transistor in the control unit. This reduces the leakage current and also the power wastage of the circuits in the total block. Bi-Trig controlled circuit reduces the power consumption and leakage power of the circuit without affecting a performance of the circuits.

Keywords

Bi-Triggering, Power Analysis, Energy Analysis, Circuit Simulation, Delay Analysis, Sub Clock Method

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1. Introduction

Leakage power occurs due to the error voltage in the transistor during the ideal mode. This leads to increase of the power consumption and also the energy, and to reduction of the power wastage and consumption. The proposed method is used. To obtain the correct result with reduced power consumption the Bi-Trig is used.

In previous method *i.e.*., Dual Mode logic [1], the operation is determined as dynamic and static function. The performance of the circuit is high only in dynamic mode; it is proved in the paper [1]. Thus similarly the paper [2] tells about the low-power dynamic operation method, in which the width of the transistor is tuned, and it reduces the overall power. This gives the result of about 25% of power consumption reduction.

The main drawback of the paper [2] is that the circuit does not have a driving load capacity and thus it is overcome by using the nanometer technology as given in the paper [3]. To overcome the drawback of the sub-threshold DML [1]-[4], this proposed system is designed with two new methodologies.

Trig01: pMOS and nMOS are connected at the voltage side of the standard CMOS circuit.

Trig10: pMOS and nMOS are connected at the ground leakage suppressor side of the standard CMOS circuit.

pMOS and nMOS are used as a Bi-Trig Control circuit to drive the entire circuit by means of voltage divider method. In design-1 the control circuit is connected at the voltage divider side of the circuit to control the entire circuit by separating the given supply voltage (VDD). Similarly in the second design methodology the Bi-Trig Control circuit is placed at the ground leakage suppressor side in order to reduce the leakage current through the circuit to ground terminal.

2. Proposed System

The design developed to reduce the leakage power in CMOS circuit during the active mode of operation. By activating the CMOS transistor there will be a direct connection between the VDD and ground will happen at the 0.7 voltage switching [5]. This causes a shot link to ground leakage current will more at the time of switching [6]. In order to reduce the leakage current the Bi-Trig method is implemented. There are two design method is implemented in order to rectify the problems. Bi mode is used to reduce the ideal current and full mode operation is used to drive the large capacitance load without using the cascading inverter units.

2.1. Trig01

In this schematic methodology the control signal is located at the voltage divider side of the CMOS circuit. By this process the operating voltage which is given to the circuit is divided into two parts by using the nMOS and pMOS transistor. These transistors are connected in with two separate inputs as shown in the **Figure 1**. Thus the input is given directly to the CMOS circuit and the output is forwarded directly from the circuit. For half mode power output is control by the Bi-Trig control circuit. (*i.e.*) Either pMOS is ON or nMOS is switched ON. pMOS is switched ON and OFF using the trig pulse as 0 and 1. Similarly the nMOS is switched ON and OFF by using the control signal as 1 and 0. For a full mode operation in order to drive the full mode the control circuitry is switched ON fully mode *i.e.*, pMOS and nMOS both are in closed loop. Thus the full power is given to the CMOS circuit.

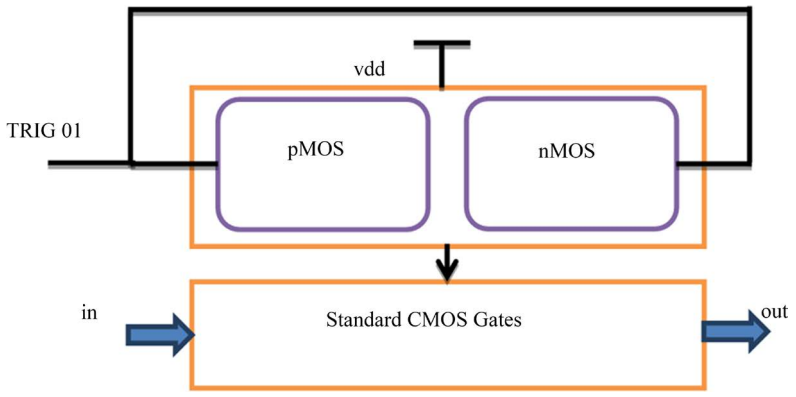

Figure 1. Design Trig01 block diagram.

2.2. Trig10

In this schematic methodology the control circuit is placed at the ground leakage suppressor side of the CMOS circuit. By this technique the error current due to the short circuit between the VDD and GND is reduced by using the nMOS and pMOS transistor. These transistors are connected in with two separate inputs as shown in the **Figure 2**. Thus the input is given straight to the proposed circuit and the output is drive directly from the circuit.

For half mode power output is control by the Bi-Trig control circuit. (*i.e.*,) Either pMOS is ON or nMOS is switched ON. pMOS is switched ON and OFF using the trigger pulse as 0 and 1. Similarly the nMOS is switched ON and OFF by the trigger pulse as 1 and 0. For a full power operation to drive the large load the trigger circuitry is switched ON fully mode *i.e.*, pMOS and nMOS both are in closed loop. Thus the full power is given to the CMOS circuit.

3. Implementation of the Design in Basic CMOS Gates

The testing of a CMOS gates and circuits is done by using the Cadence-Virtuoso tool under the GPDK 180 nm technology and the finger width of the transistor is fixed at 2 µm similarly the finger width is also 2 µm ranges.

3.1. NOT Gate

Trig01 is implemented in the NOT gate transistor level model. This circuit diagram explains how the design is implemented in the standard CMOS gate. By using the trigger pulse to pMOS and nMOS the operation is verified. The output is drive directly from the transistors. Operating voltage is given to the circuit is divided into a two parts by nMOS and pMOS transistor and given to the drive unit.

So that depending on the BTC signal the operating power is changed, when pMOS is triggered ON and due to the pull up logic the maximum voltage is applied to the circuit and it is operates in the maximum power mode. Implementation of TRIG 01 and TRIG10 in NOT gate as shown in **Figure 3** and **Figure 4** it contains the two different designs which is based on the BTC unit, voltage divide and the leakage current suppressor.

Design 2: similar to the design 1 technology the BTC is placed in the ground leakage suppressor side of the circuit. This is used to block the short circuit between the operating voltage and GND, thus it reduce the leakage current of the circuit. Four type of triggering is done by pMOS alone ON, nMOS alone ON, both pMOS and nMOS ON or both OFF. For a full power operation to switch the large load the control circuitry is switched ON fully mode *i.e.*, pMOS and nMOS both are in closed circuit. Thus the full power is given to the CMOS circuit.

3.2. EX-OR Gate

Trig01 is implemented in the EX-OR gate transistor level model.

As shown in the **Figure 5** and **Figure 6** the EX-OR gate is controlled by the Bi-Trig control circuit at the voltage divider side of the circuit. The triggering voltage given to the circuit is control by the trigger signal given to the CMOS gate. Similarly these designs are implemented in all gates and also in different CMOS circuits and the power is calculated using the Cadence tool. The average power is measured by using the tranpow in the browser window similarly the total power consumption is done by using the cadence—average (get data). By this the overall power is tabulated and checked.

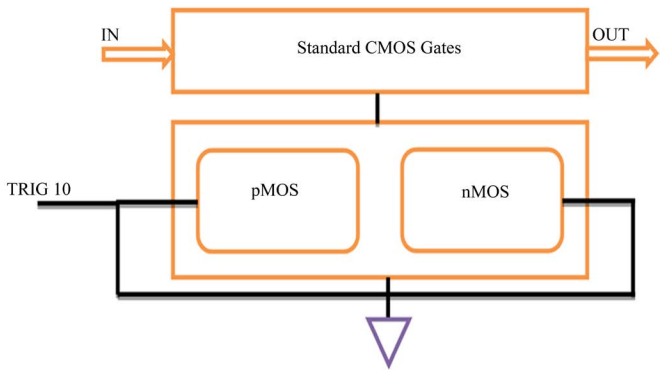

Figure 2. Trig10 block diagram.

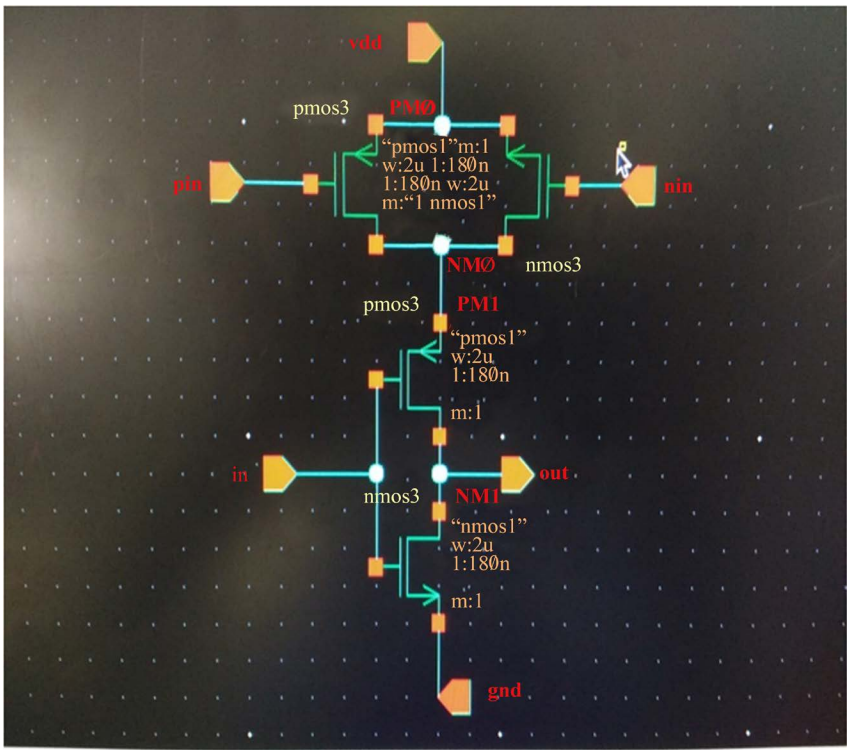

Figure 3. NOT gate with Trig01.

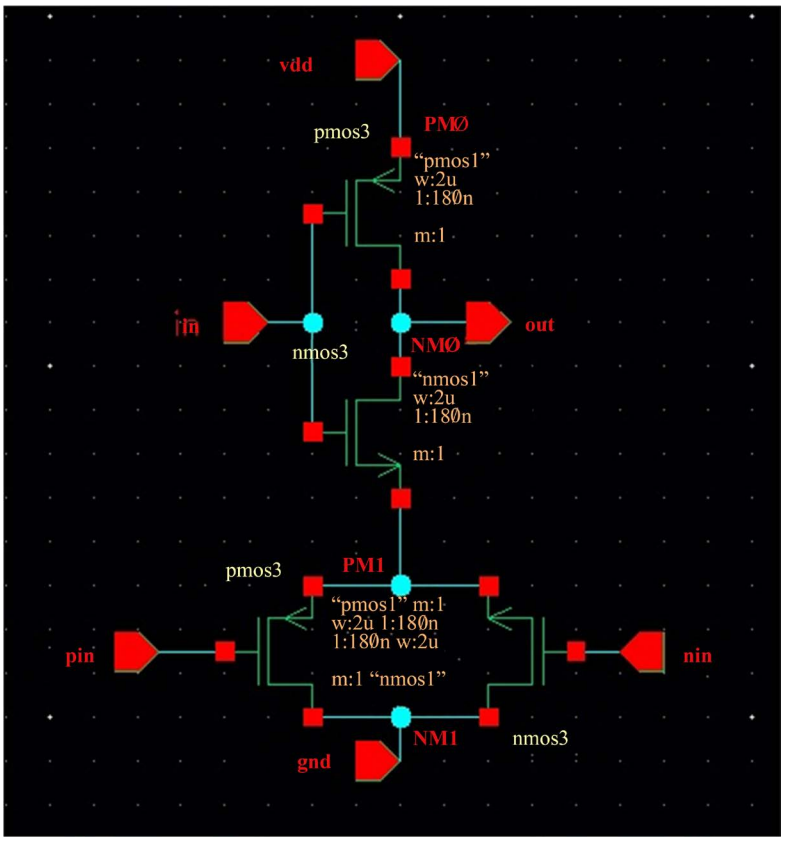

Figure 4. NOT gate with Trig10.

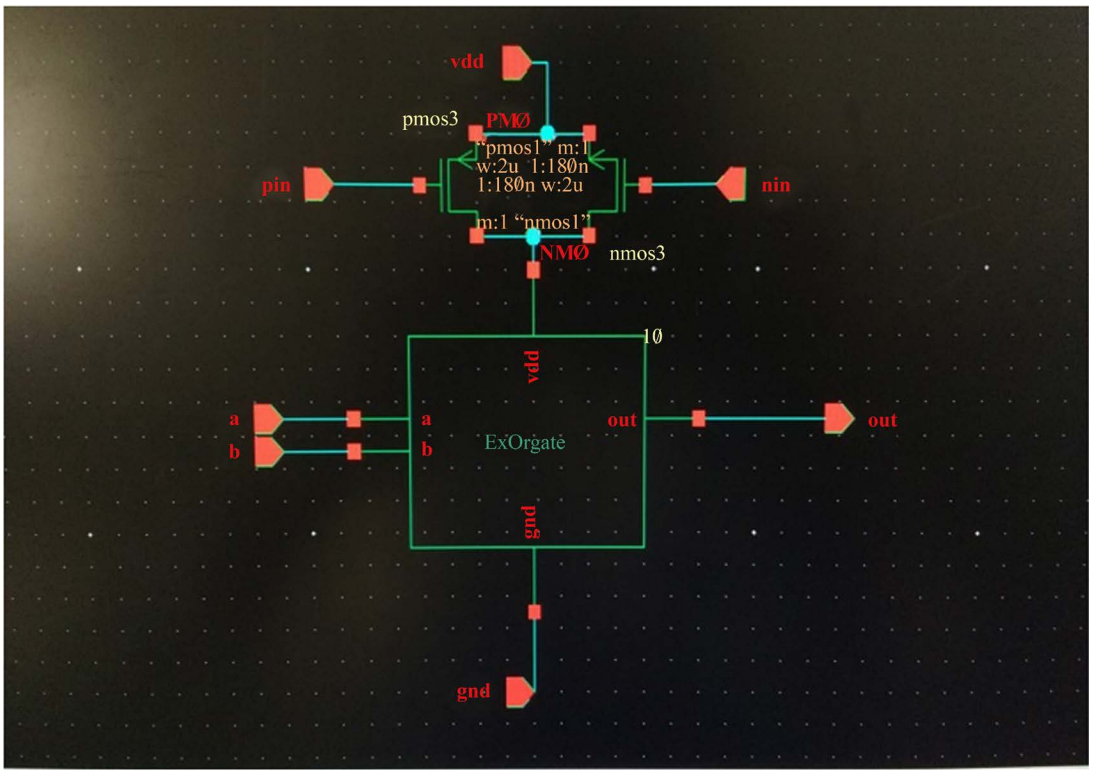

Figure 5. EX-OR gate with Trig01.

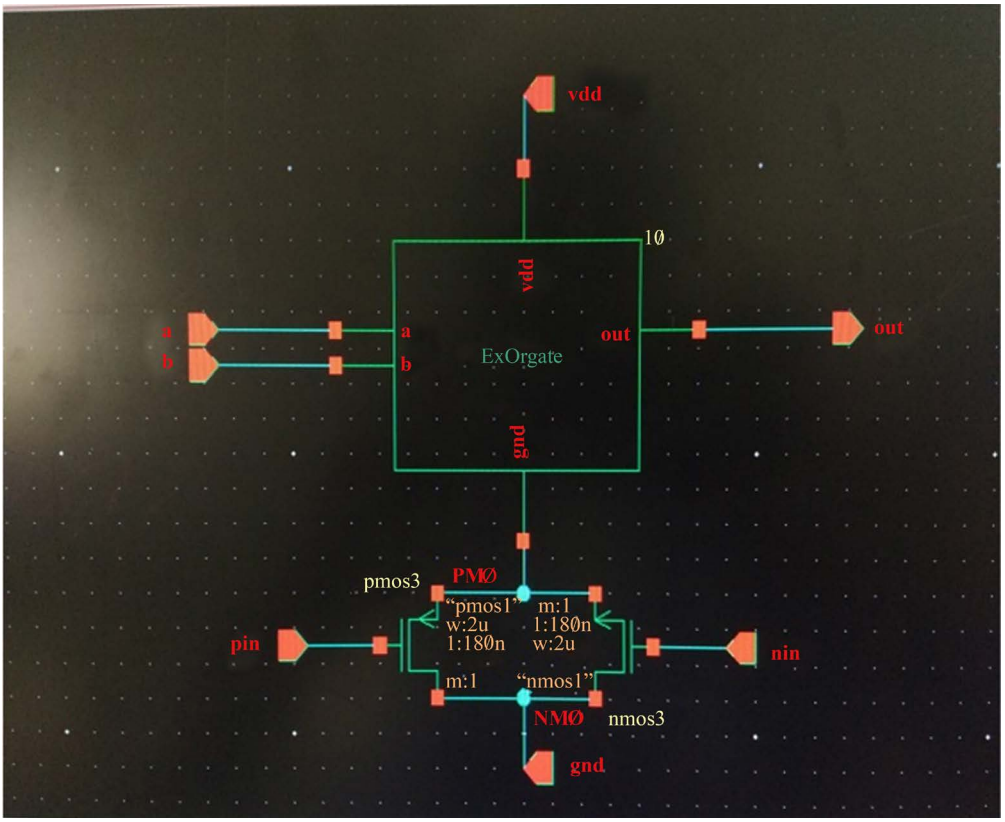

Figure 6. EX-OR gate with Trig10.

4. Power Outputs of CMOS Gates

The CMOS gates are designed using the BTC method and the power is calculated using the cadence-virtuoso tools calculator unit. The average power consumed by the gates under BTC is tabulated and shown in the **Table 1**. The power consumption will be in the range of micro wattage, BTC reduces the power wastage and also the error or noise current flow in the circuit.

5. Implementation of the Design in CMOS Circuits Gates

To implementing the BTC circuits the CMOS gates which is designed earlier is used with the same Trig01 and Trig10 technique. Thus the power consumption of the circuit is determined by using the group of gates work with the predefined techniques. Designing a BTC circuit the basic gates which is designed with the BTC unit is used to analyze the performance (*i.e.*,) power consumption of the BTC based CMOS circuit.

5.1. Full Adder Design Using BTC

Full adder contain a 3 in pins (ex: a, b, cin) and 2 out pins (ex:sum, carry). By using the BTC other two inputs are used (ex: pin, nin) as shown in **Figure 7** and **Figure 8**. Here the full adder is designed with the two EX-OR gates and three AND gate and also with two numbers of the OR gate which is designed in BTC technique.

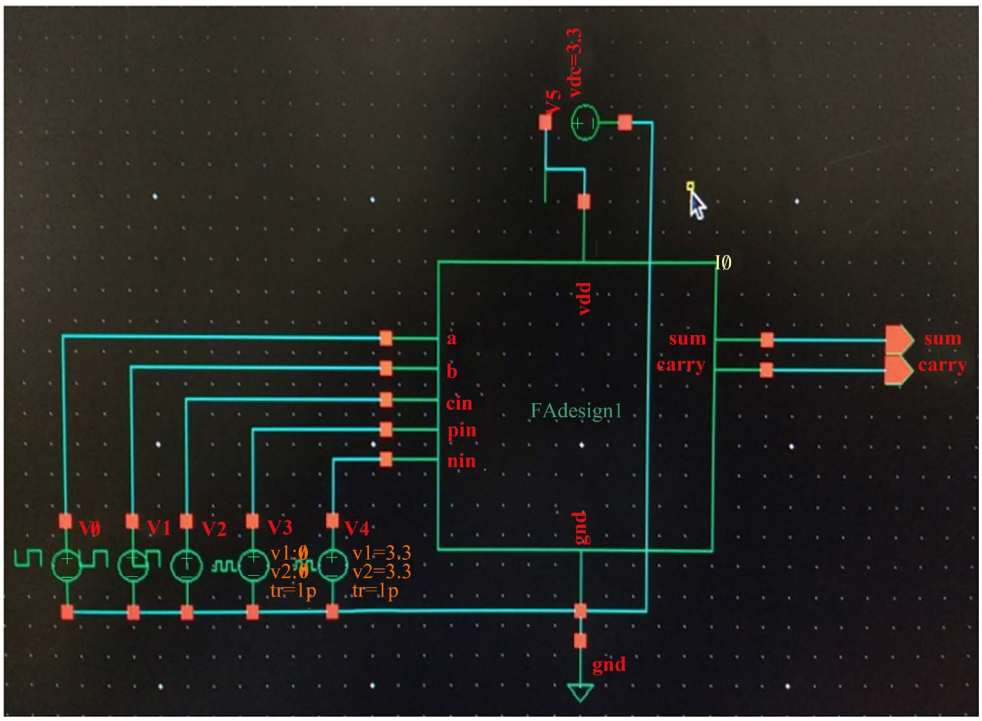

Figure 7. Full adder with BTC Trig01 gates.

Table 1. Power analysis of CMOS gates under Bi-Triggering method.

S. NO	CMOS gates	Design 1: Power in micro watts	Design 2: Power in micro watts
1	NOT gate	1332	130.82
2	EX-OR gate	107.13	156.92
3	AND gate	118.92	145.7
4	OR gate	87	134.4
5	NOR gate	76.72	96.99
6	NAND gate	111.32	141.7

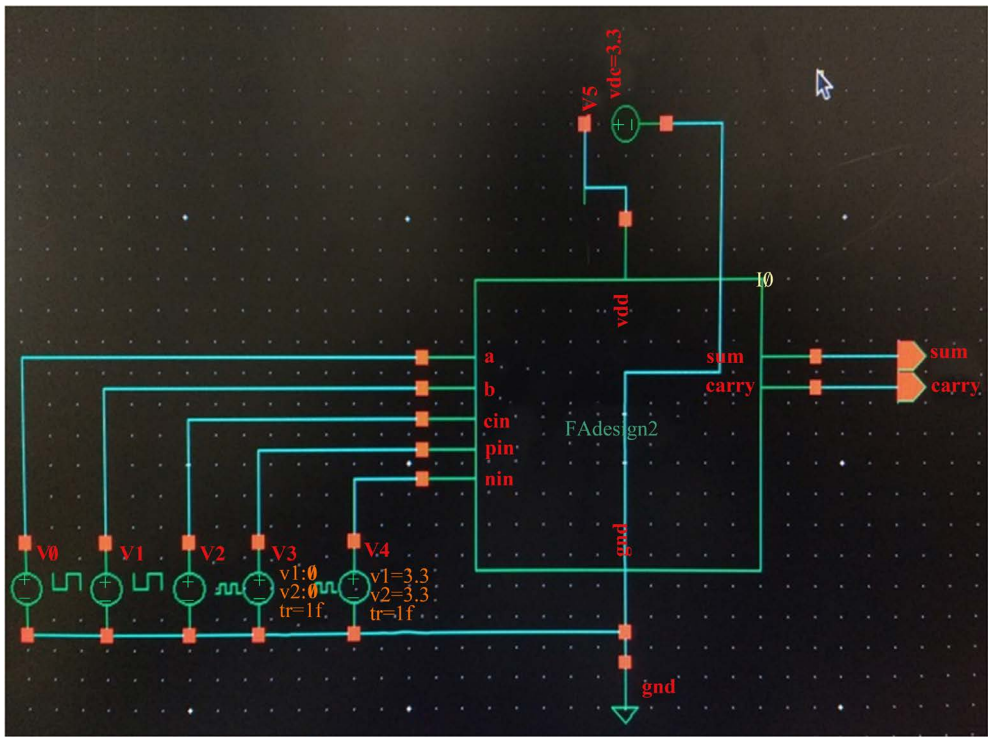

Figure 8. Full adder with BTC Trig10 gates.

The full adder designed in the papers [7]-[13] are depend only on the sizing of the transistor, reducing the finger width of the transistor due to this the circuit consume less power, even the power reduction is done due to the low width the circuit is not used in the complex design. To avoid these drawbacks the BTC is used in the two type of methodology as shown **Figure 7** and **Figure 8**. In the paper [14] [15] the transistor operated in near threshold region thus it causes an error in the output signal to drive the next or large load.

5.2. Carry Look Ahead Adder Design Using BTC

Here the CLAA is designed using the BTC design 2 gates as shown in the **Figure 9**. The BTC of all the gates are combined in a single lined and input is switched as same. Depending on the switching the operating power is changed. Trig01 and Trig10 of this circuit is used to reduce the power consumption during ideal and operation mode.

1) Ripple Carry Adder design using BTC

RCA is designed with Full adder which is designed earlier using the Trig01 and Trig10 gates, here the cells are designed by using the BTC gates and implemented with either design 1 or design 2 logic as shown in **Figure 10**.

This is a 4 bit RCA unit developed using the Trig01 method. Instead of having an eight number of input It Contain the ten numbers of inputs including the BTC pins. As shown in **Figure 10** and **Figure 11** gives the detail pin of RCA.

6. Parameters Comparison

In the proposed system the CMOS circuit are designed and the some parameters are analyzed it is shown in the tables. **Table 2** provides the power analysis, **Table 3** provides the energy consumption of the circuits, **Table 4** provides the delay analysis.

7. Conclusion

Thus the CMOS gates are designed using the design-1 and design-2 approach under Sub-Clocking method. These gates are used as building blocks for the development of the Sub-Clock CMOS circuits in order to reduce

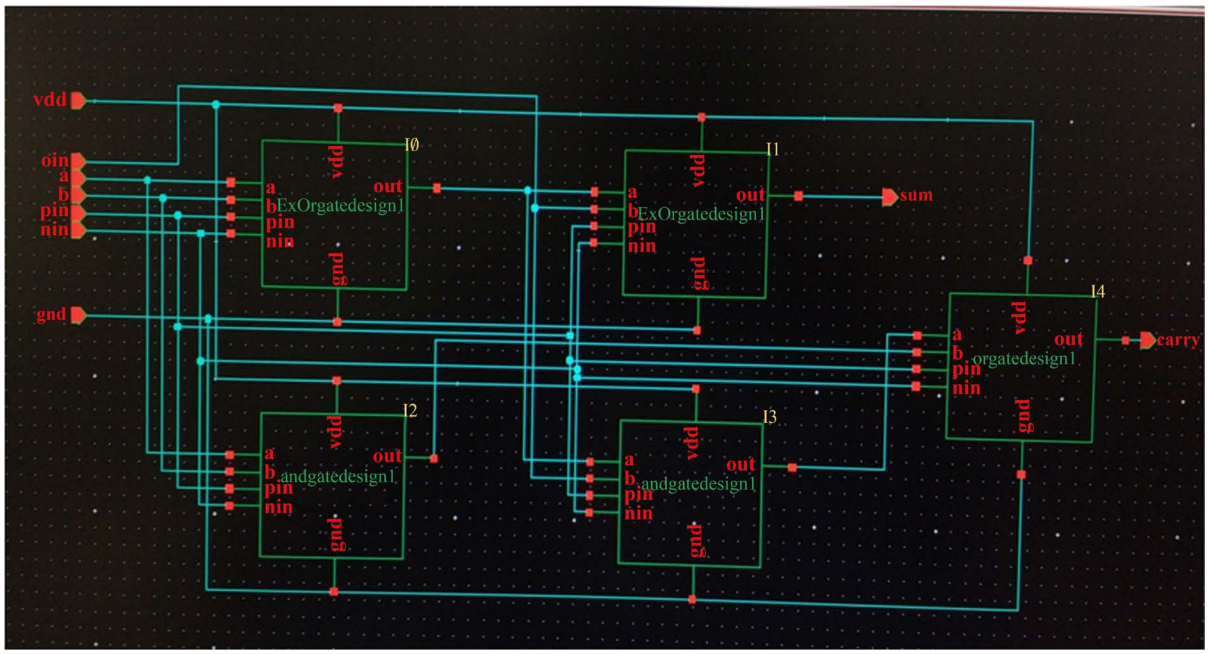

Figure 9. CLAA with BTC Trig01 gates.

Table 2. Power analysis of CMOS gates and various CMOS circuits. This comparison **Table 1** gives a detail about the power consumed by the device in previous method and the proposed method. As a result nearly 50% power consumption is reduced then existing one.

S. NO	CMOS Circuit	Existing Design power in µ watts	Proposed Design-1 Power in µ watts	Proposed Design-2 power in µ watts
1	NOT Gate	28.84	15.31	13.46
2	AND Gate	12.44	6.45	6.21
3	OR Gate	17.21	9.310	9.11
4	NAND Gate	10.59	5.630	5.22
5	NOR Gate	10.43	6.151	6.03
6	EX-OR Gate	34.50	18.34	18.40
7	Full Adder	1215	79.81	78.56
8	Carry Look Ahead Adder	915.30	66.79	67.69
9	Ripple Carry Adder	375.00	247.40	176.1
10	Carry Select Adder	19950	13170	10650
11	D Flip Flop	216.06	21.40	38.78
12	SR Latch	10.92	7.917	7.723
13	Shift Register	610.56	410.90	390.5
14	Novel Low Power FA 180 nm	76.73	47.48	44.96
15	Novel Low Power FA 90 nm	3.003	1.731	1.722
16	Novel Low Power FA 45 nm	0.501	0.383	0.375
17	Peres gate	61.48	36.79	36.47
18	Feynman Gate	49.66	34.36	33.51
19	Fredkin Gate	115.50	67.56	66.01
20	C17-ISCAS85	72.68	63.29	58.07
21	S27	3270.00	309.40	515.0

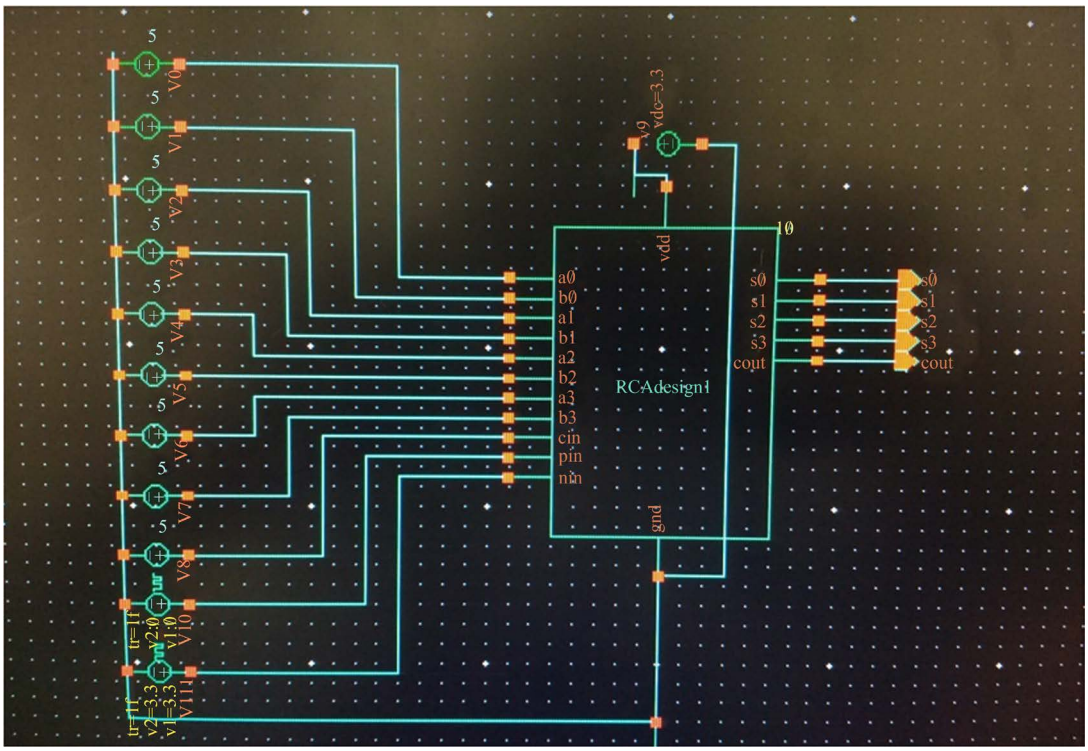

Figure 10. Ripple carry adder with Trig01 gates.

Table 3. Energy analysis of CMOS gates and various CMOS circuits. This comparison **Table 2** gives a detail about the energy consumed by the device in previous method and the proposed method. As a result nearly 48% energy consumption is reduced then existing one.

S. NO	CMOS Circuit	Existing Design Energy in nano joules	Proposed Design-1 Energy in nano joules	Proposed Design-2 Energy in nano joules
1	NOT Gate	2.88	1.50	1.36
2	AND Gate	0.490	0.258	0.248
3	OR Gate	0.688	0.372	0.364
4	NAND Gate	0.423	0.225	0.208
5	NOR Gate	0.417	0.246	0.241
6	EX-OR Gate	1.38	0.733	0.736
7	Full Adder	97.20	6.38	6.28
8	Carry Look Ahead Adder	73.20	5.34	5.41
9	Ripple Carry Adder	30.00	19.79	14.08
10	Carry Select Adder	79.80	52.68	42.60
11	D Flip Flop	21.60	2.14	3.87
12	SR Latch	0.436	0.316	0.308
13	Shift Register	61.00	41.09	39.05
14	Novel Low Power FA 180 nm	6.13	3.79	3.59
15	Novel Low Power FA 90 nm	0.240	0.138	0.137
16	Novel Low Power FA 45 nm	0.040	0.030	0.030
17	Peres gate	2.45	1.47	1.45
18	Feynman Gate	1.98	1.37	1.34
19	Fredkin Gate	9.24	5.40	5.28
20	C17-ISCAS85	7.20	6.32	5.80
21	S27	240	24.7	41.2

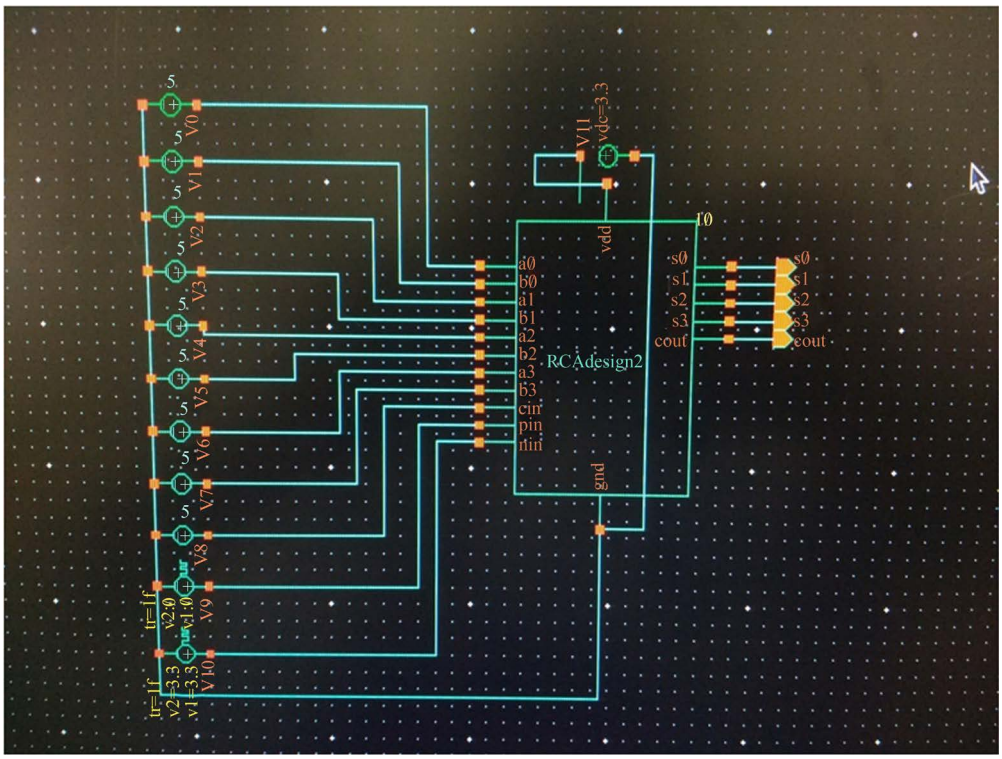

Figure 11. Ripple carry adder with Trig10 gates.

Table 4. Delay analysis of CMOS gates and various CMOS circuits. This comparison **Table 3** gives a detail about the maximum delay by the device in previous method and the proposed method. As a result delays are same as in the previous method even transistor are added in additional.

S.NO	CMOS Circuit	Existing Design Delay in Pico seconds	Proposed Design-1 Delay in Pico seconds	Proposed Design-2 Delay in Pico seconds
1	NOT Gate	26.56	25.98	26.02
2	AND Gate	20.06	20.06	20.06
3	OR Gate	40.01	39.21	39.85
4	NAND Gate	20.05	20.05	20.05
5	NOR Gate	49.41	47.77	48.42
6	EX-OR Gate	65.15	65.23	65.27
7	Full Adder	140.30	140.25	141.60
8	Carry Look Ahead Adder	142.90	142.79	142.88
9	Ripple Carry Adder	139.10	138.92	139.12
10	Carry Select Adder	599.70	598.99	600.20
11	D Flip Flop	81.19	81.02	81.15
12	SR Latch	10,020	10,040	10,020
13	Shift Register	9800	9788	9802
14	Novel Low Power FA 180 nm	80.71	80.59	81.02
15	Novel Low Power FA 90 nm	40.92	40.82	41.03
16	Novel Low Power FA 45 nm	14.31	14.19	14.20
17	Peres Gate	36.29	36.19	36.32
18	Feynman Gate	36.09	36.09	36.22
19	Fredkin Gate	10,070	10,069	10,072
20	C17-ISCAS85	10,050	10,051	10,051
21	S27	30,020	30,022	30,025

the power consumption and also the leakage current. The power consumed by the sub-clock circuit is only about 46% when compared to the ideal circuit [1]-[7]. Similarly the energy consumed by the circuit is also reduced up to 40% compared to the existing/ideal circuits. This method does not affect the performance of the circuit; delay of the circuit is similar to that of the ideal CMOS circuit and produces about 95% of efficiency. This can be implemented in any kind of logic in digital circuit. These designs can be extended to dual sleep technique and also in dual stack technique in order to utilize the whole circuit performance. Sub-clocking is the technique which is more efficient than that of the Dual Mode Logic [9] and an ideal circuit without sub-clock method. Depending on the technology (180 nm, 90 nm, 45 nm) and period of operation, the energy consumption can be varied and also the power consumption is reduced up to 54% [11]. To get the proper operating point, the width of the transistor is varied using the Cadence Virtuoso tool.

References

[1] Kaizerman, A., Fisher, S. and Fish, A. (2013) Subthreshold Dual Mode Logic. *IEEE Transactions on Very Large Scale Integration System*, **21**, 979-983. http://dx.doi.org/10.1109/TVLSI.2012.2198678

[2] Bol, D., Ambroise, R., Flandre, D. and Legat, J.D. (2008) Analysis and Minimization of Practical Energy in 45 nm Subthreshold Logic Circuits. *IEEE International Conference on Computer Design*, Lake Tahoe, 12-15 October 2008, 294-300.

[3] Calhoun, B.H., Wang, A. and Chandrakasan, A. (2005) Modeling and Sizing for Minimum Energy Operation in Subthreshold Circuits. *IEEE Journal of Solid-State Circuits*, **40**, 1778-1786. http://dx.doi.org/10.1109/JSSC.2005.852162

[4] Alioto, M. (2012) Ultralow Power VLSI Circuit Design Demystified and Explained: A Tutorial. *IEEE Transactions on Circuits Systems I*, **59**, 3-29. http://dx.doi.org/10.1109/TCSI.2011.2177004

[5] Chang, M.H, Hsieh, C.Y., Chen, M.W. and Hwang, W. (2015) Logical Effort Models with Voltage and Temperature Extensions in Super-/Near-/Sub-Threshold Regions. 2011 *International Symposium on VLSI Design, Automation and Test* (*VLSI-DAT*), Hsinchu, 25-28 April 2011, 1-4.

[6] Kwong, J. and Chandrakasan, A.P. (2006) Variation-Driven Device Sizing for Minimum Energy Sub-Threshold Circuits. *Proceedings of the* 2006 *International Symposium on Low Power Electronics and Design*, Bavaria, 4–6 October 2006, 8-13. http://dx.doi.org/10.1145/1165573.1165578

[7] Levi, Kaizerman, A. and Fish, A. (2012) Low Voltage Dual Mode Logic: Model Analysis and Parameter Extraction Excepted Elsevier. *Microelectronics Journal*, **12**, 1778-1786.

[8] Liu, X., Zheng, Y., Phyu, M.W., Endru, F.W., Navaneethan, V. and Zhao, B. (2012) An Ultra-Low Power ECG Acquisition and Monitoring ASIC System for WBAN Applications. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2**, 60-70. http://dx.doi.org/10.1109/JETCAS.2012.2187707

[9] Markovic, D., Wang, C.C., Alarcon, L.P. and Rabaey, J.M. (2010) Ultralow Power Design in Near-Threshold Region. *Proceedings of the IEEE*, **98**, 237-252. http://dx.doi.org/10.1109/JPROC.2009.2035453

[10] Morgenshtein, E.G., Friedman, Ginosar, R. and Kolodny, A. (2010) Unified logical Effort-A Method for Delay Evaluation and Minimization in Logic Paths with Interconnect. *IEEE Transactions on Very Large Scale Integration* (*VLSI*) *Systems*, **18**, 689-696. http://dx.doi.org/10.1109/TVLSI.2009.2014239

[11] Pu, Y, de Gyvez, J.P. and Corporaal, H. (2009) An Ultralowenergy/Frame Multi-Standard JPEG Co-Processor in 65 nm CMOS with Sub/Near-Threshold Power Supply. 2009 *IEEE International Solid-State Circuits Conference*, San Francisco, 8-12 February 2009, 146-147.

[12] Razak, H. (2008) High Performance ASIC Design: Using Synthesizable Domino Logic in an ASIC Flow. Cambridge University, Cambridge.

[13] Soeleman, H., Roy, K. and Paul, B. (2001) Sub-Domino Logic: Ultralow Power Dynamic Sub-Threshold Digital Logic. *Fourteenth International Conference on VLSI Design*, Bangalore, 7 January 2001, 211-214. http://dx.doi.org/10.1109/icvd.2001.902662

[14] Verma, N., Kwong, J. and Chandrakasan, A. (2008) Nanometer MOSFET Variation in Minimum Energy Subthreshold Circuits. *IEEE Transactions on Electron Devices*, **55**, 163-174. http://dx.doi.org/10.1109/TED.2007.911352

[15] Yamada, H., Hotta, T., Nishiyama, T., Murabayashi, F. and Yamauchi, T. (1995) A 13.3 ns Double-Precision Floating-Point ALU and Multiplier. 1995 *IEEE International Conference on Computer Design*: *VLSI in Computers and Processors*, 2-4 October 1995, 466-470.