

Error Correction Circuit for Single-Event Hardening of Delay Locked Loops

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Abstract

In scaled CMOS processes, the single-event effects generate missing output pulses in Delay-Locked Loop (DLL). Due to its effective sequence detection of the missing pulses in the proposed Error Correction Circuit (ECC) and its portability to be applied to any DLL type, the ECC mitigates the impact of single-event effects and completes its operation with less design complexity without any concern about losing the information. The ECC has been implemented in 180 nm CMOS process and measured the accuracy of mitigation on simulations at LETs up to 100 MeV-cm²/mg. The robustness and portability of the mitigation technique are validated through the results obtained by implementing proposed ECC in XilinxArtix 7 FPGA.

Keywords

Delay-Locked Loop, Single Event Transients, Error Correction Circuit

1. Introduction

Advanced clock networks are required in space application for implementation of data handling, communications and attitude orbit control subsystems. With the limited availability of space-qualified clock networking and frequency control, a fully integrated radiation-hardened clock generator solution is needed. Mostly clock generator employs a Phase-Locked loop (PLL), with stability issues much thwarting in harsh environment and design complexity has made Delay-Locked Loop (DLL) as a viable alternate for clock generator in stern space environment.

The Single-Event Transients (SETs) caused by energetic particle strikes are of increasing concern for the circuits working in radiation environments. The SETs taking place within a DLL are of particular concern as it could corrupt the clock or data-transfer across entire distribution networks, possibly leading to spacecraft failure

[1]. In SET characterization of DLL found the Voltage Controlled Delay Line (VCDL) as most sensitive sub-circuit followed by Charge Pump (CP). The VCDL of the DLL generates missing pulses [1] at the output of the DLL. The standard Radiation Hardening By Design (RHBD) techniques like Dual-Modular Redundancy (DMR) and Triple-Modular Redundancy (TMR) [2] have area penalties. In the literature, hardening of VCDLs has been explored to mitigate the missing pulse errors. The VCDL utilizing complementary differential pair delay cells was proposed in [1] was observed to have missing pulses at frequencies above 1 GHz, due to lower critical charge as a result of technology scaling. A peeled VCDL design with a missing-pulse detection and correction block was proposed in [3] mitigated the missing pulses with high design complexity and can be only applied to DLL with two complementary VCDL outputs.

The method proposed in this paper simplifies the Single Event Hardened (SEH) technique from [3] while maintaining performance, and generalises the technique from [3] to be able to applied DLL with both single and differential ended VCDL.

2. Single-Event Error Correction Circuit

Figure 1 introduces a proposed SEH-DLL which can simultaneously detect and mitigate the missing pulses with the proposed Single-Event Error Correction Circuit (SE-ECC) shown in Figure 2. The SE-ECC can be used in DLL with any VCDL topology. In this work the ECC is applied on the VCDL topology used in [4]. The SE-ECC is implemented using an Overlapping Sequence Detector(OSD) based on state diagram shown in Figure 3, Lock Detector (LD) [5] and multiplexers which propagate the uncorrupted V_OUT based on the truth table (Table 1). For example, when there is a upset in the V_DL output, the missing pulse error is detected by the OSD and instead of propagating the V_DL signal the REF_CLK is propagated if the loop is locked, which is detected by the LD. In this way V_OUT signal is generated without the impact of single-event transient. If there are no upsets in V_DL output, the MUX_1 select (Sel) will be set to logic “0”, and the ECC will output V_DL to the V_OUT. Figure 4 shows the error correction process of SE-ECC.

In this paper, the proposed SE-ECC minimises the duty cycle variation to be <10 ps. Furthermore, the design

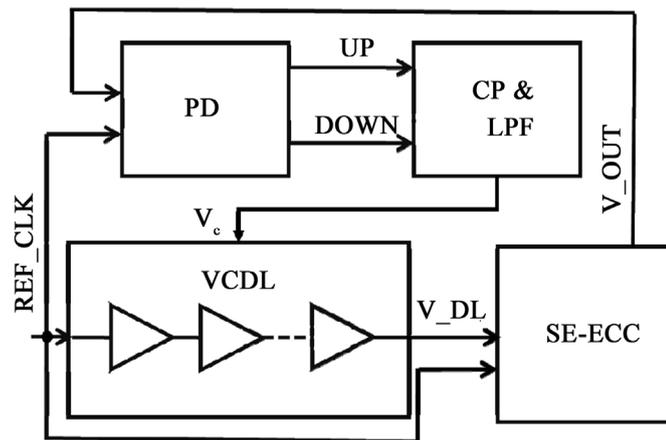


Figure 1. Proposed SEH-DLL.

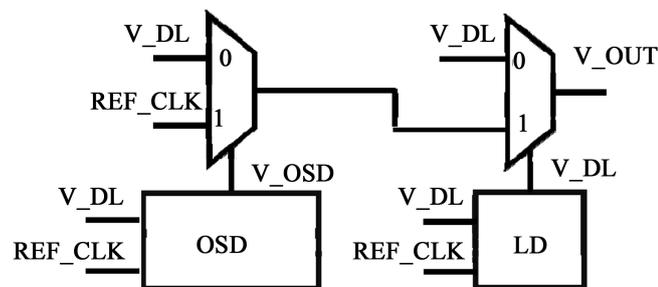


Figure 2. Architecture of proposed SE-ECC architecture.

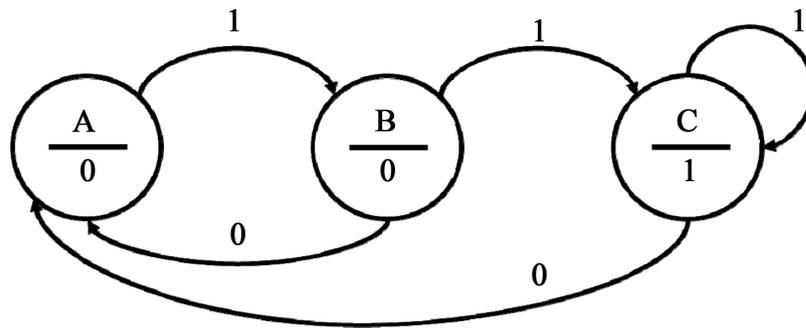


Figure 3. State diagram of OSD.

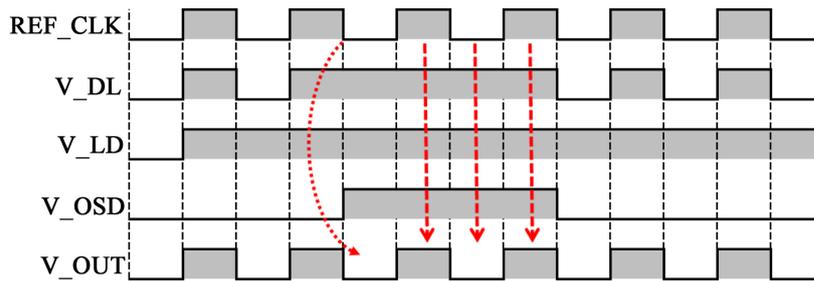


Figure 4. Proposed SE-ECC error correction process.

Table 1. SE-ECC truth table.

V_OSD	V_LD	V_OUT
0	0	V_DL
0	1	V_DL
1	0	V_DL
1	1	REF_CLK

and area complexity is high reduced in comparison with [3]. Furthermore, it can simultaneously mitigate the missing pulse without affecting the locked state of DLL (No change in the control voltage), in this manner the SE-ECC can bolster the stability and reliability of the DLL.

3. Simulation Results

The high-energy particles that pass through critical regions of the device PN junctions, depositing energy in the silicon cause single event transients. The dense track of electron-hole pairs generated by the energy deposited by the ion strike, which move across the junction, leading to a transient current pulse on the struck node [6]. The current generated by the incident ion is modeled using a current source and injected in the strike node. This radiation strike is characterized by two collection phases: a first phase of E-field accelerated free carrier motion (fast drift current) followed by a second phase of charge collection which produces a slow current diffusion due to the free carrier density gradients. Since the E-field is present in the space charge region for an off transistor the most sensitive region to an ion strike is the drain terminal [7]. Subsequently it ably collects any charge generated in the vicinity. Double-exponential pulse is a broadly accepted shape for the SET current source [8] [9]:

$$i(t) = \frac{Q}{\tau_f - \tau_r} \left(e^{-\frac{t-t_0}{\tau_f}} - e^{-\frac{t-t_0}{\tau_r}} \right) \tag{1}$$

where Q is the injected charge, and τ_f, τ_r are the fall and rise time constants of the current generated by the ion. The ion-induced Single Event (SE) current profiles for linear energy transfer values between 20 MeV-cm²/mg

and 100 MeV-cm²/mg for 180 nm NMOS are simulated using TCAD simulator .The NMOS transistors worst case current pulse profile for a heavy ion strike ranging over LET of 80 MeV-cm²/mg is obtained from TCAD mixed-mode simulations using ISE-TCAD [Sentaurus] is shown in **Figure 5**. The NMOS transistors model were calibrated for voltage over a range of 0 to 1.8 V to replicate the electrical DC transistor characteristics as defined in the PDK within a 5% error margin.

The SE-ECC was designed in 180 nm Bulk CMOS process design kits (PDKs), and simulated at frequencies between 500 MHz and 1 GHz. The circuits was simulated using ion-induced SE current profiles, obtained from the from TCAD simulations similar to ISDE bias dependent current model generator [10], with simulated LET values between 10 MeV-cm²/mg and 100 MeV-cm²/mg. The same type of simulation approach is proven to be effective via the experimental validation of the SET responses of mixed-signal circuits such as digital PLLs [10]. The transient responses of the outputs V_DL and V_OUT are compared. **Figure 6** represents the case where

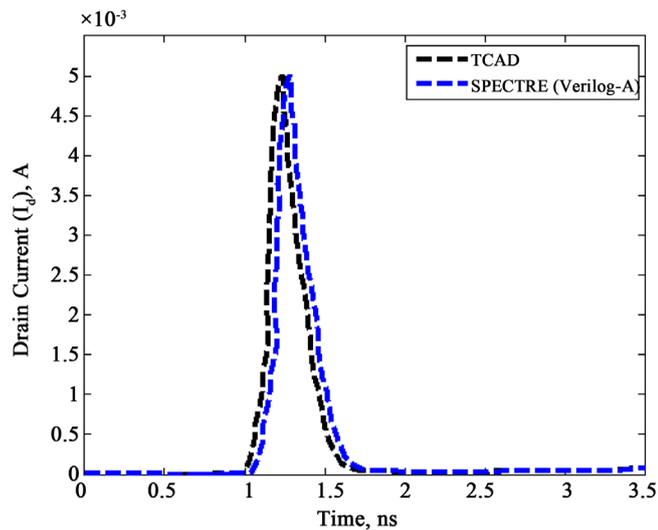


Figure 5. Ion induced current vs. time for a LET 80 MeV-cm²/mg.

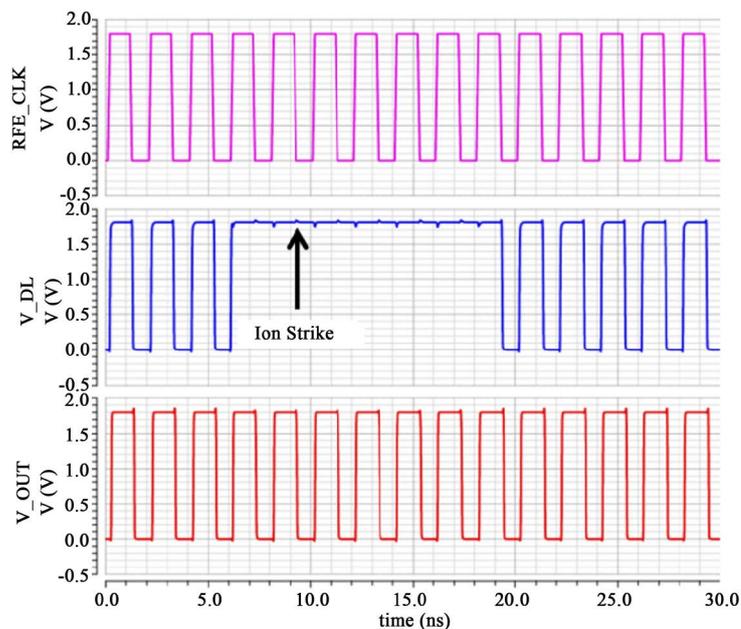


Figure 6. Worst case SET response (in terms of missing pulses and phase error) generated by VCDL and SE-ECC at LET = 100 MeV-cm²/mg.

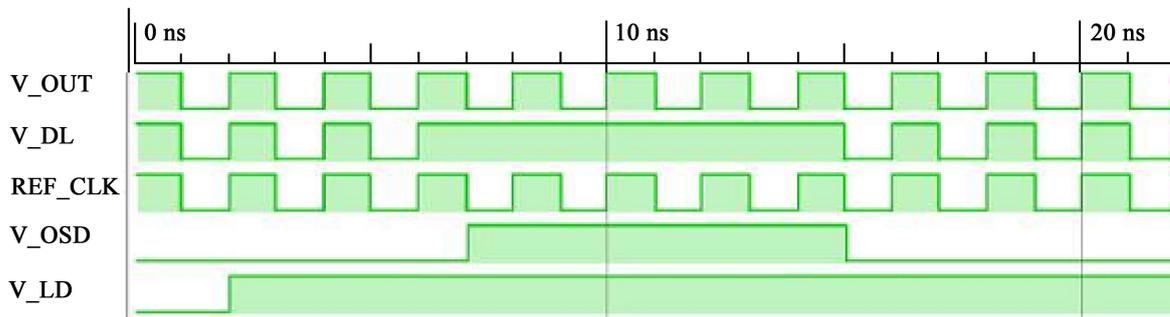


Figure 7. Worst case SET response functional simulation on a FPGA.

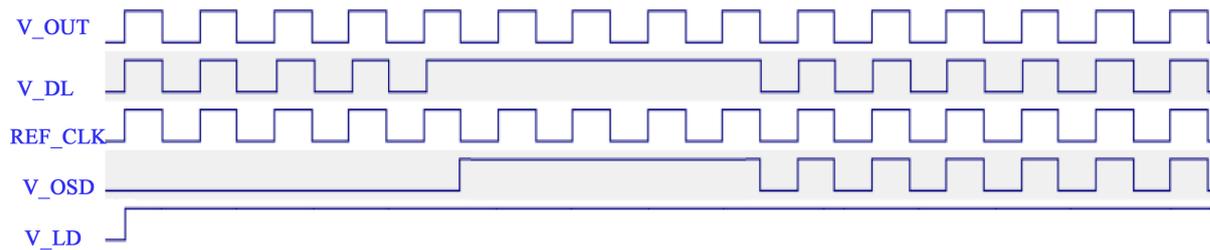


Figure 8. Experimental results of the SE-ECC implemented on the Artix 7 FPGA.

V_DL is perturbed and six missing pulses are generated. However, no missing pulses are observed at the DLL output V_OUT, and therefore no errors are propagated into the clock system. One can observe duty cycle variation caused by pulse skew following the switching operation of the MUX. The duty cycle variation was minimized to 5% in comparison with [3].

The SE-ECC effectiveness is validated experimentally using a Xilinx Artix 7 implemented on a Basys3 board. The ion strikes were emulated and missing pulses errors are generated. Then the generated errors are injected in to the SE-ECC, **Figure 7** shows the functional simulation of the SE-ECC. The experimental results of SE-ECC are obtained and analysed using ChipScope Pro Analyzer tool, the SET response on SE-ECC on injected missing pulses are shown in **Figure 8**. These results conclude the portability and robustness of SE-ECC.

4. Conclusion

A SE-ECC was implemented in a 180 nm CMOS process and measured the accuracy of mitigation on simulations at LETs up to 100 MeV-cm²/mg. The error correction technique completely eliminates missing pulses, independent of the technology node or the operating frequency of the DLL, as proven by simulation and emulation results and also any strike within the error correction circuit itself will have no significant impact on the DLL output signal. This SEH technique can be applied to a variety clock circuit using single or differential output cell topologies.

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