Circuits and Systems, 2016, 7, 1441-1454
Published Online June 2016 in SciRes. http://www.scirp.org/journal/cs
http://dx.doi.org/10.4236/cs.2016.78126

Hybrid Control Strategy for BCD Topology Based Modular Multilevel Inverter

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Received 28 March 2016; accepted 20 April 2016; published 9 June 2016

Abstract

In this paper, a Binary Coded Decimal (BCD) topology of modular multilevel inverter with reduced component count is proposed. For the control of this inverter, hybrid control strategy is used. The proposed modular multilevel inverter uses asymmetrical dc sources and reduced number of switches topology. This hybrid modulation technique uses the multicarrier based Pulse Width Modulation (PWM) and the fundamental frequency modulation strategy. The hybrid modulation algorithm is implemented with "NUC140" micro-controller. In comparison with the conventional and some of the recently reported inverter topologies, the proposed inverter topology is able to generate high number of voltage levels in the output by using minimum number of components such as dc sources, power switches and driver circuits. This inverter offers significant performance with less number of components. The feasibility of the proposed topology is confirmed by simulation and experimental results.

Keywords

Multilevel Inverter, Reduced Components, Hybrid PWM, Asymmetrical dc Sources, Harmonic Distortion

1. Introduction

A Multilevel Inverter (MLI) is an array of power semiconductor switches. It has gained increasing attention in industry and research since it was introduced in the 1980s [1]. The advantages of this method over the conventional two-level inverter approach are: improved output power quality, lower output harmonics, lower voltage stress on the switches and load, improved amplitude of fundamental components and lower electromagnetic in-

How to cite this paper: Karthikeyan, V. and Jamuna, V. (2016) Hybrid Control Strategy for BCD Topology Based Modular Multilevel Inverter. *Circuits and Systems*, **7**, 1441-1454. http://dx.doi.org/10.4236/cs.2016.78126

terference [2] [3]. The concept of MLI is to add several small dc sources with appropriate switching sequence to the array of switches so as to obtain a stepped waveform which resembles the ac sine waveform. Hence inverter operation is obtained. As the number of steps in the output waveform increases, these merits will be enhanced.

There are three types of commonly used MLI topologies: Neutral point or diode clamped (NPC) [4], flying capacitor (FC) [5] and cascaded H-bridge (CHB) [6] multilevel inverter. Among these MLI topologies CHB multilevel inverter (CHBMLI) becomes more popular, because of its superior trustworthiness arising from its modularity and lesser number of hardware components. Series connection of several H-bridge inverters forms a CHBMLI. Each H-bridge can generate three voltage levels in the output. These inverters are classified as: Symmetric (each H-bridge is fed by equal dc sources) and Asymmetric (each H-bridge is fed by unequal dc sources) MLIs. An asymmetric CHBMLI configuration is preferred to produce more number of output levels with the same number of power switches. Basically, there are two asymmetrical configurations: binary and ternary. There are various other asymmetrical MLI topologies proposed by many researchers [7]. Since the MLI topologies require reduced voltage stress on the switching devices, we can realize the high power inverters with low power matured semiconductor technology [8]. MLIs have been used in many applications, such as adjustable speed drives, liquefied energy gas (LNG) plants, power quality devices and renewable energy generation such as photovoltaic, wind and fuel cells [8]-[11].

The power quality of the MLI depends on the number of levels in the output. The main disadvantage of MLI is the requirement of more number of power switches and associated driver circuits with the increase in the number of levels at the output. This increases the circuit complexity and the overall cost and size of the system. Creation of asymmetrical dc sources is another challenge of MLI. With hybrid renewable energy generation, various voltage levels produced by different energy sources can be used as the dc sources of asymmetrical MLI. It avoids the use of flying capacitors or boost converters stage of the conventional hybrid energy generation system. To conquer these disadvantages, many topologies are introduced with reduced number of switches [7] [12]-[21]. Major disadvantage with the conventional MLI is the requirement of small isolated dc voltage sources or series bank capacitors. This disadvantage is overcome by using the renewable energy generation sources.

The modulation technique used to generate the gating signals is very vital to attain high performance control in the MLIs. Various modulation techniques have been introduced to improve the performance of the MLIs [2] [11] [22]-[27]. The commonly used modulation techniques are selective harmonic elimination (SHE) [22]-[24] carrier-based PWM (CBPWM) [25] and space vector PWM (SVPWM) [26] [27]. In [28], the MLI performances of a SVPWM and a carrier based PWM are compared, and a carrier based PWM method is proposed to obtain an optimal output voltage in the MLI.

In this paper, a BCD topology of modular multilevel inverter with unequal dc sources and reduced number of switches is proposed. The performance of the proposed inverter is controlled by the hybrid control strategy. This topology requires lesser number of power switches, power diodes and associated driver circuits than the conventional topologies. These advantages are proved by comparing the proposed topology with the conventional symmetric and various asymmetric optimal topologies reported in the literature. The power loss and conversion efficiency are estimated from the simulation results. Finally, the experimental results of a 9-level inverter are presented and these validate all the theoretically obtained results.

2. Structure of BCD Topology Inverter

Figure 1(a) shows the generalized circuit diagram of proposed 9-level inverter with reduced number of switches. The functional block diagrams of hybrid energy generation system with symmetrical MLI and Hybrid energy generation with proposed asymmetrical MLI are given in **Figure 1(b)** and **Figure 1(c)**. The proposed topology of inverter is built by the cascaded connection of a number of sub-modules. Each sub-module consists of two unidirectional switches and one dc source. The switches in one sub-module should not be turned-on simultaneously. The dc sources are considered to follow the sequence of values like $1:2^0:2^1:\ldots.:2^n$ (BCD numbers). These asymmetrical sources are derived from the various renewable energy sources (RES). It avoids the intermittent stage of boost converters (BC). One of the issues in MLIs is controlling the input dc source voltages. Several techniques were used to control the input dc voltages of sources [22]. A MLI with unequal dc sources allows lesser freedom of choice in controlling the input voltages based on the switching states. The operation of this topology divides the circuits into two parts: Magnitude or Level generator and Polarity generator. For 9-level inverter, this topology uses two sub-modules (SM_1, SM_2) and three asymmetrical dc sources (V_{dc}, 2^0V_{dc}, 2^1V_{dc}) in the magnitude or level generator part. For higher levels of output, the number of sub-modules can be

cascaded in the level generator part. The level generator part is responsible for generating all the possible positive voltage levels of the output by proper switching function of switches in the level generator part. **Table 1** summarizes the parameters used in the present work.

The polarity generator is a simple full H-bridge (HBM) which provides the positive and negative polarities to the output of the level generator alternatively, so that the alternating output voltage is obtained. Switches SH_1 and SH_2 are turned ON and SH_3 and SH_4 are turned OFF during the positive half cycle while switches SH_3 and SH_4 are turned ON and SH_1 and SH_2 are turned OFF during the negative half cycle. The switches in this polarity generation part are operated at the fundamental (line) frequency. **Table 2** shows the switching patterns used to generate various levels of output voltage. Switching status '0' and '1' represents the switch OFF and ON conditions. 'x' represents don't care condition (either "0" or "1").

Each sub-module in the level generation part can generate one positive level and zero level output voltage. "*m*" numbers of dc sources are required for "*N*" levels in the output of the inverter,

$$N = 2^m + 1 \tag{1}$$

Number of sub-modules (n) required is given by,

$$n = m - 1 \tag{2}$$

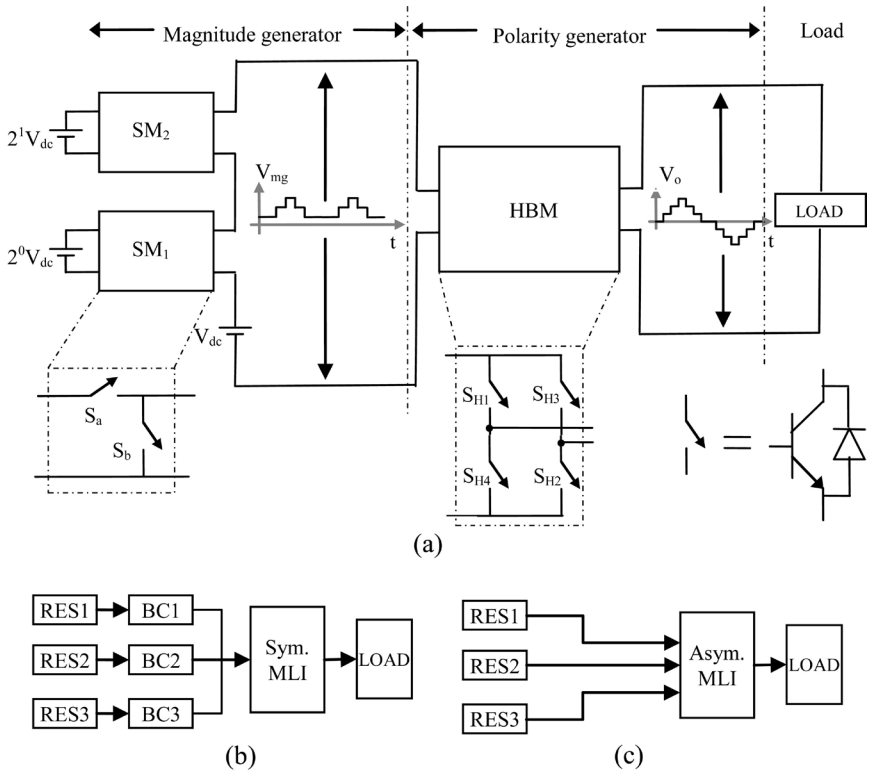

Figure 1. Proposed 9-level inverter (a) Circuit diagram (b) Hybrid energy generation with symmetrical MLI (c) Hybrid energy generation with proposed asymmetrical MLI.

Table 1. Parameters of proposed inverter.

Parameter	Value
No. of Levels	9
No. of Sub-Modules	2
Input dc Sources	3
No. of Switches	8
Load	50Ω

Table 2. Switching functions of proposed inverter.

Level	Output Voltage	Magnitude Generator S_{a1} S_{b1} S_{a2} S_{b2}	Polarity Generator S_{H1} S_{H2} S_{H3} S_{H4}
1	$4V_{dc}$	1010	1100
2	$3V_{dc}$	0110	1100
3	$4V_{dc}$	1001	1100
4	V_{dc}	0101	1100
5	0	xxxx	1010/0101
6	V_{dc}	0101	0011
7	$2V_{dc}$	1001	0011
8	$3V_{dc}$	0110	0011
9	$4V_{dc}$	1010	0011

Maximum output voltage obtainable is,

$$V_{o\max} = \left(2^{m-1}\right) \times V_{dc} = \frac{(N-1)}{2} \times V_{dc} \tag{3}$$

where, V_{dc} is the dc source voltage.

Number of power switches (N_{sw}) required for a single phase inverter is,

$$N_{sw} = 2(m-1) + 4 = \left[\frac{\log(N-1) - 0.301}{0.1505}\right] + 4 \tag{4}$$

Number of driver circuits required is,

$$N_{\text{driver}} = N_{sw} \tag{5}$$

In the proposed 9-level inverter, four levels of positive output voltage are generated by the level generator part. As the switch S_b of each sub modules (SM_1 & SM_2) conducts, the output voltage level of V_{dc} is obtained. As the switches S_a of SM_1 and S_b of SM_2 are operated, the output voltage level becomes $2V_{dc}$. For the output voltage level of $3V_{dc}$, the switches S_b of SM_1 and S_a of SM_2 are triggered and for the output voltage level of $4V_{dc}$, the switches S_a of each sub modules are triggered. By properly controlling the ON and OFF states of the switches in the H-bridge module, the four-level unidirectional output voltage waveform is converted into bidirectional eight-level output voltage waveform. The zero level output voltage is achieved by turning ON the switches SH_1 and SH_3 or SH_2 and SH_4.

3. Hybrid Control Strategy

To generate high quality output with MLI, various modulation techniques are used. Out of these techniques, SHE or CBPWM techniques are commonly used because of ease of controllability. With fundamental frequency modulation, each switch has to be turned ON and OFF once per cycle of the fundamental frequency output. This fundamental frequency modulation provides minimal switching loss, but the harmonic contents at the output voltage become high. The quality of the output is enhanced in the CBPWM techniques, but the switching losses and the circuit complexity are increased.

The idea behind this hybrid control strategy is to combine the advantages of both the fundamental frequency modulation and the CBPWM. In fundamental frequency modulation, one carrier signal and one reference signal are used. These signals are compared and produce the switching pulses at fundamental frequency. In CBPWM, phase disposition PWM (PDPWM) is more popular. THD content is much lesser with PDPWM control strategy based MLI. In this paper, a unipolar phase disposition PWM (UPDPWM) is considered as the number of carriers required in the UPDPWM is half of the carriers required by the PDPWM. In this modulation technique, the switches in the polarity generation part are operated at the fundamental frequency and the switches in the level generation part are operated by the UPDPWM. **Figure 2** shows the functional block diagram of the proposed hybrid modulation method. It consists of fundamental frequency PWM generator and UPDPWM generator to generate the modulated control pulses. These pulses are combined by the combinational logic circuit and produce the sequence of switching pulses required for the modular multilevel inverter.

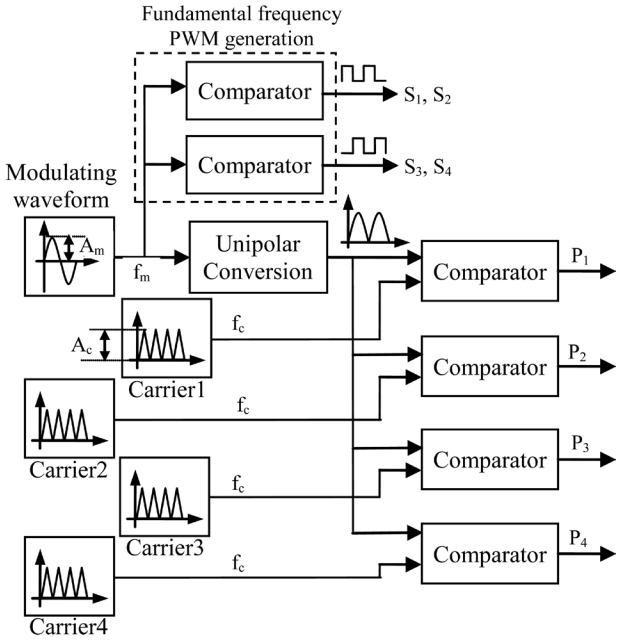

Figure 2. Block diagram of hybrid modulation for a 9-level inverter.

3.1. Fundamental Frequency PWM Generation

A basic comparator is used for the fundamental frequency PWM generation. The modulating sine waveform at fundamental frequency is compared with the zero reference and produces the pulses at the fundamental frequency. These pulses are processed by the combinational logic formed by (6)-(9). The pulses produced by the combinational logic circuit are used to control the switches in the polarity generation part of the proposed inverter.

$$G_{H1} = (P_1 + P_2 + P_3 + P_4) \cdot S_1 \tag{6}$$

$$G_{H2} = (P_1 + P_2 + P_3 + P_4) \cdot S_2 \tag{7}$$

$$G_{H3} = (P_1 + P_2 + P_3 + P_4) \cdot S_3 \tag{8}$$

$$G_{H4} = (P_1 + P_2 + P_3 + P_4) \cdot S_4 \tag{9}$$

where, G_{H1}, G_{H2}, G_{H3}, G_{H4} are the gating pulses applied to the switches H_1, H_2, H_3 and H_4 in the polarity generation part. S_1, S_2, S_3, S_4 are the pulses produced by the fundamental frequency PWM generation part. P_1, P_2, P_3 and P_4 are the pulses produced by the UPDPWM generation part.

3.2. UPDPWM Generation

The modulating and high frequency carrier signals used for UPDPWM are shown in **Figure 3**. In UPDPWM, four triangular carrier signals are compared with the unipolar modulating signal. All the carrier signals are in phase, but they are level shifted. The pulses (P_1, P_2, P_3 and P_4) produced by the comparators give the level transition point of the output waveforms and these signals are processed by the combinational logic formed by (10)-(13) and produce appropriate switching patterns for different output voltage levels. **Table 3** summarizes the parameters used for hybrid modulation.

$$G_{a1} = (P_1 \oplus P_2) + (P_3 \oplus P_4) \tag{10}$$

$$G_{b1} = (P_1 P_2) + (P_3 \oplus P_2) \tag{11}$$

$$G_{a2} = P_2 \oplus P_4 \tag{12}$$

$$G_{b2} = P_2 \tag{13}$$

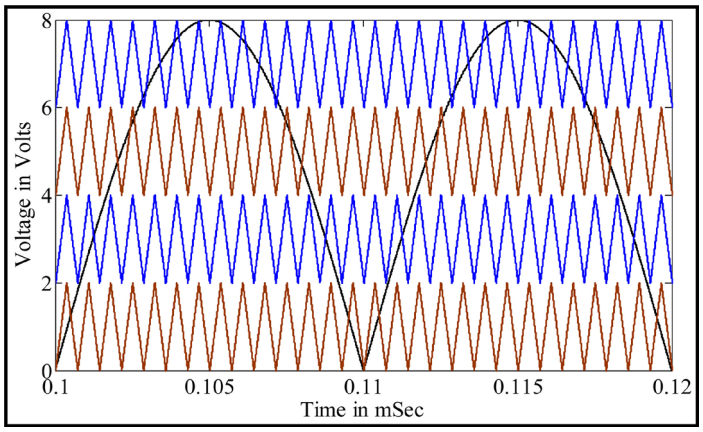

Figure 3. Carrier and reference waveforms for the UPDPWM of 9-level inverter.

Table 3. Parameters used for hybrid modulation.

Parameter	Value
No. of Carriers	4
No. of Reference signals	1
Modulation index for frequency	26
Modulation index for amplitude	1.05
Fundametal Frequency	50 Hz

where, G_{a1}, G_{b1}, are the gating pulses applied to the switches in the first sub-module (SM_1). G_{a2}, G_{b2} are the gating pulses applied to the switches in the second sub-module (SM_2).

4. Results and Discussions

4.1. Simulation Results

In order to study, the feasibility of the proposed BCD topology of multilevel inverter with hybrid control strategy, simulations were carried out using MATLAB/Simulink. The developed Simulink model for the proposed topology is shown in **Figure 4**. As per the general structure of BCD topology discussed earlier, two sub-modules, namely SM_1, SM_2 and one polarity generator (HBM) were used. The driving pulses for the switches used in the proposed topology were generated using hybrid control strategy discussed in **Table 2**. The generated switching patterns used for various switches in the proposed inverter are shown in **Figure 5(a)** and **Figure 5(b)**. It is interesting to note that the switches in the polarity generation part are operated at the fundamental frequency and the switches in the level generation part are operated at higher frequency. **Figure 5(c)** shows the output voltage (V_{mg}) waveform of the magnitude generator part. **Figure 6(a)** and **Figure 6(b)** shows the 9-level output voltage (V_o) and output current (I_o) waveforms for R-load respectively. **Figure 6(c)** shows the FFT spectra of output voltage. **Figure 6(d)** shows the output comparison of total harmonic distortion and fundamental voltage for various modulation indices. It produces a 9-level output with the Total Harmonic Distortion (THD) of 10.9% and also almost all the lower order harmonics are less than 4%. The output current waveform for RL-load is shown in **Figure 6(e)** which looks like a smooth sine waveform.

In order to explore the capability of the suggested topology, the proposed inverter was compared with various types of MLIs such as symmetric CHB, asymmetric CHB and some of the topologies of asymmetrical MLI with reduced number of switches reported in the literature [14] [15]. It was evident that the suggested MLI could considerably reduce the required number of power switches and dc sources. For the same number of dc sources (n), **Table 4** explains the number of output levels, the required number of switches, driver circuits, diodes and control signals of the proposed inverter and the existing MLI topologies. From **Figure 7(a)**, it is clear that the proposed method requires lesser number of dc sources than the other topologies with reduced number of switches. For instance, at N = 33, the existing topologies [14] [15] require 7 and 6 asymmetric dc sources re-

spectively, whereas the proposed topology requires only 5 asymmetric dc sources. As shown in **Figure 7(b)**, it can be noticed that the proposed topology requires lesser number of power switches. For instance, at N=33, the existing topologies [14] [15] require 16 and 18 switches respectively, whereas the proposed topology requires only 12 switches. **Figure 7(c)** shows that the number of driver circuits required in the proposed topology is also lesser than the other topologies. The input dc voltage of the proposed inverter is considered as constant, but it is not practical it may be controlled as described in [32].

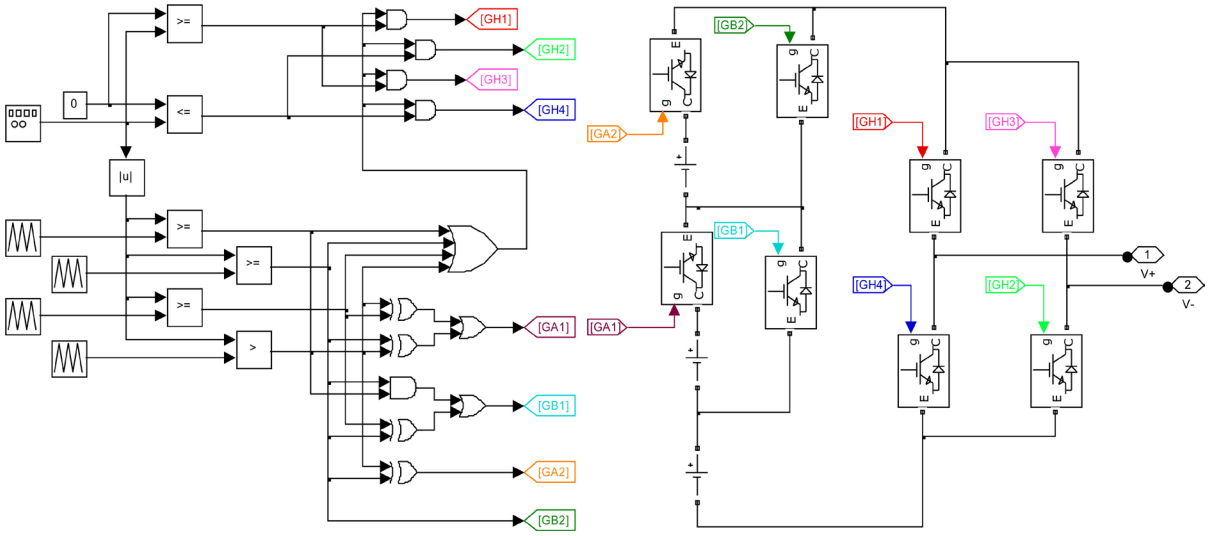

Figure 4. Simulink model of proposed 9-level inverter.

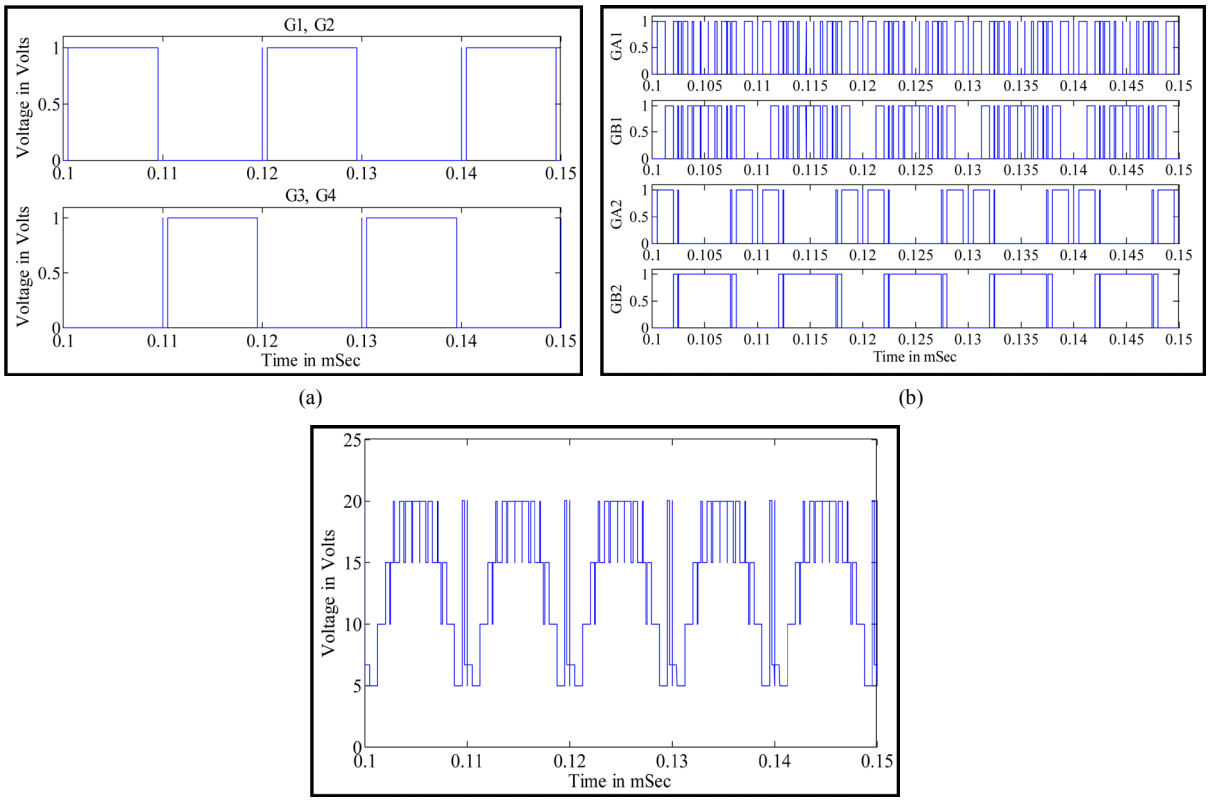

Figure 5. Switching pulses for (a) polarity generator (b) magnitude generator (c) Output of magnitude generator(V_{mg}).

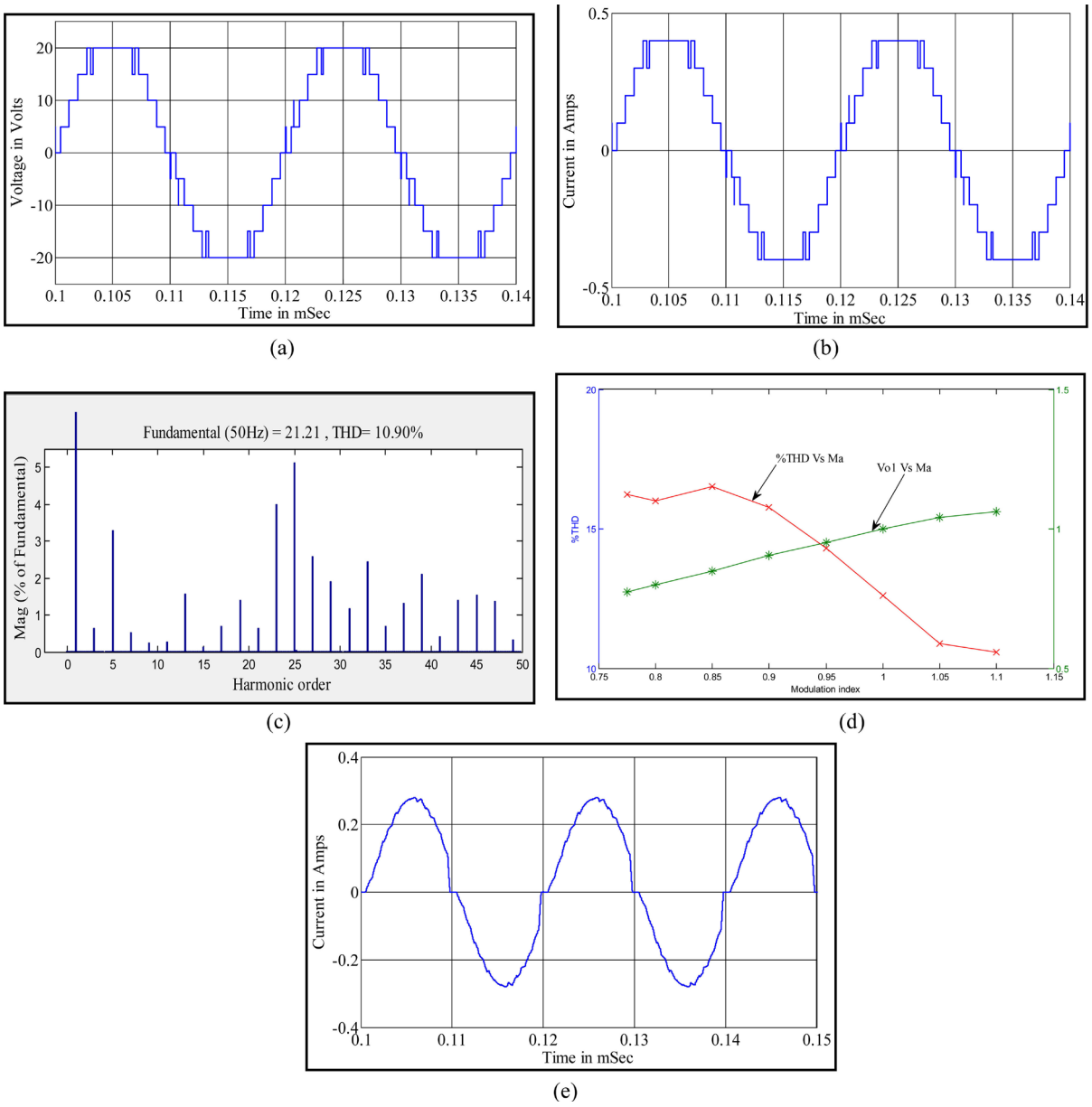

Figure 6. Simulated outputs of 9-level inverter (a) Output voltage waveform (b) Output current waveform for R-load (c) FFT spectra of output voltage (d) Output comparison for various modulation indices (e) Output current waveform for RL-load.

Table 4. Comparison of proposed topology with other topologies.

Converter Type	CHB			Topology in [14]	Topology in [14]	Proposed topology
	Symmetric	Binary	Ternary			
No. of Levels	$2n+1$	$2^{(n+1)}-1$	3^n	$2^{(n+3)}-5$	$3\times2^{(n+1)}-7$	2^n+1
Switches	$4n$	$4n$	$4n$	$5n+6$	$6n$	$2(n-1)+4$
Gate Drivers	$4n$	$4n$	$4n$	$5n+6$	$6n$	$2(n-1)+4$
Diodes	$4n$	$4n$	$4n$	$5n+6$	$6n$	$2(n-1)+4$
DC Supplies	n	n	n	$3n+1$	$2n$	n
Control Signals	$4n$	$4n$	$4n$	$5n+6$	$6n$	$2(n-1)+4$
Max. output voltage	n	2^n-1	$(3^n-1)/2$	$2^{(n+2)}-3$	$3\times2^n-4$	2^{n-1}

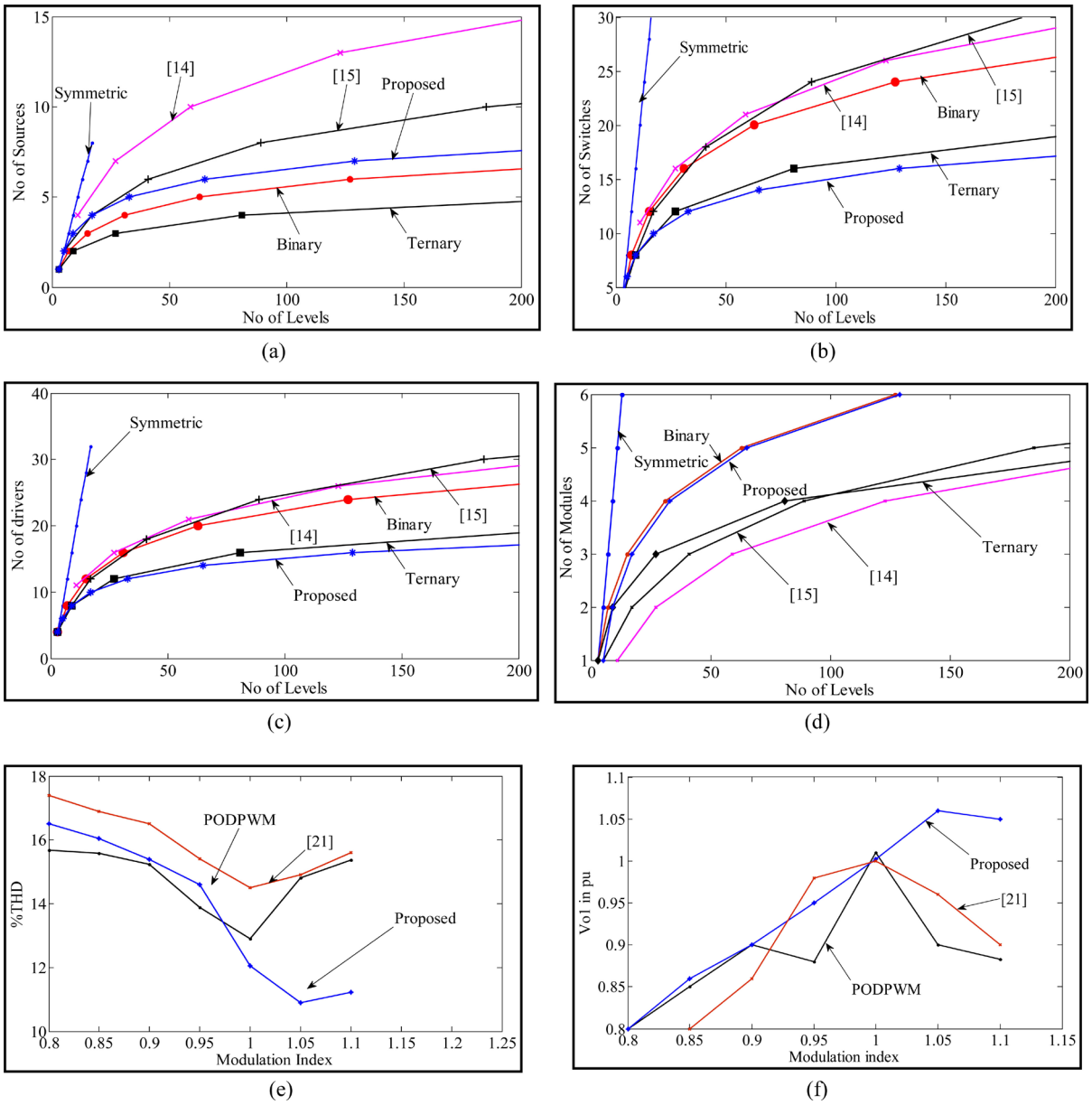

Figure 7. Comparison of proposed topology and other topologies (a) No. of Sources Vs No. of Levels (b) No. of Switches Vs No. of Levels (c) No. of Drivers Vs No. of Levels (d) No. of Modules Vs No. of Levels (e) %THD Vs Modulation Index (f) V_{o1} Vs Modulation index.

The numbers of sub-modules used in various topologies are shown in **Figure 7(d)**. The performance comparison of the hybrid control and other control techniques for various modulation indices are shown in **Figure 7(e)** and **Figure 7(f)**, it is noticed that this hybrid control can be used for wide range of modulation indices.

In the proposed 9-level inverter, the number of on-state switches at any instance of operation is only four switches (two from polarity generation part and two from level generation part). This is less than the topologies presented in [14]. Therefore, the conduction loss of the proposed inverter is less. Also the switches in the polarity generator part are operated at the fundamental frequency and those in the level generation part are operated at the higher frequency. Therefore, the switching loss of the proposed topology is also less. Hence, the lesser conduction loss and switching losses lead to higher conversion efficiency of the inverter.

This section is arranged to evaluate the losses of the multilevel inverters. There are three types of losses incurred in the multilevel inverters: Conduction losses (when the switch is in ON state), switching losses (when

the state of the switch changes from ON to OFF or vice versa) and losses due to leakage current (when the switch is in OFF state). Since the leakage current during the OFF state or blocking state is practically negligible, the losses due to leakage current are also negligible. Therefore, in the present work the losses due to conduction (P_{con}) and switching (P_{sw}) alone are considered for the power loss calculation.

In order to calculate the conduction losses, it is necessary to evaluate the losses of one typical switch and then, the similar approach could be generalized to overall system. Each power semiconductor switch is composed of a MOSFET and anti-parallel diode. To identify instantaneous values of conduction losses, the following Equations [29] [30] are used.

$$P_{con,T}(t) = \left[V_T + R_T i^{\beta}(t)\right] i(t) \tag{14}$$

$$P_{con,D}(t) = \left[V_D + R_D i(t)\right] i(t) \tag{15}$$

V_T and R_T are on-state voltage and the resistance of the MOSFET respectively. β is a constant dependent on the MOSFET characteristics. V_D and R_D are on-state voltage and the resistance of the diode respectively. To calculate the conduction losses, it is required to specify the number of MOSFETs, $N_T(t)$, and diodes, $N_D(t)$, existing in the current mode of operation. It is clear that the number of on-state switches is dependent on the current mode of operation and time-variant. The average of the conduction losses is calculated by,

$$P_{con} = \frac{1}{\pi}\int_0^{\pi}\left(N_T(t)\times P_{con,T}(t) + N_D(t)\times P_{con,D}(t)\right)\mathrm{d}(\omega t) \tag{16}$$

To evaluate the switching losses, the linear approximation of the current and voltage during switching periods is considered. Based on these assumptions, the energy losses during the turn-on period of power switch are calculated by [29] [30],

$$E_{on,J} = \int_0^{t_{on,J}} v(t)i(t)\mathrm{d}t = \int_0^{t_{on,J}} \left[\frac{V_{sw,J}}{t_{on,J}}\times t\right]\left[\frac{-I}{t_{on,J}}\times\left(t - t_{on,J}\right)\right]\mathrm{d}t \tag{17}$$

$$E_{on,J} = \frac{1}{6}V_{sw,J}\times I_J \times t_{on,J} \tag{18}$$

where, $E_{on,J}$ is the turn-on loss of the J^{th} switch; $t_{on,J}$ is the turn on time of the J^{th} switch and I is the current through the switch after turning on. I'_J is the current through the switch after turning off. To formulate the energy loss during the turn-off process is calculated by,

$$E_{off,J} = \frac{1}{6}V_{sw,J}\times I'_J \times t_{off,J} \tag{19}$$

The total switching loss depends on the number of switching per cycle. The average switching loss (P_{sw}) can be evaluated by,

$$P_{sw} = 2\times f\left[\sum_{J=1}^{N_{sw}}\left(\sum_{i=1}^{N_{on,J}} E_{on,Ji} + \sum_{i=1}^{N_{off,J}} E_{off,Ji}\right)\right] \tag{20}$$

where, f is the fundamental (line) frequency; $N_{on,J}$ and $N_{off,J}$ are the number of turn-on and turn-off of the J^{th} switch during one half cycle of the fundamental frequency. $E_{on,Ji}$ and $E_{off,Ji}$ are the energy losses of the J^{th} switch during i^{th} turn-on and turn-off respectively.

The total loss (P_t) of the inverter is calculated by,

$$P_t = P_{con} + P_{sw} \tag{21}$$

Once the total loss is determined, the relative inverter efficiency of the inverter is calculated by,

$$\%\eta = \frac{P_{\text{out}}}{P_t + P_{\text{out}}}\times 100 \tag{22}$$

To evaluate the output voltage waveform quality, the values of total harmonic distortion (THD) are calculated as suggested in the IEEE standard 519. THD of the output voltage can be evaluated by,

$$\text{THD} = \frac{1}{V_1}\times\sqrt{\sum_{n=2}^{\infty} V_n^2} \tag{23}$$

where, V_1 and V_n are the fundamental component and harmonic component of the output voltage.

The value of weighted total harmonic distortion (WTHD) can be evaluated by,

$$\text{WTHD} = \frac{1}{V_1} \times \sqrt{\sum_{n=2}^{\infty} \left(\frac{V_n}{n} \right)^2} \tag{24}$$

Table 5 summarizes the parameters such as total harmonic distortion, weighted THD, fundamental voltage, total power loss and the conversion efficiency of the proposed 9-level inverter for various modulation indexes. The dominance of the proposed hybrid control strategy is indicated by **Table 6**.

4.2. Experimental Results

To verify the achievability of the proposed BCD topology, a hardware set-up was fabricated for a 9-level inverter with hybrid control strategy. **Figure 8(a)** shows the functional block diagram of single phase 9-level inverter. The modular MLI circuit was implemented with eight MOSFET (IRF540) switches with internal anti-parallel diodes. The isolation and driver circuit was implemented with optically coupled isolator MCT2E and eight gate driver circuits with discrete components. The carrier and reference waveforms required for PWM pulse generation were generated using an ARM® Cortex™ – M0 Core, NUC140 micro-controller. The generated PWM pulses are applied to the digital logic circuits, to produce proper switching pulses required by the proposed 9-level inverter. Optically coupled isolators provide electrical isolation between the controller and the MOSFET power circuit. The hardware layout used for a 9-level proposed inverter is shown in **Figure 8(b)**. **Table 7** summarizes the parameters used for the hardware set-up. Three asymmetrical dc sources are considered. The resistive load and inductive loads are used. Peak value of output voltage is 20 V. The RMS value of output current is 0.4 A. The power rating of the set up is 10 W. However, the proposed experimental set-up can be extended to high/medium power rating applications by including the dc sources and the semiconductor switches of suitable ratings. The 9-level output voltage waveform with hybrid modulation strategy and without modulation strategy is shown in **Figure 9(a)** and **Figure 9(b)** respectively. The output current waveform with R load is just similar to the output voltage waveform except the magnitude. The output current waveform with RL load is shown in **Figure 9(c)**. Using the proposed modular MLI, the number of levels could be increased to improve the quality of output voltage waveform by inserting more number of sub-modules. The captured output voltage waveform with 9-level stepped waveform is shown in **Figure 9(a)** which gives %THD of 11.15. It was confirmed that the output voltage waveforms were as expected and also similar to the simulation results.

5. Conclusion

In this work, BCD topology based modular multilevel inverter with hybrid control strategy was successfully de-

Table 5. Comparison of output parameters for various modulation indexes.

M_f	M_a	%THD	%WTHD	V_{o1} in pu	P_t in pu	%η
26	1.1	11.22	0.883	1.05	0.113	88.72
26	1.05	10.9	0.779	1.06	0.151	84.9
26	1	12.05	0.694	1.002	0.198	80.23
26	0.95	14.6	0.596	0.95	0.279	72.15
26	0.9	15.38	0.648	0.9	0.352	64.82
26	0.85	16.05	0.615	0.86	0.414	58.59
26	0.8	16.5	0.594	0.8	0.49	50.96

Table 6. Comparison of output parameters for various modulation techniques.

Modulation Technique	%THD	V_{o1} in pu
Presented in [21]	14.5	1.00
Presented in [31]	12.66	1.09
Phase opposition disposition PWM	12.9	1.01
Hybrid control strategy	10.9	1.06

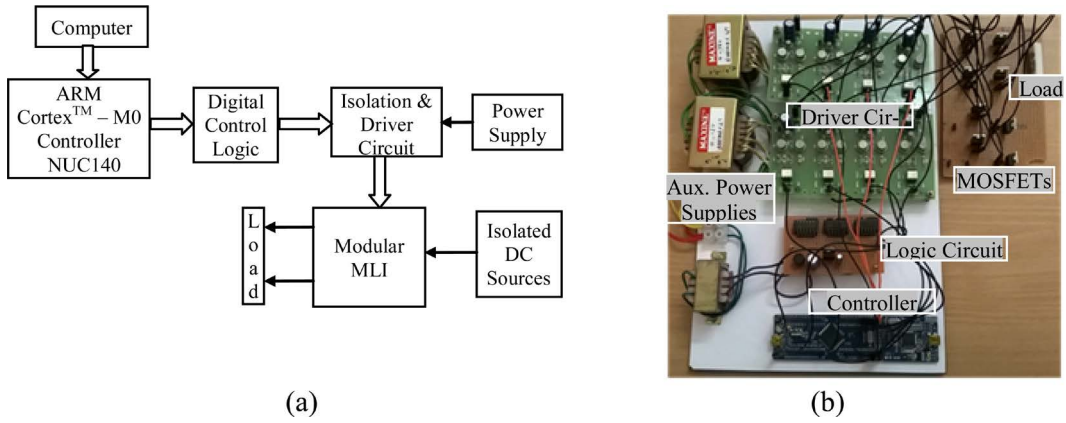

Figure 8. Hardware set-up of 9-level inverter (a) Functional block diagram (b) Test rig.

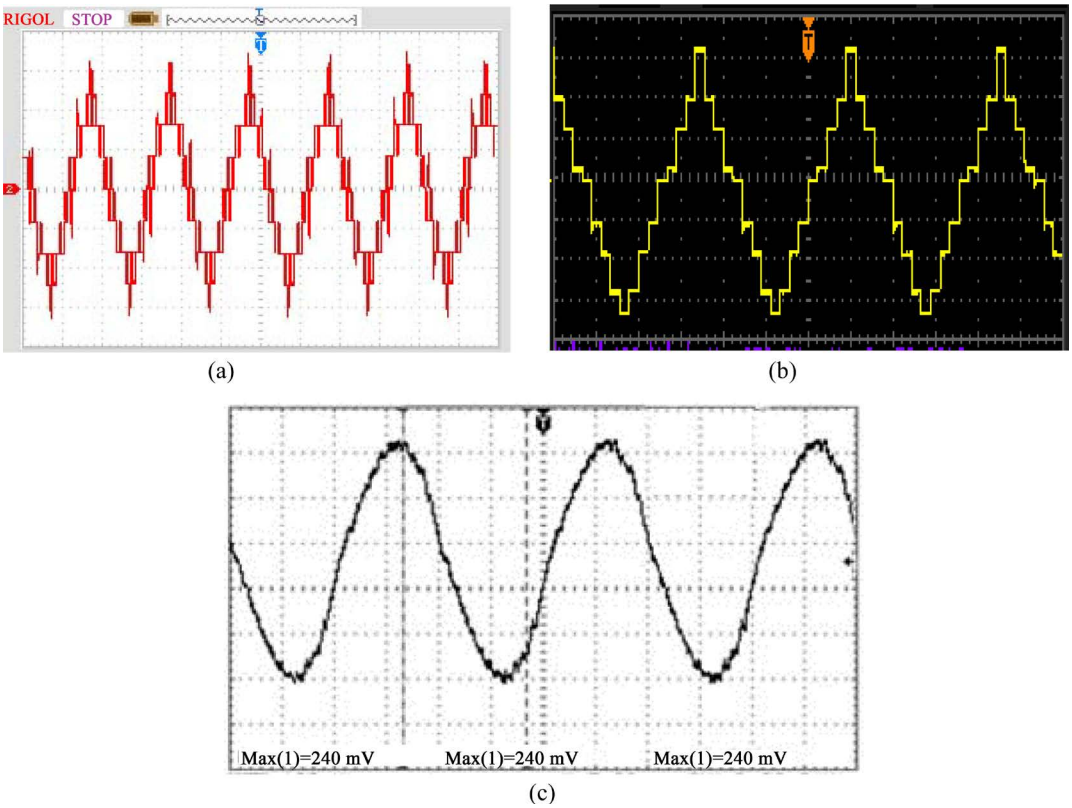

Figure 9. (a) Output voltage waveform hybrid modulation (X-axis 1 cm = 10 ms, Y-axis 1 cm = 5 V) (b) Output voltage waveform without modulation (X-axis 1 cm = 5 ms, Y-axis 1 cm = 5 V) (c) Output current waveform (X-axis 1 cm = 5 ms, Y-axis 1 cm = 0.1 amps).

Table 7. Parameters used in experimental setup.

Parameter	Value
No. of Levels	9
Input DC Sources	$V_1 = V_2 = 5$ V, $V_3 = 10$ V
No. of Switches	8
Type of switch	MOSFET (IRF540)
Type of controller	ARM® Cortex™-M0 NUC140

veloped. To demonstrate the superiority of the proposed topology, several comparisons were made between the developed proposed inverter topology and the other topologies that the literature cites. From the comparisons it could be seen that the proposed topology required less number of power switches, driver circuits, and dc sources than the topologies reported in the literature. The proposed inverter topology needed minimum number of components, could promise better performance, reliability, efficiency and reduction in cost and size of the inverter when we went for the higher number of output levels. Finally, the performance of the proposed inverter with hybrid control strategy was demonstrated with the experimental results obtained through a 9-level inverter.

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