

Leakage Analysis of a Low Power 10 Transistor SRAM Cell in 90 nm Technology

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Abstract

In this paper, a novel 10 Transistor Static Random Access Memory (SRAM) cell is proposed. Read and Write bit lines are decoupled in the proposed cell. Feedback loop-cutting with single bit line write scheme is employed in the 10 Transistor SRAM cell to reduce active power consumption during the write operation. Read access time and write access time are measured for proposed cell architecture based on Eldo SPICE simulation using TSMC based 90 nm Complementary Metal Oxide Semiconductor (CMOS) technology at various process corners. Leakage current measurements made on hold mode of operation show that proposed cell architecture is having 12.31 nano amperes as compared to 40.63 nano amperes of the standard 6 Transistor cell. 10 Transistor cell also has better performance in terms of leakage power as compared to 6 Transistor cell.

Keywords

SRAM, Transmission Gate, Subthreshold Leakage, Gate Leakage, Read Access Time, Write Access Time

1. Introduction

Static Random Access Memory (SRAM) is a vastly used circuit in modern integrated chips. SRAM chips find applications in caches, register files, First In First Out (FIFO) buffers, battery operated mobile platforms such as Personal Digital Assistant (PDA), cell phone, Radio Frequency Identification (RFID) tag, hearing aid, defibrillator, iPod, Smartcard, Smart Phone, Smart Pen etc. SRAM constitutes more than half of chip area and more than half of the number of devices in modern designs. Scaling of the process technology has improved integration density and device performance, but in turn led to increased power consumption, particularly the consump-

tion of leakage power. Lowering the supply voltage is one of the most straightforward and effective ways to suppress energy consumption because reducing the supply voltage could reduce the dynamic power quadratically and leakage power. Subthreshold operation holds promise for ultra-low power operation of these emerging applications. Due to scaling of device dimensions, random variations in Process, Supply Voltage and Temperature (PVT) poses major challenges to the high performance circuits and system design [1]-[3]. The random fluctuations are much pronounced in smallest-geometry devices usually used in area-constraint circuits such as SRAM cells [7]. The intrinsic fluctuations are independent of the transistor location on a chip. The static (leakage) power consumption of CMOS devices has created undesirable effects on technology scaling as both supply voltage (V_{DD}) and threshold voltage (V_{th}) are scaled [1]. Several new low leakage architectures SRAM cells have been proposed [4]-[10].

This work analyses standard 6 Transistor (6T) and Proposed 10 Transistor (10T) SRAM cells and compares various SRAM design metrics. In standby mode SRAM cells are inactive, but consume power for data retention due to various leakage components and this is called as leakage power. This paper investigates leakage power consumption and leakage current comparison at 90 nm technology node. It presents an analysis of read access time, write access time due to the impact of process corners at different supply voltages. The analysis shows that the proposed 10T SRAM cell outperforms standard 6T SRAM cell with respect to most of its design metrics.

2. Standard 6T SRAM Cell

In the standard 6T SRAM cell, M3 and M4 are access transistors. M1 and M5 forms left inverter. M2 and M6 form right inverter. Differential Bit Lines Bit Line (BL) and Bit Line Bar (BLB) are connected to the access transistors M4 and M3 respectively. The more stable the cell is during a read operation, the more difficult is to write the data into the cell. Due to this problem, 6T cell cannot be scaled without parametric and yield loss. **Figure 1** shows the schematic diagram of the 6T SRAM cell. The Lengths of all the six transistors are maintained at 100 nm. The Width of the transistors M3, M4, M5, M6 transistors are maintained at 0.15 μm or 150 nm. The Width of the transistors M1, M2 are at 0.35 μm or 350 nm.

Rigorous increase in threshold voltage fluctuation in short channel devices is caused by global and local process variations. Due to this problem, 6T SRAM cell and its variants cannot be operated at reduced supply voltages without parametric and functional failure causing yield loss. Single-ended 6T SRAM cell [11] suffers from write delay. Write assist circuits are required for proper operation of 6T cell. It fails to perform reliably at a low voltage due to the read disturbance formed by the voltage division between the access transistors and the pull-down transistors. Strict constraints on the sizing of the access transistors and pull-up transistors are required for ensuring data stability and the write operation.

3. Proposed 10T SRAM Bit Cell and Its Principle of Operation

Several Read-decoupled and single ended SRAM cell architectures have been proposed in [12]-[15]. These architectures ensures low power operation, but failed to improve read and write delay considerably. Novel 10T SRAM cell architecture is proposed for low leakage operation with reduced read and write delay.

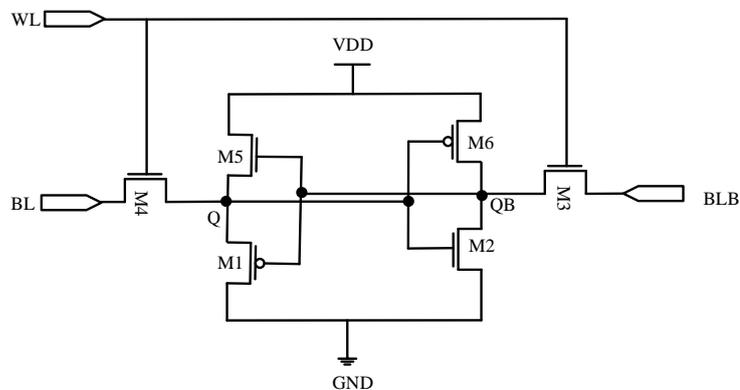


Figure 1. Schematic diagram of standard 6T SRAM cell.

3.1. Single Bit Line Write Scheme with Feedback Loop Cutting

Single Bit line Write Scheme with Feedback Loop-Cutting is used to reduce the write active power consumption and improve the write ability. When the cell is in the write “1” mode, the Write Word Line (WWL) is activated and Write Word Line Bar (WWLB) is deactivated and the Word line (WL) signal remains low. Further, M2 and M1 are turned off and the content of the Write Bit Line (WBL) is transferred through M6 and M9 to the storage node Q. During the entire write operation, the storage nodes do not suffer any disturbance because the positive feedback loop of the cross-coupled inverter pair is cut off by M2 and M1, consequently enlarging the write margin. The voltage of storage node Q reaches strong “1” or “0” due to the use of a transmission gate formed by PMOS (M9) and NMOS (M6) transistors thereby enhancing write ability of the cell. After the WWL turns off, the cell enters into the hold mode. The cell performs write/read operations through only one bit line, thereby decreasing the leakage and active power consumption. **Figure 2** shows the schematic diagram of the proposed 10T SRAM.

3.2. Single Bit Line Read Scheme

For performing read operation, the Read Bit line (RBL) is charged to VDD. When the cell enters into read mode, the Read Word line (RWL) turns higher, Read Word line Bar (RWLB) turns lower and the WL signal turns lower. The stored data is transferred to the bit line through M5, M10 and M4. The dedicated read port momentarily decouples the read path from the storage nodes, enabling a nondestructive read operation since, M1 is turned off. Readability of the proposed cell is enhanced as strong “1” or “0” is read out due to the use of a transmission gate formed by NMOS (M5) and PMOS (M10) at the read path. Data “1” is stored in the node Q and data “0” is stored in the node QB. The read buffer of the proposed cell is made stronger by enlarging the width of the transistors.

4. Simulation Results and Discussions

4.1. Read Access Time

The read access time or read delay is estimated from the point when Read Word Line (RWL) is activated to the time Read Bit line (RBL) is discharged to 50% point from its initial high level. Read Access time of the proposed cell is analyzed at various process corners by storing “1” at Q and “0” at the node QB of 10T cell. Process Corners represent the extremes of the parameter variations within which a circuit that has been etched onto the wafer must function correctly. There are therefore five possible process corners: Typical-Typical (TT), Fast-Fast

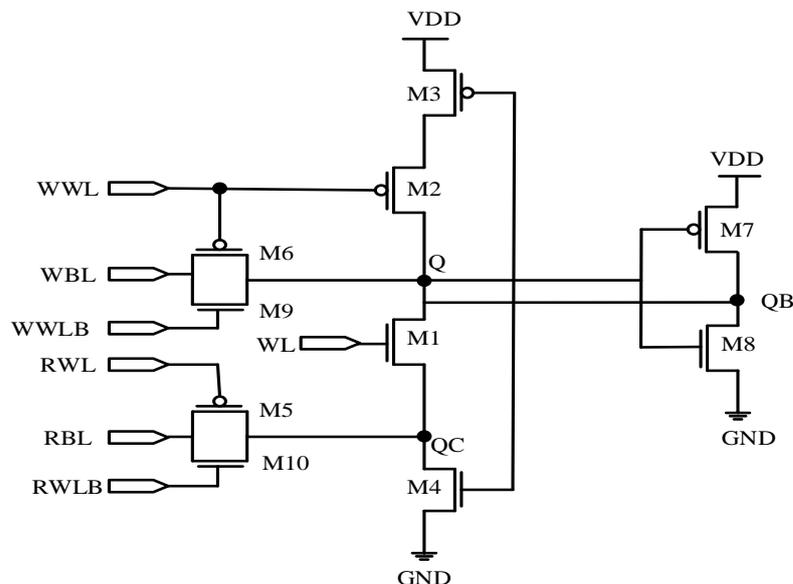


Figure 2. Schematic diagram of proposed 10T SRAM cell.

(FF), Slow-Slow (SS), Fast-Slow (FS), and Slow-Fast (SF). The first three corners (TT, FF, and SS) are called even corners; because both types of devices are affected evenly, and generally do not adversely affect the logical correctness of the circuit. In TT corner, both PMOS and NMOS devices switch faster. In SS corner, both PMOS and NMOS devices switch slower. In TT corner, both PMOS and NMOS devices switch at a moderate speed.

Figure 3 shows read access time of the proposed 10T SRAM cell (Read “1” & “0” operation) at different supply voltage of 1 V, 0.5 V and 0.2 V for various process corners. At 0.2 V, FF corner has better read “1” access time of 2.2 ns when compared with TT, FS corner which have 2.4 ns and 2.3 respectively. As the supply voltage reduces, read “1” access time of 10T cell increases. FF corner is having lesser read “1” delay at the simulated voltage ranges. SS corner is having higher read “1” delay than other corners at all the simulated voltages. At 0.2V, SS corner has read “1” access time of 5.2 ns when compared with SF corner which has 4.9 ns.

At 0.2 V, FF corner has better read “0” access time of 1.8ns when compared with TT, FS corner which both have 2.5 ns. As the supply voltage reduces, read access time of 10T cell increases. FF corner is having lesser read “1” delay at the simulated voltage ranges. SS corner is having 3.8 ns read “0” delay at 0.2 V. For Read “0” and “1” operations, FF corner is better than all other corners and SS corner is having higher read access time at the different voltage ranges.

4.2. Write Access Time

The write access time or write delay is estimated at the time required for writing “0” at storage node “QB” from the point when WL reaches 50% of its full swing (from its initial low level) to the point when “QB” falls to 10% of its initial high level (*i.e.*, its 90% swing). Similarly, write access time for writing “1” at “QB” is estimated from the point when WL reaches 50% of its full swing (from its initial low level) to the point when “QB” rises to 90% of its full swing from its initial low level. **Figure 4** shows the write access time of the proposed 10T SRAM cell (Write “1” & “0” operation) at different supply voltage of 1 V, 0.5 V and 0.2 V for various process corners.

4.3. Leakage Current Components of 6T SRAM Cell

The leakage current is the most important donor to the power consumption in the SRAM cell in the subthreshold regime. The total leakage current in an SRAM cell mainly consists of the subthreshold leakage current (I_{sub}), the gate leakage current (I_{gate}) and the reverse-biased drain-and source-substrate junction band-to-band tunneling (I_{BTBT}) or Junction leakage current ($I_{junction}$) through different transistors [1].

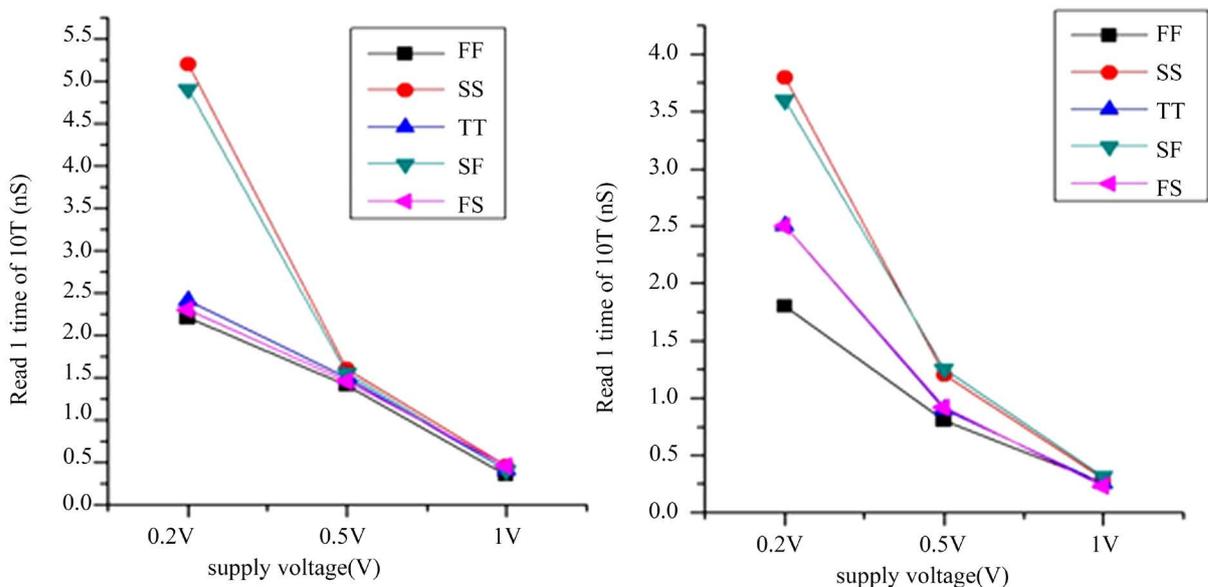


Figure 3. Read access time for 10T SRAM cell (Read “1” and “0” operation) for various process corners at different supply voltages.

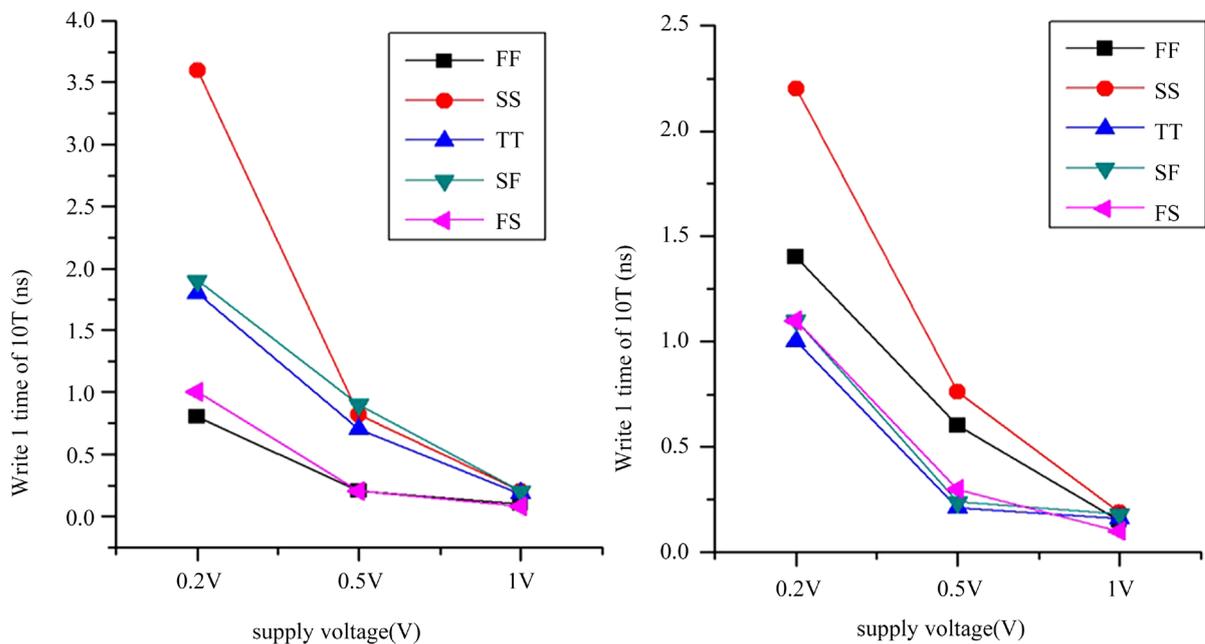


Figure 4. Write access time for 10T SRAM cell (Read “1” and “0” operation) for various process corners at different supply voltages.

Figure 5(a) and **Figure 5(b)** shows the subthreshold and gate leakage current components of the 6T SRAM cell respectively. Subthreshold leakage current is absent in M3 transistor and is maximum in M4, M1 and M2 transistors. I_{GIDL} and $I_{punch-through}$ are the minor contributors and hence neglected. $I_{junction}$ is negligible in terms of Femto Amperes and so it is not included in the calculation of the leakage current. Gate Leakage current is maximum at M3 and M4 transistor and is negligible in M5 transistor and M6 transistor. All the leakage measurements are made in the hold mode of operation of 6T SRAM cell by storing $Q = “1”$ and $QB = “0”$ at a supply voltage of 0.3 V.

4.4. Leakage Current Components of Proposed 10T SRAM Cell

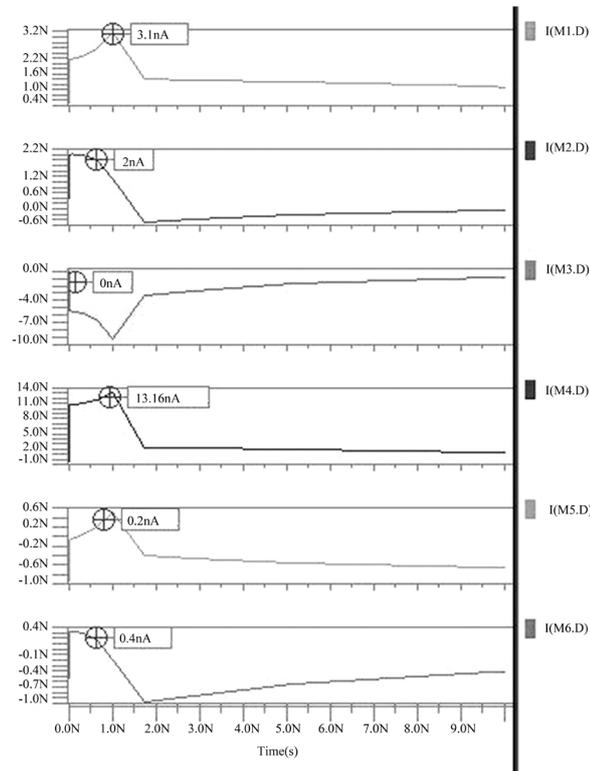
Figure 6 and **Figure 7** shows the subthreshold leakage currents and gate currents in the proposed 10T SRAM cell respectively. Subthreshold leakage current is high for M4 and M10 transistors and it is negligible in all other transistors. Gate leakage current is absent in M4, M5 and M10 transistors and is maximum in M7 transistor.

The leakage currents flowing through the transistors depend on the value stored in the cell. Leakage current of conventional 6T and 10T are measured during the HOLD mode of operation. Junction leakage current is negligible and insensitive to temperature variations and is not considered for leakage analysis. Simulations are carried at 27°C. All the with supply voltage of 0.3 volt by storing $Q = 1$ and $QB = 0$. All the simulations are carried using TSMC based 90 nm CMOS technology using Typical-Typical (TT) process corner for leakage current measurement.

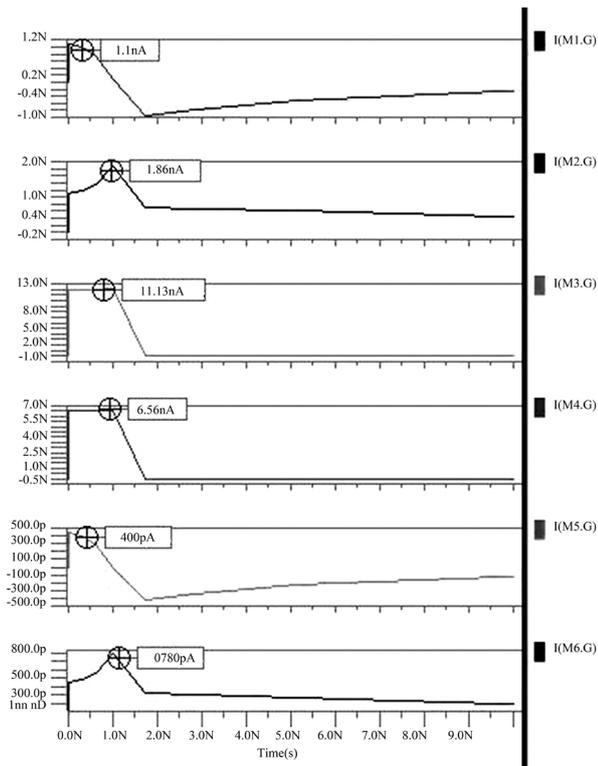
Junction leakage current is negligible in terms of Femto Amperes and is not taken for the leakage comparison. **Table 1** shows that the proposed 10T SRAM cell has reduced sub-threshold leakage of 5.48 nanoamperes as compared to 18.86 nanoamperes of the conventional 6T cell. There is a substantial improvement in the gate leakage current of the proposed 10T cell which is reduced to 6.83 nanoamperes from 21.77 nanoamperes as that of the standard 6T cell.

4.5. Hold or Data Retention Power

The leakage power or the data retention power or hold power is the power consumed due to the above mentioned leakage currents. Hold power is measured as a voltage of $VDD = 1$ V and 0.5 V. Leakage power of proposed 10T cell has improved by 81% at a supply voltage of 1 Volt and by 54% at a supply voltage of 0.5 Volt as compared to standard 6T cell. **Table 2** provides the hold power comparison of 6T and 10T.



(a)



(b)

Figure 5. (a) Subthreshold leakage current (I_{sub}); (b) Gate Leakage current (I_{gate}) in Conventional 6T SRAM cell at $V_{DD} = 0.3$ V.

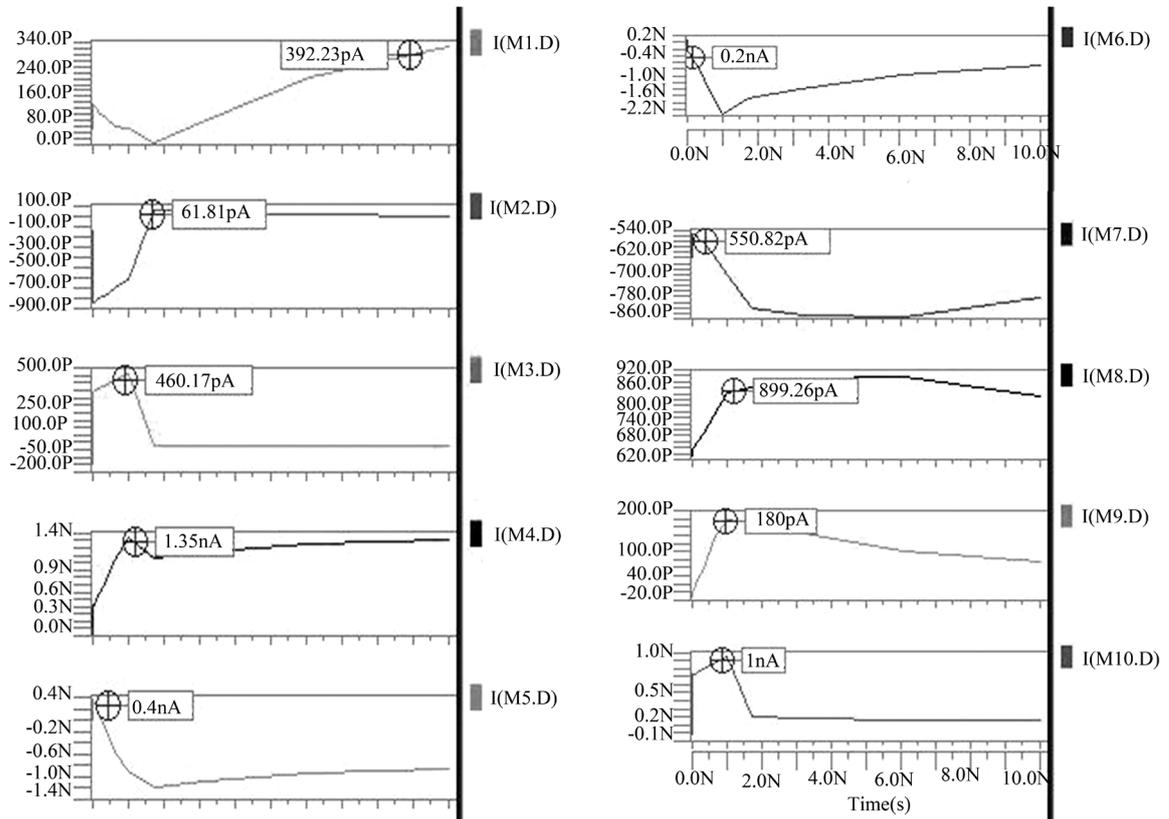


Figure 6. Subthreshold leakage current (I_{sub}) in the proposed 10T SRAM cell at $V_{DD} = 0.3$ V.

Table 1. Leakage currents in 10T SRAM cell (in Hold mode) at a temperature of 27°C ($V_{DD} = 0.3$ V and node $Q = 1$, $QB = 0$).

| Transistors | Type of Leakage current | Standard 6T SRAM cell | Proposed 10T SRAM Cell |
|-----------------------|-------------------------|-----------------------|------------------------|
| M1 | I_{sub} (nA) | 3.1 | 0.39 |
| | I_{gate} (nA) | 1.1 | 0.05 |
| M2 | I_{sub} (nA) | 2 | 0.06 |
| | I_{gate} (nA) | 1.86 | 1.18 |
| M3 | I_{sub} (nA) | 0 | 0.46 |
| | I_{gate} (nA) | 11.13 | 0.005 |
| M4 | I_{sub} (nA) | 13.16 | 1.35 |
| | I_{gate} (nA) | 6.5 | 0 |
| M5 | I_{sub} (nA) | 0.2 | 0.4 |
| | I_{gate} (nA) | 0.4 | 0 |
| M6 | I_{sub} (nA) | 0.4 | 0.2 |
| | I_{gate} (nA) | 0.78 | 0.6 |
| M7 | I_{sub} (nA) | - | 0.55 |
| | I_{gate} (nA) | - | 4.02 |
| M8 | I_{sub} (nA) | - | 0.89 |
| | I_{gate} (nA) | - | 0.39 |
| M9 | I_{sub} (nA) | - | 0.18 |
| | I_{gate} (nA) | - | 0.58 |
| M10 | I_{sub} (nA) | - | 1.0 |
| | I_{gate} (nA) | - | 0 |
| Total I_{sub} (nA) | | 18.86 | 5.48 |
| Total I_{gate} (nA) | | 21.77 | 6.83 |
| Total Leakage (nA) | | 40.63 | 12.31 |

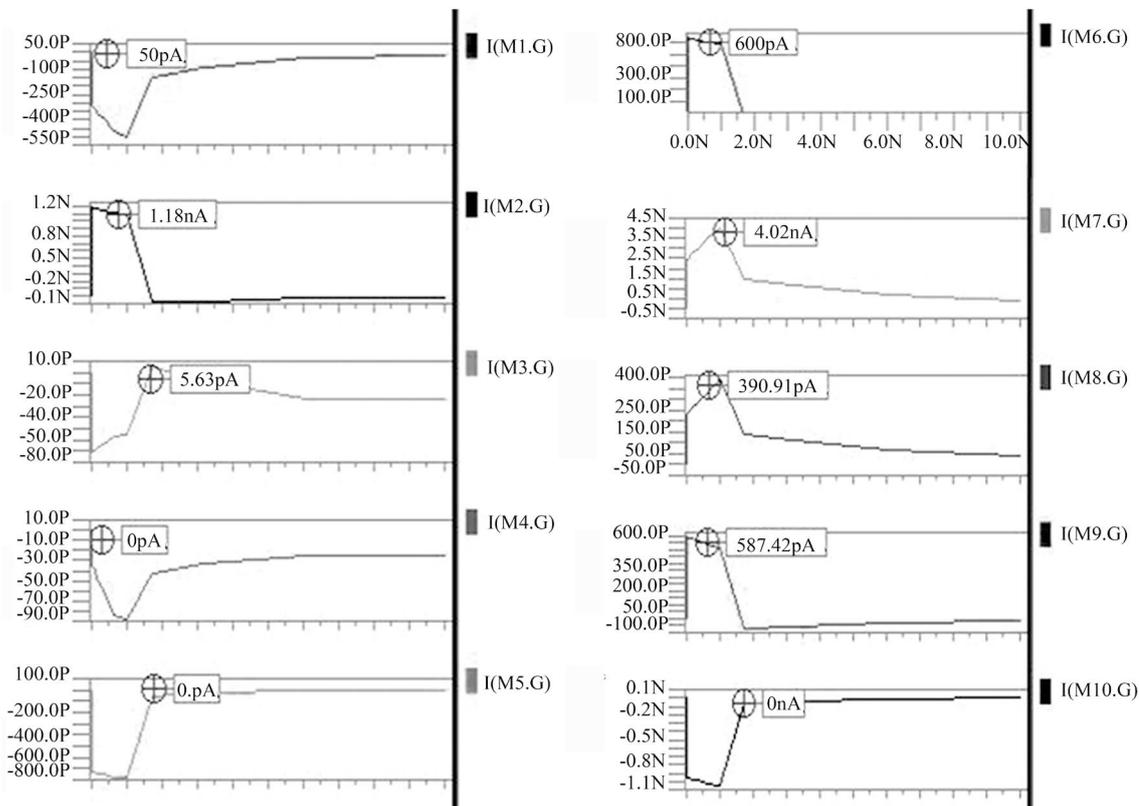


Figure 7. Gate leakage current (I_{gate}) in the proposed 10T SRAM cell at $V_{DD} = 0.3$ V.

Table 2. Hold power 6T and 10T SRAM cell at a temperature of 27°C ($V_{DD} = 0.3$ V, $V_{DD} = 1$ V and node Q = 1, QB = 0).

| Supply Voltage (Volt) | Hold Power while Q = 1 and QB = 0 (Watt) | SRAM Cell Topology |
|-----------------------|--|------------------------|
| 1 V | 3.4×10^{-8} | Standard 6T SRAM cell |
| 1 V | 0.92×10^{-8} | Proposed 10T SRAM cell |
| 0.5 V | 0.65×10^{-8} | Standard 6T SRAM cell |
| 0.5 V | 0.42×10^{-8} | Proposed 10T SRAM cell |

5. Conclusion

A single ended Transmission Gate based 10T SRAM cell is proposed. Read delay and write delays are measured at all the process corners. Read delay is less in Fast-Fast corner and found to be high in Slow-Slow corner from the simulations at varying supply voltages. Write delay measurements at different process corners show that write delay is less in Fast-Fast corner for write “1” and less in Typical-Typical corner for write “0” operations. The detailed leakage analysis is done on standard 6T and proposed 10T SRAM cell during the hold mode operation at a supply voltage of 0.3 V. Subthreshold leakage current being the major contributor to the total leakage is reduced by 71% in the proposed cell, when compared to 6T cell. Gate leakage also reduced 68% as compared to that of 6T cell. So it can be concluded that 10T SRAM cell is better as compared to 6T SRAM cell in terms of leakage current and leakage power with little area overhead of extra four transistors.

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