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A Process Variation Tolerant OTA Design for Low Power ASIC Design

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Abstract

Technology development and continuous down scaling in CMOS fabrication makes Mixed Signal Integrated Circuits (MSIC) more vulnerable to process variation. This paper presents a well defined novel design methodology for process variability aware design by incorporating the major challenge of statistical circuit performance relating the device and circuit level variation in an accurate and efficient manner to improve the reliability, robustness and stability of the circuit. The device sensitive parameters are identified and accurately quantified by continuous realistic assessments using statistical methods. The modularity of the methodology can be validated by the output performance obtained from the gain and phase response of OTA which is highly stable when subjected to worst case process variation scenario. In the proposed optimization, the circuit is strengthened by fixing the optimum aspect ratio without adding any additional compensation devices complicating the circuit resulting in low power consumption of only 0.116 mW in standard CMOS 0.18 µm technology with 1.8 V power supply.

Keywords

MSIC, Process Voltage Temperature, Operational Transconductance Amplifier, Monte Carlo Simulation

1. Introduction

Large demand of high performance CMOS mixed signal systems requires stable output performance independent of power supply, process and temperature variations. With the technology development and supply voltage reduction impact of process variation, parameters are more dominant in low power battery operated electronic systems. Highly accurate and high precision stable OTA driving large capacitive loads are used as error amplifiers in low-voltage low-drop-out (LDO) regulators [1]-[3]. Due to constraints on the minimization of design time

and die area/cost, efficient circuit developments with design reuse and/or technology migration methodologies have been developed for principle analog blocks, such as operational transconductance amplifiers (OTAs), comparators, LNAs and so on [4]. Despite its popularity, only uncompleted design procedures were proposed for this OTA which arbitrarily reduced the degree of freedom in the design equations, hence precluding the possibility to meet optimized performance. Indeed, the approach proposed in [5] sets arbitrarily the compensation capacitor equal to the load capacitor, and that presented in [6] introduces constraints that require an onerous recursive procedure. With the scaling down of device sizes and supply voltages, single-stage cascode or telescopic amplifiers are not suitable for high-gain wide-bandwidth amplifiers. A low-power low-area and frequency-compensated multistage amplifier capable of driving large capacitive loads is a necessity. OTA [7]-[12] required a robust frequency compensation scheme due to their potential closed-loop stability problems. In an OTA, the ratio of transconductance to current consumption reflects the power efficiency. In order to obtain lower power, the efficiency of the OTA must be improved. In addition with the scaling of the supply voltages, the reduction of the threshold voltage is not aggressive, which limits signal swings. In recent years, the process variation parameters of the MOSFET have become a dominant cause in variation affecting the stability of the circuit. Therefore, OTAs generate large distortion when produced by the present manufacturing process. Many design methodologies have been developed to optimize the design of OTA's. In this paper, a new methodology is adopted to design the OTA and hence satisfies the state of art design specification.

2. Challenges in Statistical Optimized Design Methodology

The major challenge of statistical circuit performance analysis is how to relate the device-level variation to the circuit-level variation in an accurate and efficient manner. Two conventional approaches for simulating the impact of device variation on circuit performance are as follows: 1) corner-model method and 2) Monte Carlo (MC) SPICE simulation [14]. The corner method is simple, computationally efficient, and thus widely adopted by circuit designers. However, the corner approach usually gives overly pessimistic or optimistic performance prediction due to insufficient attention to the quantitative correlations between the corner models and the circuit performance variations. The MC SPICE provides more accurate prediction using statistical information but is computationally expensive for complex VLSI circuits. In addition, the accuracy of the MC approach depends on the accuracy of the variations of the SPICE model parameters. The latter accuracy can be improved with greater attention paid to the ET variation data [15]. Principal component analysis (PCA) was introduced to capture the complex correlations of device parameters [16]. PCA transforms the correlated device parameters into uncorrelated variable (principal component). Each device parameter is a linear or nonlinear combination of the principal components. There is no physical interpretation of these principal components. However, the accuracy of PCA can be problematic in nanoscale CMOS technology due to highly nonlinear device characteristics and heterogeneity of device parameter [17]. To overcome this issue, an ET-based direct sampling methodology (DSM) extracts device model parameters for all test sites and preserves the existing complex nature of parameter correlations [17] [18]. DSM can predict more accurate distribution of circuit performance due to stochastic process variations. However, the accuracy of the DSM relies on the number of generated device parameter sets. The more generated parameter sets lead to more accurate predicted results. The efficiency of the device parameter extraction for significant number of test sites could be problematic due to a more complex process introduced in the advanced CMOS technology. Backward propagation of variance approach was introduced to model the process variations based on physical process parameters and the propagation of the variance. The model is efficient and general for all kinds of variability studies. However, the model requires a very accurate nominal SPICE model card with correct sensitivities to different process parameters. In addition, the model does not account for nonlinearities of the sensitivity, which could lead to inaccurate results when variations are large. The improved set of model parameter variations will directly improve the accuracy of MC circuit simulations. Furthermore this paper proposes a systematic optimized methodology that correlates the corner model approach and montecarlo simulation. This paper presents a methodology to develop a variability aware computationally compact parameter set for the parameters that impact on the sensitivity of the device parameter.

3. The Principle of Approach

Process variations can be incorporated in the design of OTA by considering the worst case condition as shown in **Table 1** under a desired level of confidence. Instead of choosing a minimal or the nominal value, optimal

Table 1. Worst case corner conditions for typical, slow and fast transistors [M5].

Parameters	Typical	Slow	Fast
Threshold Voltage V_{th} (mV)	499.9	590.88	408.92
Temperature (˚C)	27	−40	125
Supply Voltage V_{dd} (V)	1.8	1.6	2
On current I_{on} (µA)	243.862	207.287	279.45
Off current I_{off} (µA)	12.9356	3.8806	51.74
Width W (µm)	3.25	3.84	2.65
Length L (nm)	500	480	570

values have to be chosen by incorporating various methodologies. In this paper an OTA is designed considering the process sensitive parameter in the design. The proposed optimization design flow is shown in **Figure 1**. The optimal value of the process sensitive parameter is chosen such that the values are not allowed to be greater than the worst case value (*i.e*. the degradation in performance is allowed to be greater than the maximum acceptable). For simplicity threshold voltage variation and drain current variation is described in this paper. Initially to model circuit process variability is modeled by worst case corner models for OTA as shown in **Table 1** are generated from slow nMOS and slow pMOS (SS) to model the worst-case delay (WS), and from fast nMOS and fast pMOS (FF) to model the worst-case power (WP); whereas, the corner models for digital applications are generated from fast nMOS and slow pMOS (FS) to model the worst-case "1", (WO) and from slow nMOS and fast pMOS (SF) to model the worst-case "0" (WZ). A standard set of model parameters {e.g. V_{th}, W, L, T_{ox}, μ_{eff}, γ, R_{bs}, C_{ov}, C_j} is used to account for process variability and model the worst-case corner performance of devices and circuits.

Threshold Voltage Mismatch (VTH)

The threshold voltage V_{th} is mainly determined by process variation dependent sensitive parameters {V_{th}, W, L, T_{ox}, μ_{eff}, γ, R_{bs}, C_{ov}, C_j}, whose effect strongly dominates over the intrinsic imbalance at nominal conditions. This clearly shows that variations are very critical in ULP/ULV mixed signal standard CMOS circuits. Since the performance of the device changes drastically with PVT associated parameters. To model the threshold voltage V_{th}, the standard deviation (σ) limits are preset to include any process variability over a wide range. The worst case corner models are generated by offsetting the selected compact model parameter (P) of the typical (TT) compact model by $\pm dp = n\sigma$ to account for a window of process variability, where n is the number of σ for P so that it is selected to set the upper and lower limits. The corner models of BSIM4 TT model parameter V_{th0} is defined as

$$V_{th} = V_{th0} + dv_{th} \tag{1}$$

where dv_{th} is used to set the fixed UL and LL of the models. The variation of threshold voltage ΔV_{th} due to global and local mismatch is calculated and the variance $\sigma_{\Delta v_{th}}$ is determined.

$$\sigma_{Vth} \cong C \cdot \left(\sqrt[4]{q^3 \varepsilon_{Si} \varnothing_B} \right) \frac{T_o}{\varepsilon_o} \left(\frac{\sqrt[4]{N_{CH}}}{\sqrt{W_{eff} L_{eff}}} \right) \tag{2}$$

where C is a constant and is given by 0.8165 [19] or 0.7071 [20] with or without the dopant variation along the depth of the channel region, respectively; q is the electronic charge, ε_{Si} and ε_{ox} are the permittivity of silicon and silicon-dioxide (SiO_2), respectively; $\varphi_b = 2k_B Tin\left(\frac{N_{CH}}{n_i}\right)$ is the bulk potential of the channel region of MOSFETs with k_B, T, and n_i are the Boltzmann constant, absolute temperature, and intrinsic carrier concentration, respectively. W_{eff} and L_{eff} represent the effective dimension of W and L, respectively. The impact of v_{th} on device scaling as shown in **Figure 2**.

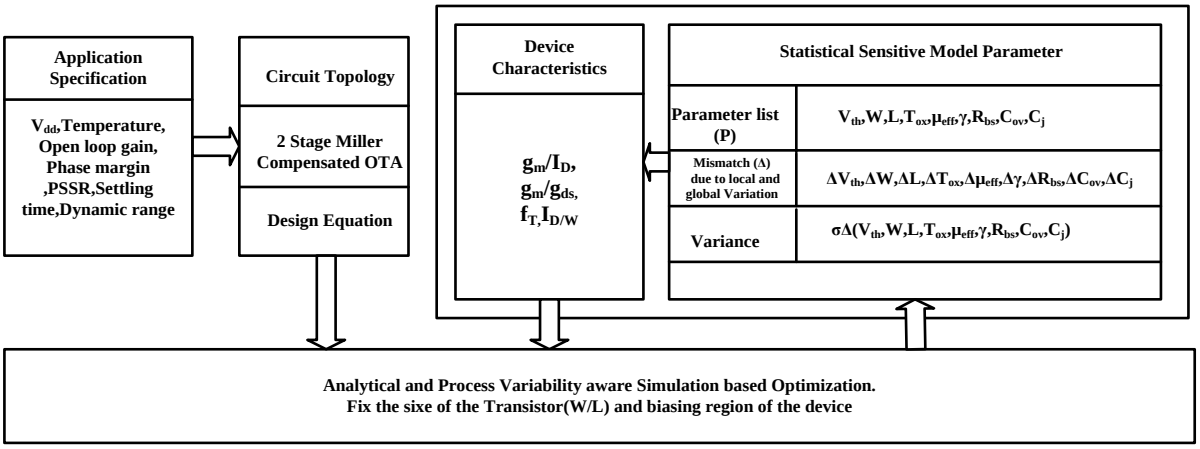


Figure 1. Proposed design optimization flow for OTA considering Worst case (PVT) scenario.

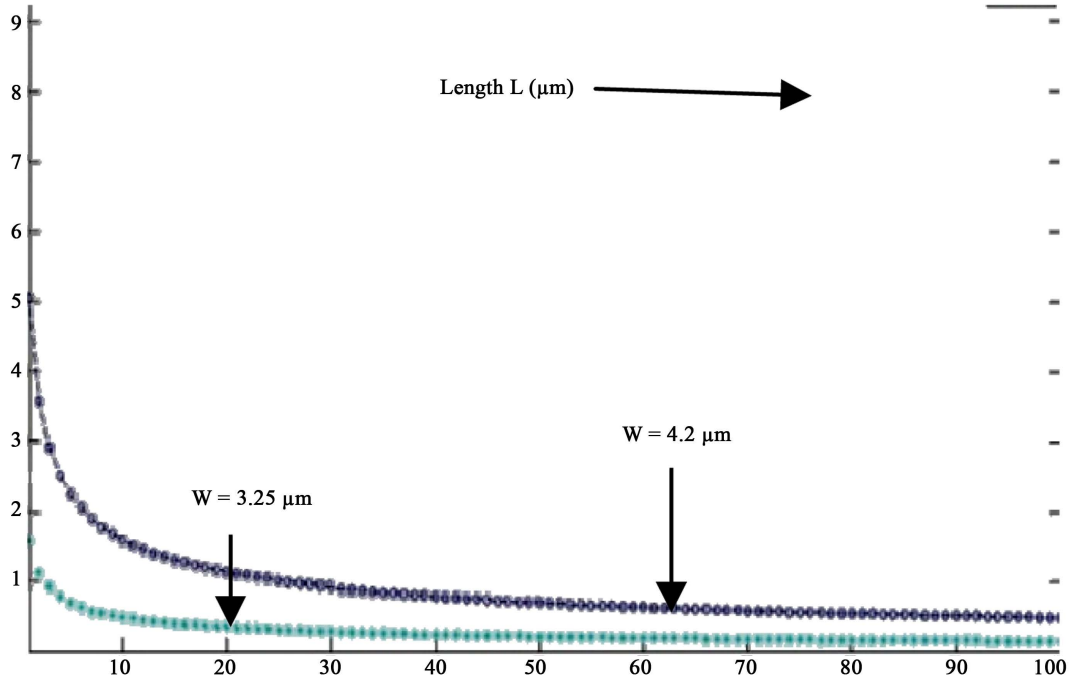


Figure 2. Estimated V_{th} variation for variation in width W = 3.25 µm and 4.2 µm.

Normal distribution $N\left(0,\sigma_{\Delta M_{mismatch}}\right)$, where $\sigma_{\Delta M_{mismatch}} \cong A_m/\sqrt{WL}$ [20]-[22]. A_m is the technology dependent constant of ΔM. Thus for threshold voltage model V_{th0}, the variance of ΔV_{th0} between two transistor is given by $\sigma_{\Delta V_{th0}} \approx A_{V_{th}}/\sqrt{WL}$, where $A_{V_{th}}$ is an area dependant constant of ΔV_{th0}, depends on ΔXW, ΔXL, ΔT_{ox}, ΔU_0 and ΔK_1. Now for a single device we get

$$\sigma_{M_{mismatch}} = \frac{1}{\sqrt{2}}\sigma\Delta M_i = \frac{A_m}{\sqrt{2}\sqrt{WL}} \tag{3}$$

where $\sigma_{M_{mismatch}}$ is the variance of ΔM due to process variability. Thus the variance of ΔV_{th0} is given by

$$\sigma_{V_{th0\,mismatch}} = \frac{1}{\sqrt{2}}\frac{A_{V_{th}}}{\sqrt{WL}} \tag{4}$$

Thus the model parameter M including both local and global process variability components is given by

$$M = M_0 + \sigma M_{mismatch} + n\sigma M_{global} \quad (5)$$

Equation (5) is the generalized compact model of the target technology for process variability aware analysis. Thus for compact model parameter V_{th} is given by

$$V_{th} = V_{th0} + \sigma V_{th0,mismatch} + n\sigma_{Vth0,global} \quad (6)$$

This Equation (6) is used to build a statistical corner model for threshold voltage V_{th} realistic analysis of process variability. Similar method is adopted for all the sensitive parameters in the design. Montecarlo simulations are made for 200 runs and the histogram of V_{th} for M_5 is shown in **Figure 3**. The mean and standard deviation of the parameter is observed, compared with the value and scattered plot is obtained as shown in **Figure 4**. The optimized value is validated with Equation (6) and optimized.

4. Proposed Optimized Ota Design Flow Considering the Worst Case Scenario

General methodology adopted for process variation insensitive design

1) Select transistor gate length from intrinsic gain plat, so that the designed OTA satisfies the required gain.
2) Determine the transconductance g_m to realize the OTA's required frequency response. Analytical expression for the transfer function and settling behavior must be derived for a specific topology.

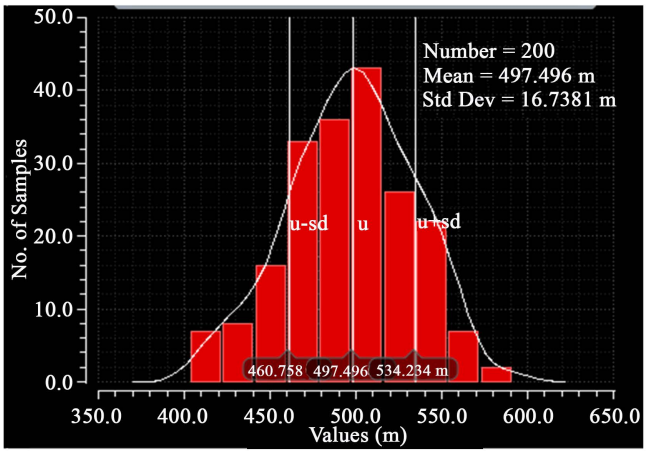


Figure 3. Histogram for V_{th} variation representing the mean and standard deviation.

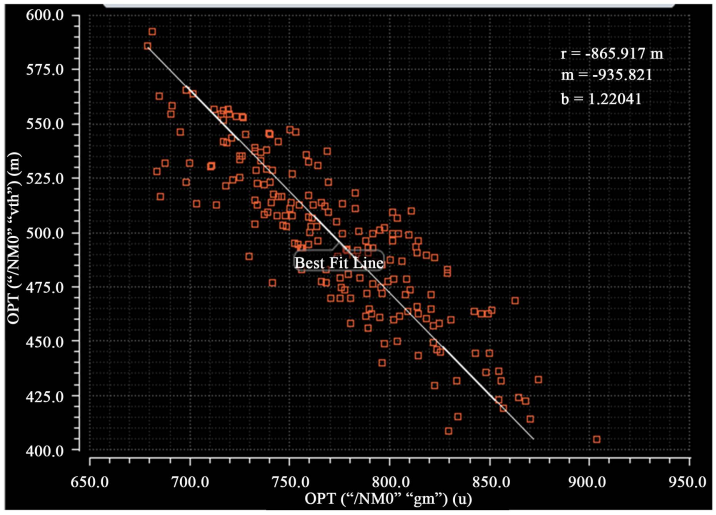


Figure 4. Scatter plot representing G_m and V_{th} over all corners.

3) Optimize g_m/I_{DS} to meet the required specification. Once g_m/I_{DS} (intrinsic gain) is determined, F_T, C_{gg} and the associated parasitic capacitors can be obtained from the statistical variation sensitive model parameter look-up table developed.
4) Determine I_{DS} from g_m and g_m/I_{DS}.
5) The mismatch in the relative drain current $\Delta I_{DS}/I_{DS}$ is calculated. The variance of the relative drain current including global and local mismatch is derived.
6) Relative drain current mismatch $\Delta I_{DS}/I_{DS}$ is calculated by including the variation sensitive compact model parameter set $\{V_{th0}, W, L, C_{ox}, \mu_{eff}, \gamma, R_{DS}, C_{ov}, C_j\}$.
7) The process variability sensitive model parameter is included and optimized I_{DS} is calculated.
8) Determine the transistor gate widths W from the calculated IDS and current density plot.

OTA Design Optimization Flow

1) Determine the value of the total capacitance including the global and local variability sensitive compact model parameter, with overlap capacitance C_{ov} {CGSO, CGDO, CGSL AND CGDL}; {CJS, CJD} defining the source to drain junction area capacitance; and {CJSWS, CJSWD, CJSWGS, CJSWGD} defines the source to drain junction sidewall capacitance.
2) Determine the variance of the model parameter and add it to the mean value to analyze the change in value of the parameter.
3) Determine the gate length from the DC requirements and optimize g_m/I_{DS} for the output of the optimized OTA design.
4) Optimize the circuit parameters [V_{th}, W, L, T_{ox}, μ_{eff}, γ, R_{bs}, C_{ov}, C_j] of the OTA with an iteration loop until the variation in output is tolerable to the change in variation sensitive parameter.
5) Optimize the bias currents and fix the region of transistor to satisfy the reqired design specification.
6) Determine the gate width (W_{eff}) of the transistor to be used in amplifier design.
7) Repeat the above process for each transistor in the design.

5. Design Approach

Generally the design of OTA can be divided into two distinct design related activities that are most port independent of one another. The tail current transistor for the differential amplifier will only consume voltage thus reducing the output swing. The first of these activities involves choosing or creating basic structure for the op-amp. Once the structure has been selected, the designer must select dc current and begin to size the transistors and design the compensating circuit. Most of the work involved in completing a design is the second activity of the design process. Note that the devices must be properly scaled in order to meet all the ac and dc requirements imposed on the top. Before designing the OTA one must sort out all the requirements and boundary conditions that will be required to guide the design flow.

5.1. Analysis and Design of DC Gain

The overall gain of the OTA is given by

$$A_v = A_{v0} \cdot \frac{\left(1-\frac{s}{z}\right)}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)} \tag{7}$$

$$A_{v0}\left(DC\ gain\right) = \left[g_{m1,2}\left(r_{02} \parallel r_{04}\right)\right]\left[g_{m6}\left(r_{06} \parallel r_{07}\right)\right] \tag{8}$$

where A_{v0} is the DC gain of the OTA, g_m is the trans conductance of the MOS, r_0 is the effective output impedance. The design procedure begins by choosing a device length to be used throughout the circuit. In general in designing analog circuit we normally avoid channel-length modulation. Therefore the chosen length $L > L_{\min}$. From the minimum value for the compensation capacitor C_c, such that placing the output pole p_2 2.2 times higher than the GB permitted a 60˚ phasemargin. Therefore the pole and zero placements results in the following requirement for the minimum value for $C_c > 0.22C_L$. Next determine the minimum value for tail currents I_5

known as bias current. Based on slew rate (SR) requirements the value of I_5 is determined to be $I_5 = SR \times C_c$. The requirement of the transconductance of the input transistor can be determined from the quantified value of C_c and GB. The transconductance $g_{m1,2}$ can be calculated using the following. $g_{m1,2} = GB \times C_c$. The range of input value needed such that the transistors are designed to be in saturation. The two limitations on the input range are.

$$\text{CMR} + V_{in(\max)} = V_{DD} - \sqrt{\frac{I_5}{\mu_n C_{ox}\left(\frac{W}{L}\right)_3}} - \left|V_{T3}\right|_{(\max)} + V_{T1(\min)} \tag{9}$$

$$\text{CMR} - V_{in(\max)} = V_{SS} - \sqrt{\frac{I_5}{\mu_n C_{ox}\left(\frac{W}{L}\right)_3}} + V_{T1(\min)} + V_{DS5(\text{sat})} \tag{10}$$

5.2. Tuning of Aspect Ratio

The aspect ratio of the transistor M_1, M_2 is $\left(\frac{W}{L}\right)_{1,2}$ is directly obtained from $g_{m1}\left(\frac{W}{L}\right)_{1,2} = \frac{g_{m1,2}^2}{\mu_n C_{ox} I_5}$. The aspect ratio of M_3 and M_4 are found from the positive CMRR $V_{in(\max)}$ such that M_1 to be in saturation.

$$\left(\frac{W}{L}\right)_{3,4} = \frac{I_5}{\mu_p C_{ox}\left[V_{DD} - V_{in(\max)} - \left|V_{T3}\right|_{(\max)} + V_{T1(\min)}\right]^2} \tag{11}$$

If the value determined for $\left(\frac{W}{L}\right)_{3,4}$ is less than one, then it should be increased to a value that minimizes the product of *W* and *L*. This gate capacitance contributes to the mirror pole which may cause degradation in phase margin. From the datas available calculate the saturation voltage of transistor M_5. Using the negative ICMR equation, calculate V_{DS5} using the following relationship.

$$V_{DS5} = V_{in(\min)} - V_{SS} - \sqrt{\frac{I_5}{\mu_n C_{ox}\left(\frac{W}{L}\right)_3}} - V_{T1(\min)} \tag{12}$$

If the value of V_{DS5} is less than about 100 mV, then the possibility of a large $\left(\frac{W}{L}\right)_5$ may result. This may not be acceptable if the value for V_{DS5} is less than zero, then the ICMR specification may not be too stringent. To solve this problem, I_5 can be reduced or $\left(\frac{W}{L}\right)_1$ increased. The aspect Ratio of $\left(\frac{W}{L}\right)_5$ is given by $\left(\frac{W}{L}\right)_5 = \frac{2I_5}{\mu_n C_{ox}\left[V_{DS5}\right]^2}$. At this point; the design of the first stage of the op-amp is complete.

For a phase margin 60˚, the location of the output pole was assumed to be placed at 2.2 times GB. Based on this assumption and the relationship for pole 2. The transconductance g_{m6} can be found $g_{m6} = 2.2 g_{m1,2}\frac{C_L}{C_c}$. generally, for reasonable phase margin, the value of g_{m6} is approximately ten times the input stage transconductance g_{m1}

$$\left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_4 \cdot \frac{g_{m6}}{g_{m4}} \tag{13}$$

Knowing the g_{m6} and $\left(\frac{W}{L}\right)_6$ will be defined the dc current

$$I_6 = \frac{g_{m6}^2}{2\mu_p C_{ox}\left(\frac{W}{L}\right)_6} \tag{14}$$

Noting that one must now check to make sure ha the maximum output voltage specification is satisfied. Finally the device size of M_7 can be determined from the balance equation $\left(\frac{W}{L}\right)_7 = \left(\frac{W}{L}\right)_4 \cdot \frac{I_6}{I_5}$. The first-cut design of all $\frac{W}{L}$ ratios is now complete.

5.3. Small Signal Analysis of OTA

In analog circuit designs, the small signal model is widely used to analyze the behavior of analog circuits. To ensure the accuracy of the model, we must verify the small signal model with CMOS circuit. In order to achieve simplicity without losing of accuracy, the intrinsic part of complete small signal equivalent circuit of CMOS transistor, has been applied in the small signal model. The verification of the small signal model is illustrated by a CMOS two-stage OTA shown in **Figure 1**. The conventional small signal model of CMOS amplifier is widely used based on the hybrid-pi model of CMOS transistor shown in **Figure 5**. In the hybrid-pi model, the Gate-Source capacitor (C_{gs}) and Gate-Drain capacitor (C_{gd}) have not been considered. The capacitor C_{gs} can be neglected while the voltage V_{GS} is an ideal voltage source. In the two stage OTA, the input voltage V_{in} connects to M_1 and M_2 is generally assumed to be the ideal voltage source in the small signal model. Thus, the Gate-Source capacitor of M_1 can be ignored in the small signal model. The Gate-Drain capacitor C_{gd1} of NMOS input differential pair M_1 and M_2 is connected to input voltage V_{in} and cannot be ignored.

The Gate-Source capacitor of M_6, C_{gs6}, must be considered in the small signal model since V_{GS6} is not an ideal voltage source. The Gate-Drain capacitor of M_6, C_{gd6}, is connected to the output node V_{out}. Thus, capacitor C_{gd5} will affect the circuit performance of the two-stage OTA and cannot be ignored in the small signal model. The complete small signal equivalent circuit of CMOS transistor has been discussed in [6]. In order to achieve simplicity without losing of accuracy, the intrinsic part of complete small signal equivalent circuit of CMOS transistor, has been applied in the modified model. Therefore, the modified small signal model of the two-stage OTA can be obtained as shown in **Figure 6**. The modified model contains three parasitic capacitors C_{gd1}, C_{gs5}, and C_{gd5} compared to the conventional model. In order to achieve simplicity without losing of accuracy, the intrinsic part of complete small signal equivalent circuit of CMOS transistor, has been applied in the small signal model. The nominal value of the parasitic capacitors C_{gd1}, C_{gs6}, and C_{gd6}, can be obtained from the SPICE simulations of the two stage OTA shown in **Table 2**.

Table 2. Optimized parameters of transistor.

Device	W/L	Gm μA/V
M_1	1.4/0.5	67.25
M_2	1.4/0.5	67.25
M_3	4.5/0.5	52.10
M_4	4.5/0.5	52.10
M_5	3.25/0.5	157.10
M_6	55.5/0.5	596.32
M_7	10/0.5	840.36
M_8	3.25/0.5	157.10

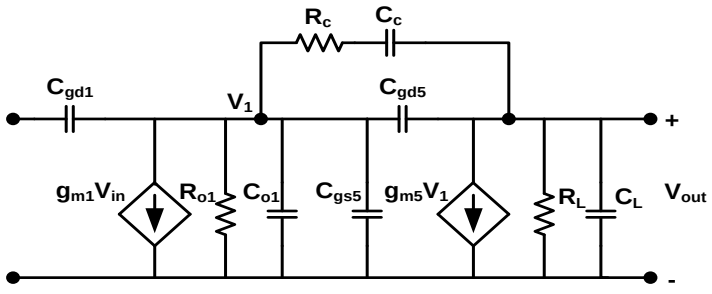


Figure 5. Small signal model of OTA.

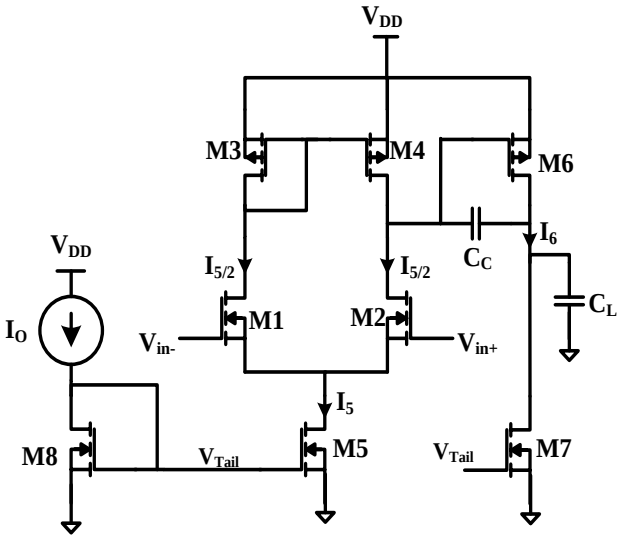


Figure 6. Schematic of OTA.

5.4. Miller Compensation Technique

This technique is applied by connecting a capacitor from the output to the input of the second transconductance stage g_{m11}. Two result came from adding the compensation capacitor C_c. First, the effective capacitance shunting R_1 is increased by the additive amount of approximately $g_{m11}R_{11}C_c$. This moves P_1 closer to the origin of complex frequency plane by a significant amount. Second, P_2 is moved away from the origin of the complex frequency plane, resulting from the negative feedback reducing the output resistance of the second stage.

From the simplified model

$$V_1 = \frac{V_o sC_c R_1 - g_{m1}R_1 V_{in}}{1 + sR_1\left[C_1 + C_c\right]} \tag{15}$$

$$V_o\left[s\left[C_H + C_c\right] + \frac{1}{R_2}\right] = V_1\left[sC_c - g_{m11}\right]$$

The overall transfer function that results

$$\frac{V_0}{V_{in}} = \frac{\left[g_{m1}\cdot R_1\right]\left[g_{m11}\cdot R_2\right]}{s^2\left[R_1R_2\left(C_1C_{11} + C_1C_c + C_{11}C_c\right)\right] + s\left[R_2\left(C_c + C_{11}\right) + R_1\left(C_c + C_1\right) + C_c g_{m11}R_1R_2\right] + 1} \frac{\left[1 - \frac{sC_c}{g_{m11}}\right]}{}$$

From the standard second order system

$$\frac{V_0}{V_{in}} = A_{DC} \cdot \frac{\left(1-\frac{s}{z}\right)}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)} \tag{16}$$

where $A_{DC} = g_{m1}R_1 \cdot g_{m11}R_2$ is the DC gain of OTA, $R_1 = \left(r_{ds2} \parallel r_{ds4}\right)$ $R_2 = \left(r_{ds6} \parallel r_{ds7}\right)$. For the stability reason the pole $P_2 \gg P_1$

$$P_1 = \frac{1}{R_2\left(C_c + C_{11}\right) + R_1\left(C_c + C_1\right) + C_c g_{m11} R_1 R_2} \tag{17}$$

Since $C_c g_{m11} R_1 R_2$ is very large value Equation (17) is reduced to $P_1 \cong \frac{1}{C_c g_{m11} R_1 R_2}$ and $P_2 \cong \frac{C_c g_{m11}}{C_1 C_{11} + C_1 C_c + C_{11} C_c}$ since $C_{11}C_c \gg C_1 C_{11}$ & $C_1 C_c$ the pole $P_2 \cong \frac{g_{m11}}{C_{11}}$ and $z \cong \frac{g_{m11}}{C_c}$.

5.5. Phase Margin (PM)

This Phase Margin will define the stability of an amplifier. Higher value of PM will allow the output signal to achieve steady state without much ringing. Lower values will cause ringing at the output. The value of phase margin depends on the application. For most or well defined PM of 60˚ is needed

$$\frac{V_0}{V_{in}} = A_{DC} \cdot \frac{\left(1-\frac{s}{z}\right)}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)} \tag{18}$$

$$< \frac{V_0}{V_{in}} = -\tan^{-1}\left(\frac{w}{z}\right) - \tan^{-1}\left(\frac{w}{p_1}\right) - \tan^{-1}\left(\frac{w}{p_2}\right)$$

$$PM = 84.29 - \tan^{-1}\left(\frac{GBW}{p_2}\right) \tag{19}$$

For stability of OTA the phase margin $PM \geq 60^\circ$ then $P_2 \geq 2.2GBW$ for $PM \geq 5^\circ$ then $P_2 \geq 1.22GBW$ $Z \geq 10GBW$, where the Gain Bandwidth (GBW) is given by $GBW = g_{m1}/C_c$. Based in the expressions the pole P_1 and P_2 is given by $P_1 = \frac{1}{C_c g_{m11} R_1 R_2}$, $P_2 \cong \frac{g_{m11}}{C_{11}} \geq 2.2GBW$, $C_c \geq 0.22C_{11}$.

6. Simulation Results

The OTA is designed using conventional and proposed optimization methodology as shown in **Figure 6** is designed and simulated in CADENCE spectre in 180nm CMOS technology. The supply voltage of the OTA is 1.8 V. The size of the transistors is optimized and the transistor parameter together with transconductance is shown in **Table 3**.

All significant variation sensitive process parameters are varied by the optimum percentage value from their nominal values and Monte Carlo simulations for the two-stage OTA and corner analysis is made with the variation range of each circuit parameter and results are obtained model can be obtained as shown in **Table 4**. The circuit parameters are varied up to its maximum allowable value from their nominal values. By consider the variation range of each circuit parameter, the performance bounds can be evaluated by the proposed approach. It is observed that the aspect ratios of the transistors are as minimum as possible demonstrating to give stabilized response as shown in **Figure 7(c)**. **Table 4** shows a summary of the performance parameters of OTA under typical conditions. The frequency and phase response of the OTA designed with conventional and proposed me-

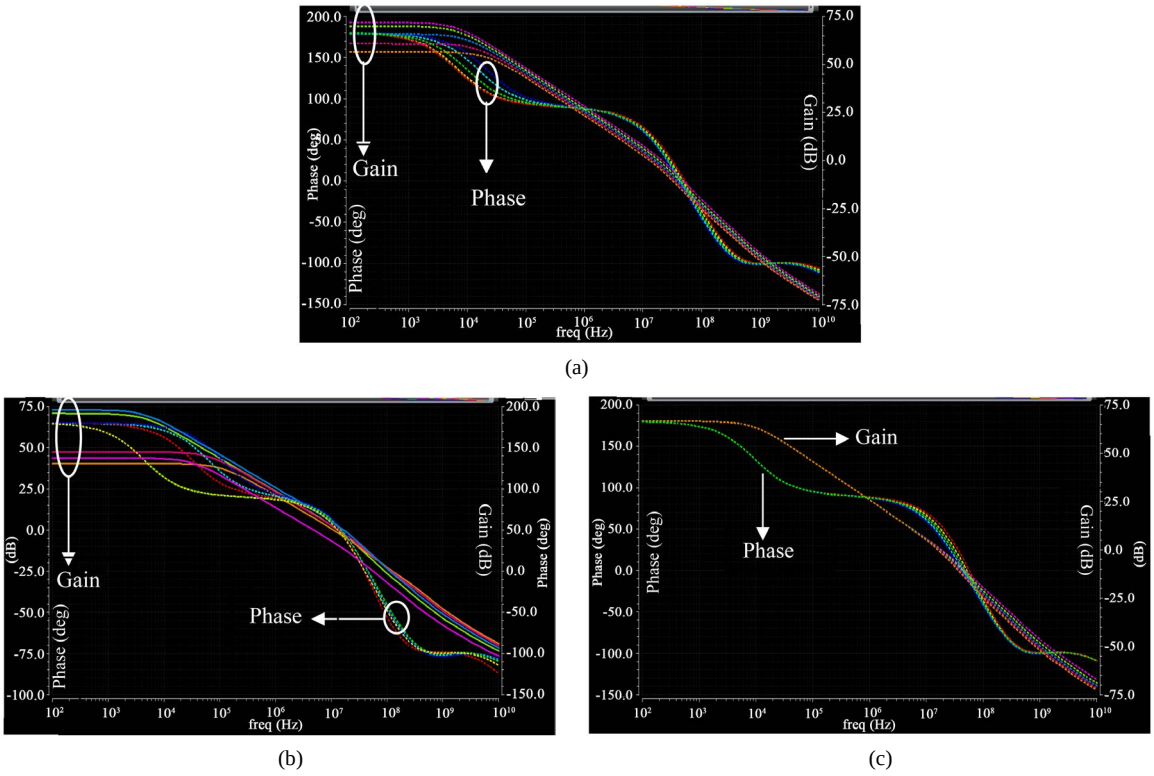


Figure 7. Frequency response of OTA (a) Conventional design with W5 variation; (b) Conventional design with temperature variation; (c) Proposed design with W5 variation.

Table 3. Optimal value of small signal parameters obtained from montecarlo analysis 200 runs.

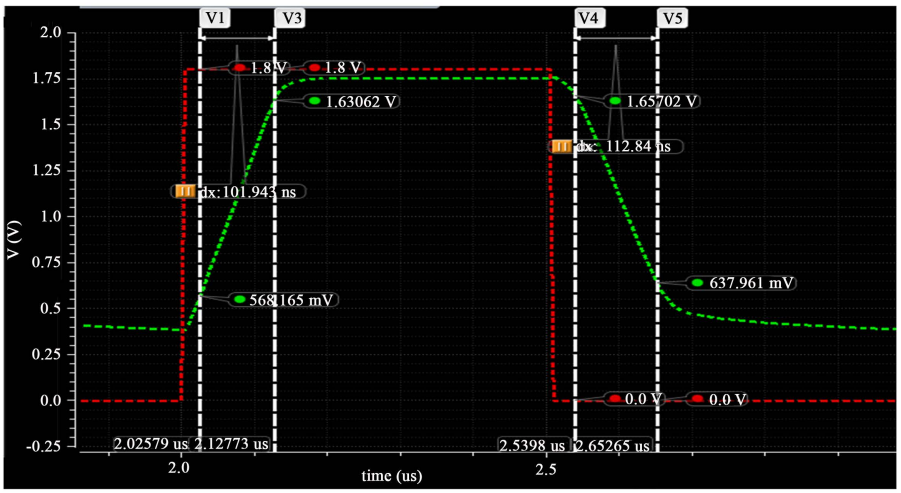
Parameters	Value	Parameter	Value
C_{gd1} (fF)	391.39	g_{m5} (μA/V)	157.10
C_c (fF)	800	C_L(pF)	2
C_{gd5} (fF)	1.28	g_{m1} (μA/V)	67.25
C_{gs5} (fF)	9.72	-	-
R_{o1} (KΩ)	752.8	C_{o1} (pF)	2.35 pF

Table 4. Simulated performance of OTA with proposed design methodology.

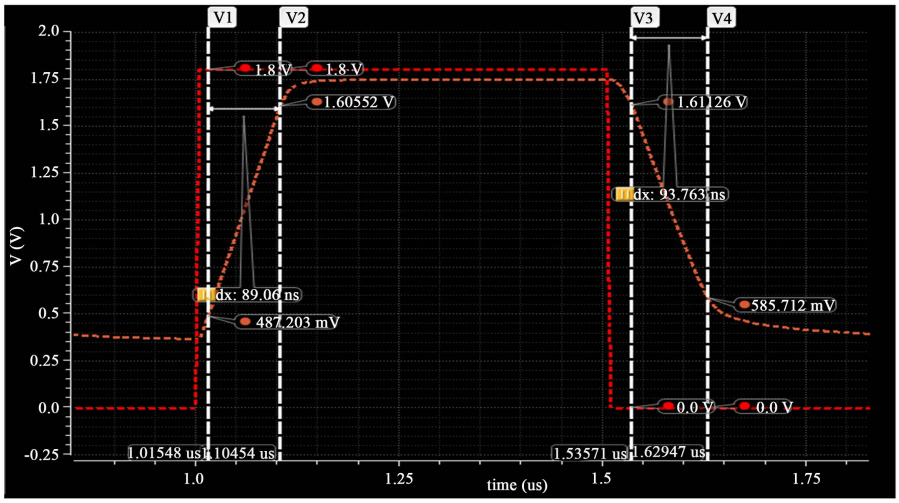
PARAMETERS	Simulated values	
Load pF	2 pF	5 pF
DC Gain (dB)	64.11	66.43
Gain Bandwidth (MHz)	21.61	16.95
Phase Margin	58.07	50.88
Slew Rate (V/μs)+ Slew Rate (V/μs)−	12.56 11.03	10.58 9.10
CMRR(dB)	68.78	65.78
PSRR (dB)	79.83	63.40
Power Dissipation	0.116 mW	0.193 mW
FOM_s MHz.pF/mW	1.25	0.65
FOM_L V/μs.pF/mW	216.55	274.09
$IFOM_s$ MHz.pF/mW	4.32	5.29
$IFOM_L$	2.512	3.30

thodology is shown in **Figure 7**. Simulated results show that the DC gain of the OTA with conventional methodology for a load of 2 pF and 5 pF is 64.11 dB and 66.43 respectively. The slewrate of the OTA is observed from the simulated response obtained from the step input as shown in **Figure 8**. **Figure 9** shows the variation of gain and phase margin of the OTA with conventional and proposed design methodology with varying width (W µm), temperature representing PVT variations. It is observed that the frequency of the OTA designed with optimized methodology is more stable than the conventionally designed. The both the OTA is simulated for the worst case corner models with the constraints as shown in **Table 1** and it is observed that the gain and phase variation more in conventionally designed OTA.

To study robustness to mismatch and process variations, montecarlo analysis with over 200 runs were performed. The results are shown in **Table 1**. **Figure 9(a)** shows the variation in gain for OTA with the conventional and proposed design methodology over all process corners. It is observed that the deviation in gain is more in conventionally designed OTA. **Figure 9(c)** shows the change in gain for the conventional and optimized OTA with varying loads. **Figure 10** shows the layout of the optimized OTA is implemented in CADENCE 0.18 µm CMOS technology thus proving the enhancement in stability of the frequency responses even under worst case mismatches and process variations. **Figure 11** depicts the comparative analysis of the power consumption by different OTA's. **Table 5** depicts the performance summary of conventionally designed OTA's with the proposed design methodology.



(a)



(b)

Figure 8. Simulated response for step input for CL (a) 5 pF; (b) 2 pF.

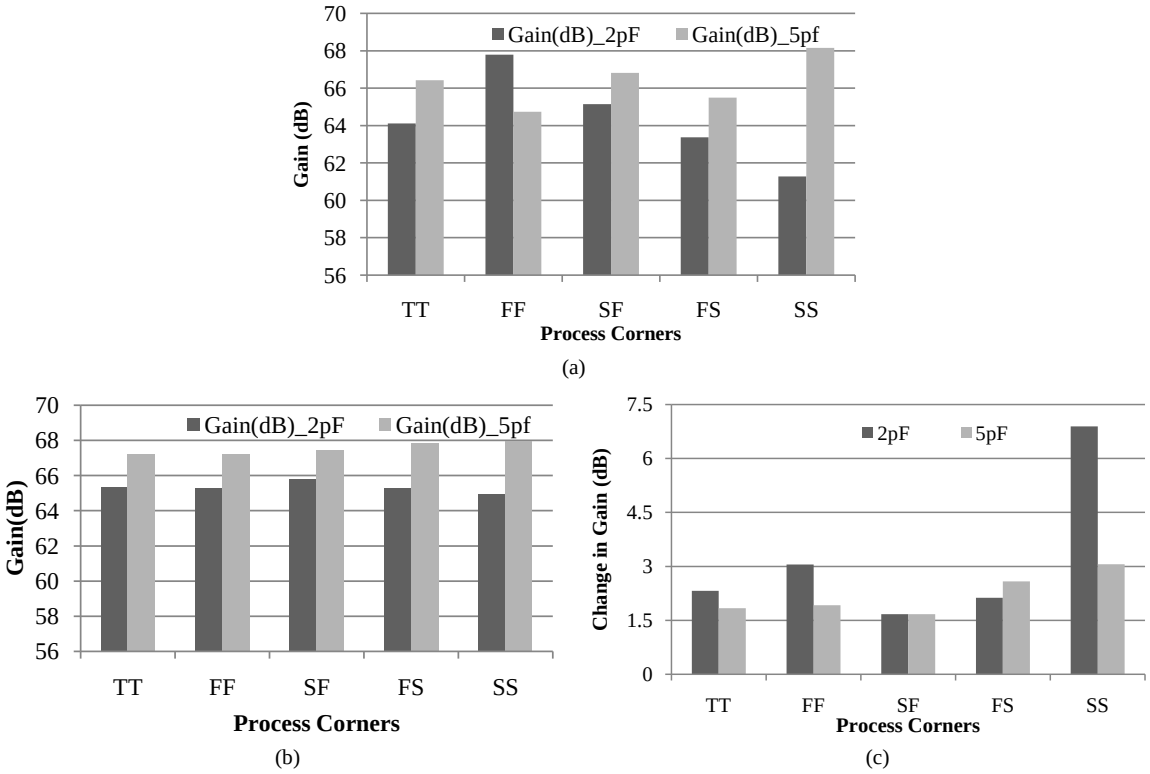


Figure 9. Variation of gain in OTA for worst case process corners (a) Conventional design; (b) Proposed design; (c) Change in gain for OTA by both conventional and proposed designs.

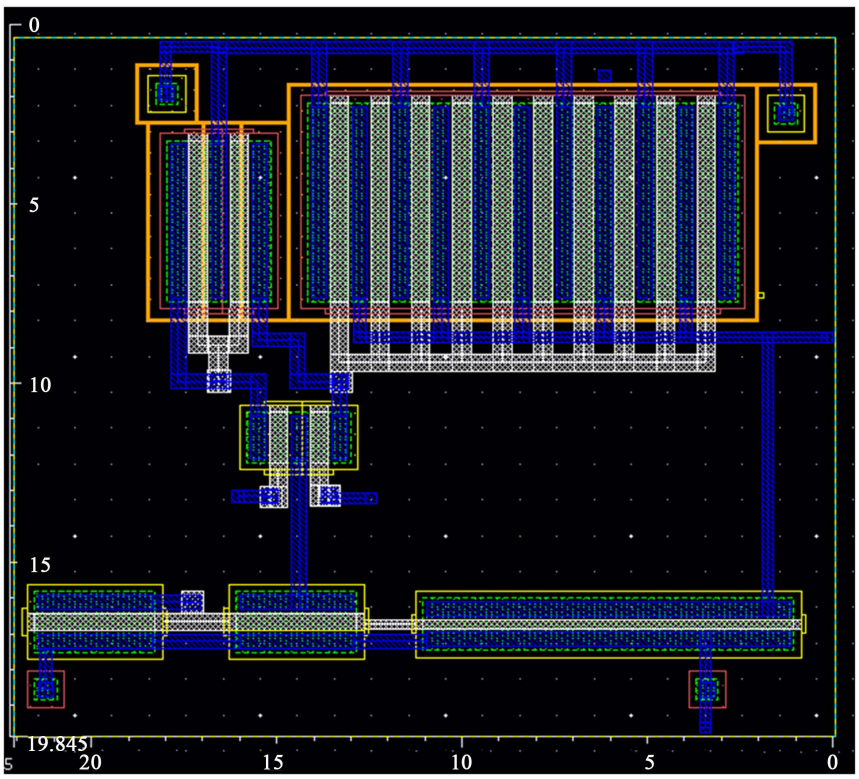


Figure 10. Layout of the optimized OTA 180 nm CMOS technology.

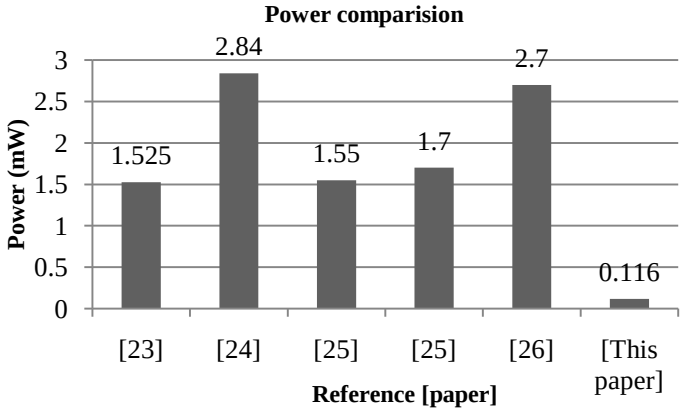


Figure 11. Power comparison of proposed optimized OTA.

Table 5. Performance summary of the OTA and comparison with recently published work.

Parameters	[13]	[23]	[25] CONV	[25] PROP	[26]	[27] OTA-A	[27] OTA-B	[27] OTA-C	[27] PROP	THIS PAPER	THIS PAPER
Technology (µm)	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.18
Supply Voltage (V)	1.0	1.8	0.9	0.9	1.5	3	3	3	3	1.8	1.8
DC gain (dB)	42	50.1	48.5	67	60	48.5	59	53.3	64.1	66.43	64.11
Phase margin	52˚	67.2˚	64˚	62˚	-	89.5˚	86.3	86.2	83.2	50.88	58.07
Load C_L	20 pF	2 nF	-	-	-	30 pF	30 pF	30 pF	30 pF	5 pF	2 pF
Power Dissipaton (mW)	1.26	1.525	1.55	1.7	2.7	-	-	-	-	0.193	0.116

7. Conclusion

This paper presents a simple and efficient design methodology to stabilize the gain and phase margin of a conventional OTA in 180 nm CMOS process subjected to process variation. An efficient methodology to evaluate the performance of the circuit considering the PVT variations is modeled. By considering the worst case design scenarios in the design a combination of analytical and simulation based circuit optimization is performed. A significant improvement in stability of the device process sensitive parameters is observed in all stages in the design. From the comparative analysis, it is identified that the OTA designed by proposed optimized methodology consumes only 23 percent of the average power consumed by different other OTA's designed by conventional methodology. The circuit simulation results confirm that the frequency response of OTA is more stabilized and this proves the superiority of the proposed design approach over all the conventional approach. From the performance metrics observed a series of comparison is made confirming the technical merits of reliability, robustness and performance enhanced characteristics using the proposed design approach.

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