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Design and Analysis of Low Power Hybrid Memristor-CMOS Based Distinct Binary Logic Nonvolatile SRAM Cell

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Abstract

Memristor is a newly found fourth circuit element for the next generation emerging nonvolatile memory technology. In this paper, design of new type of nonvolatile static random access memory cell is proposed by using a combination of memristor and complemented metal oxide semiconductor. Biolek memristor model and CMOS 180 nm technology are used to form a single cell. By introducing distinct binary logic to avoid safety margin is left for each binary logic output and enables better read/write data integrity. The total power consumption reduces from 0.407 mw (milli-watt) to 0.127 mw which is less than existing memristor based memory cell of the same CMOS technology. Read and write time is also significantly reduced. However, write time is higher than conventional 6T SRAM cell and can be reduced by increasing motion of electron in the memristor. The change of the memristor state is shown by applying piecewise linear input voltage.

Keywords

Memristor-CMOS, Nonvolatile Memory, Power Consumption, DBL, PWL Input

1. Introduction

SRAM is used as a memory element because of faster operation and better performance. However, data retention leads a main problem in SRAM since data is lost when power is switched off. The volatility characteristic of conventional SRAM rises the booting time for systems utilizing SRAM either as main memory or cache. Introduction of nonvolatile memory into the main memory or cache architectures can be an effective means to decrease booting time and energy consumption. As the technology developed, new storage capabilities are re-

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quired. Memristor-CMOS based SRAM cell can be a capable circuit component that would permit conventional SRAM cells to retain data when power is off without need of extra circuitry. A memristor is a fourth fundamental circuit element and can be used as a memory because of its nonvolatile characteristics, better scalability, higher packing density and low power consumption. It can be characterized by Loen Chua in 1971 as a fourth fundamental missing circuit component [1]. The other three basic components are resistor, capacitor and inductor. The main difference between the memristor and three fundamental circuit elements (R, L, and C) is its nonlinear input-output characteristics. In 2008, Hewlett Packard lab declared that the memristor was fabricated physically using two terminal titanium-di-oxides (TiO_2) [2]. HP lab clarified the first physical demonstration of a memristor, conforming Chua's theory [3] and flashing in the electronic industry.

Basically the memristor is a memory resistor whose resistance changes when a voltage is applied to this element and maintained on that particular value when the source is removed. It is suitable to use the name memristor to explain a "memristive device". It links magnetic flux to electric charge in similar to the resistor links voltage to current, capacitor links voltage to charge and inductor links flux to current. By exploiting memristor as storage element in a memory is a clear choice. The most emerging memory technologies, which are measured as potential replacement for Flash, DRAM and SRAM, are based on memristors. These technologies are somewhat unformed and are not yet fully commercial [4]. The ability to control and alter their current-voltage characteristics can be used for performing different computational operations. Current CMOS based memory technology looks many challenges to meet the increasing demand for refining the processing speed and higher data size. For instance, static random access memory (SRAM), the most widely used on-chip memory, is facing its physical limits in attaining higher densities and lowering power consumption. In addition, progress in using other emerging memory technologies, such as eDRAM, MRAM, PCRAM, is prohibited by their lack of compatibility with CMOS, their slow access time, and their limited scalability [5]. Memristor is a two terminal device that works in one of two nonvolatile resistive states R_{ON} or R_{OFF}. It consume less power than transistors as they do not require a minimum voltage to sense their state or need of power to retain [6].

The paper planned with introduction of memristor and modelling of memristor with nonlinear dopant drift with new parameter [7]. Then it goes directly into the structure of the proposed circuit, its working principle and its functionality. Then it confers the nonvolatile property and power dissipation of memristor-CMOS based memory cell and finally it concludes with the future views of the circuit.

2. HP Labs Model of the Memristor

The physical model of the memristor involves two-layer of thin film (size $D \approx 10$ nm) made up of TiO_2, sandwiched between platinum (Pt) contacts. The structure of model is shown in **Figure 1**. One of the layers is doped with oxygen vacancies and thus it acts as a semiconductor. The second layer is an undoped region has an insulating property. As a significance of complex material processes, the width w of the doped region is modulated depending on the amount of electric charge passing through the memristor. With electric current passing in a given direction, the boundary between the two regions is moving in the same direction.

The total resistance of the memristor R_{MEM} is a sum of the resistances of the doped and undoped regions. The relation is given in Equation (1) as follows.

$$R_{mem}(x) = R_{ON}(x) + R_{OFF}(1-x) \tag{1}$$

where, $x = w/D$ is the width of the doped region, referenced to the total length D of the TiO_2 layer, and R_{OFF} is the bound values of the memristor resistance for $w = 0$ and R_{ON} are the bound values of the memristor resistance for $w = D$. The Ohm's law is valid between the memristor voltages and current [7] as shown in Equation (2)

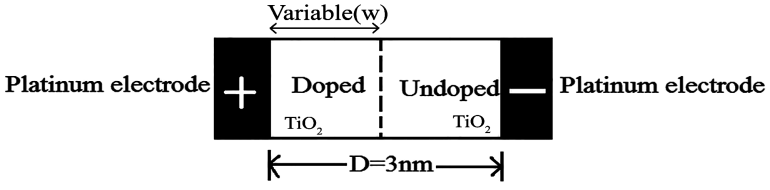

Figure 1. Memristor model based on [2].

$$v(t) = R_{mem}(w) \cdot i(t) \tag{2}$$

The speed of the movement of the boundary between the doped and undoped regions depends on the resistance of doped area, on the passing current, and on other factors according to the state Equation (3).

$$\frac{\mathrm{d}x}{\mathrm{d}t} = k \cdot i(t) \tag{3}$$

$$k = \frac{\mu_v R_{ON}}{D^2}, \tag{4}$$

where $\mu_v = 10^{-14}\,\mathrm{m}^2 \cdot \mathrm{s}^{-1} \cdot \mathrm{V}^{-1}$ is the so-called dopant mobility.

Small voltages can yield massive electric fields, which can secondarily produce significant nonlinearities in ionic transport. These nonlinearities clear themselves particularly at the thin film edges, where the speed of the boundary between the doped and undoped regions slowly decreases to zero. This phenomenon, called nonlinear dopant drift, can be modeled by the so called window function *f*(*x*). The paper [8] proposes the window function in the form of following Equation (5).

$$f(x) = 1 - (2x-1)^{2p}, \tag{5}$$

where *p* is a positive integer. This window function confirms zero drift at the boundaries but it grieves with terminal state problem. Biolek [7] proposed an alternative window function that contains memristive current i as an additional parameter. The following Biolek window function in Equation (6) is used for simulation.

$$f(x) = 1 - (x - stp(i))^{2p}, \tag{6}$$

where $stp(i) = 1$ for $i \geq 0$ and

$$stp(i) = 0 \text{ for } i \leq 0$$

The current is considered to be positive if it increases the width of the doped layer. Function (6) is zero at either edge.

3. Related Works

SRAM is a semiconductor memory commonly used in electronics industry and general computing applications. It is a volatile because when the power is removed from the memory device, the data will disappear. The most commonly used SRAM type is the 6T SRAM which offers better speed of operation, noise immunity and standby current. The main disadvantage of the 6T SRAM structure is its large size and high power consumption. To overcome these restrictions, hybrid memristor-CMOS SRAM memories are being developed recently. There are many researches on memristor-CMOS based memories. Barker Mohammad *et al*. [6] examined the write and read performance for a memristor based memory, based on surveying three different types of existing mathematical: linear, nonlinear, and exponential drift models. In [9] Syed Shakib Sarwar *et al*. proposed a new idea of NVRAM cell using memristor. The read time is much faster compared to a conventional SRAM and the power consumption is also much smaller. In [10] E. Linn *et al*. presented a complimentary resistive switch and it consists of two anti-serial memristive elements which validates the construction of large passive crossbar arrays with a drastic reduction in power consumption. Eshraghian *et al*. in [11] provided the nonvolatile characteristics and nanoscale geometry of the memristor together with its compatibility with CMOS process technology increases the memory cell packing density, reduces power dissipation and provides for new approaches towards power reduction and management through disabling blocks of MCAM cells without loss of stored data.

4. Proposed Memristor-CMOS Hybrid Memory Cell

The main feature of proposed circuits is as follows.

1) Create a spice model of memristor that closely matches the mathematical model by using Biolek window function [7] that includes memristor current as an additional parameter.

2) Design of new nonvolatile memory cell that consists of four transistors and it is compared with existing memristor based memory cell [9] and conventional 6T SRAM cell [12].

3) No need of generating external "comb" signal for enabling data input and data out of the memory cell [9]. The same read and write signal within the memory cell is used for enabling data in and out.

4) No need of safety margin is allotted for each logic output [13]. By using DBL method it can be removed and provides better read/write data integrity.

5) Analyses the nonvolatile property, read time, write time and power dissipation of proposed memory cell.

DBL Method

In this method, a ground potential is raised to slightly negative rather than zero. During read operation, the memory cell output goes to positive volts when data input is logic 1 and negative volts when data input is logic zero for the corresponding data input Din = vdd (logic 1) and Din = 0 volt (logic 0). It will eliminate a safety margin is left for each logic output [13] and enables a better Read/write data integrity. This voltage can be easily interpreted as a logic1 and logic 0 by any one of the sensing amplifier or comparator techniques.

The circuit schematic of proposed SRAM cell is shown in **Figure 2**. The NMOS transistor M1 and M2 are used to Read the data from memristor and write the data into the memristor respectively. The transistor M3 and M4 are used to isolate a memory cell from other memory cell during read and write operation and enables the data input into the memory cell and data out from the memory cell. No extra signal is needed such as comb in [9]. Two memristors U1 and U2 are used as a storage element.

During write operation, two memristors U1 and U2 are comes under parallel connection as shown in **Figure 3(a)** and during read operation, they are comes under serial connection as shown in **Figure 3(b)**. When a bit is to be written, RD is connected to low state and WR is connected to high state. The data input Din = 2 volts (logic 1) and Din = 0 volt (logic 0). If a bit is to be read, RD is connected to high state and WR is connected to low state, then the voltage at data out as [9] following in Equation (7).

$$\text{Data out} = \{(Vdd/2)-(-Vdd/10)\}\times\{R2/(R2+R1)\}+(-Vdd/10) \quad , \tag{7}$$

where, R1 and R2 are the resistances of memristor U1 and U2 respectively. As a polarities of the memristors are opposite, flux produced at U1 and U2 are also opposite in direction. If Din = logic 1, flux at U2 is higher than U1 and Din = logic 0, flux at U1 is higher than U2.

5. Simulation Results and Analysis

Simulation arrangement is formed with additional transistor for the verification of nonvolatile property of a

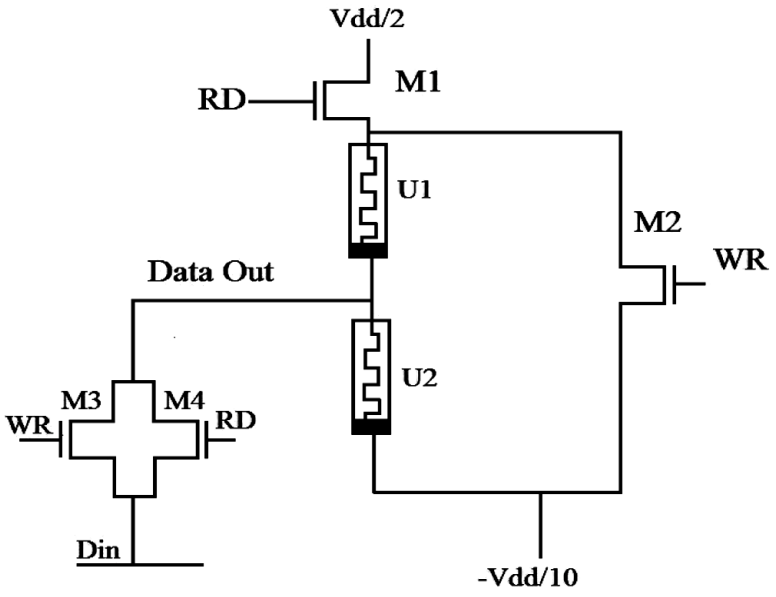

Figure 2. Proposed SRAM Cell.

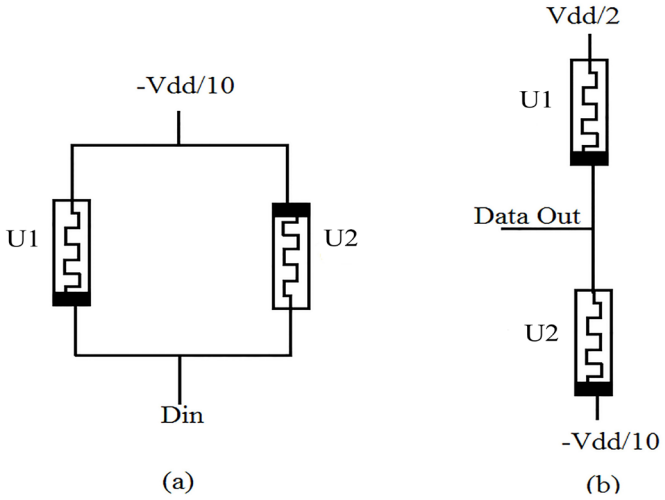

Figure 3. Circuit schematic while (a) Write operation, (b) Read operation.

memristor. MOSFETs of the tsmc-180 nm technology are used for simulation. The proposed circuit is simulated by using LTspice IV 4.1 simulation tool. It is a fourth generation switching regulator design program from Linear Technology. The program consists of a high performance SPICE simulator protracted with a mixed mode simulation capability. The Program's integrated classified schematic capture and SPICE simulator are available for general use. The improved performance of the SPICE Simulation engine is an advantage for simulating general analog circuits and should be of attention to all electronic engineers [14]. In this paper, during write operation −0.2 volt (−vdd/10) is applied at one end of memory cell and other end having 2 volts for logic 1 and 0 volt for logic 0. During read operation, voltage applied between the memory cell is vdd/2 and (−vdd/10). A voltage −0.2 volt is selected based on the best output pattern and simulation parameter of the memristor. The memory cell output bounces distinct binary logic *i.e.* 1.043 volts for logic 1 and −0.571 volt for logic 0. This voltage can be easily understood by using comparator with zero reference voltage. The following parameters are used for circuit simulation: R_{ON} = 1 kΩ, R_{OFF} = 100 KΩ, R_{INIT} = 80 KΩ, D = 3 nm, u_v = 350e−9 and p = 25. The above parameters are chosen based on the biolek window function and best output pattern after the number of iterations are completed.

5.1. Write and Read Operation (When Din = 1)

During write1operation, logic 1 is written in to the memory cell. For that, data input Din = 1, write signal WR = 1 is activated in the interval 2 ns to 4.5 ns by applying PWL input voltage as shown in **Figure 4(a)**. The input data for logic 1 is appeared at memristor as shown in **Figure 4(b)**. The write time interval is found based on the best flux pattern created when writing logic 1. At that time flux at memristor U2 is higher than U1, *i.e.* in opposite direction as shown **Figure 4(c)**. After write operation, all the power sources are switched off for the interval 20 ns to 40 ns, the power supply Vdd/2 and (−Vdd/10) goes to low state as shown in **Figure 5**. Next read signal RD = 1 is applied continuously five pulses and each pulse having 0.1ns duration to examine the saved data as shown in **Figure 6(a)**. After that the data is present *i.e.* data out = 1.043 volts as shown in **Figure 6(b)**. The results reveal that the reading operation does not interrupt the internal state of the memory cell.

5.2. Write and Read Operation (When Din = 0)

During write 0 operation, logic 0 is written in to the memory cell. For that, Din = 0, WR = 1 is activated in the interval 2 ns to 4.5 ns by applying PWL input voltage as shown in **Figure 7(a)**. The input data for a logic 0 is appeared at memristor as shown in **Figure 7(b)**. When writing logic 0, flux at memristor U1 is higher than U2 *i.e.* in opposite direction as shown **Figure 7(c)**. After write 0 operations, all the power sources are switched off for the interval 20 ns to 40 ns. Next data is to be read by activating RD = 1 for a continuously five pulses having 0.1 ns duration as shown in **Figure 8(a)**. Data is present *i.e.* data out = −0.571 volt as shown in **Figure 8(b)**.

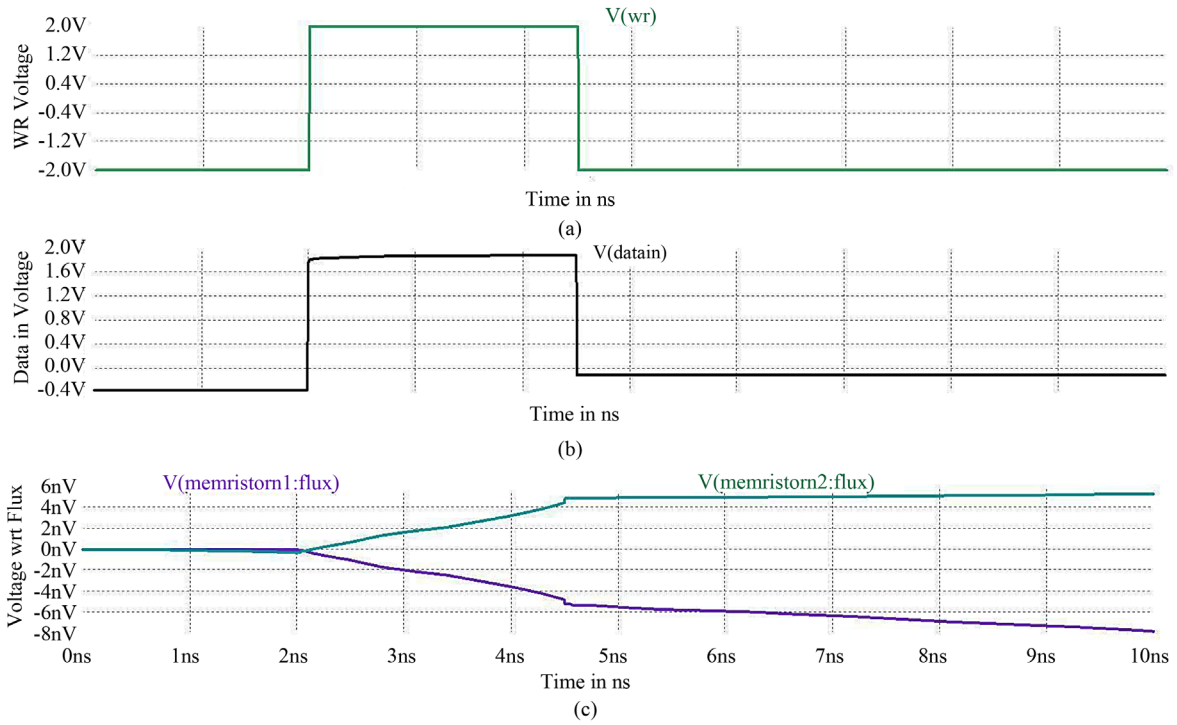

Figure 4. Timing diagram of write operation when Din = 1. (a). Write signal, (b). Data input at memristor, (c). Flux of memristor U2 is higher than U1.

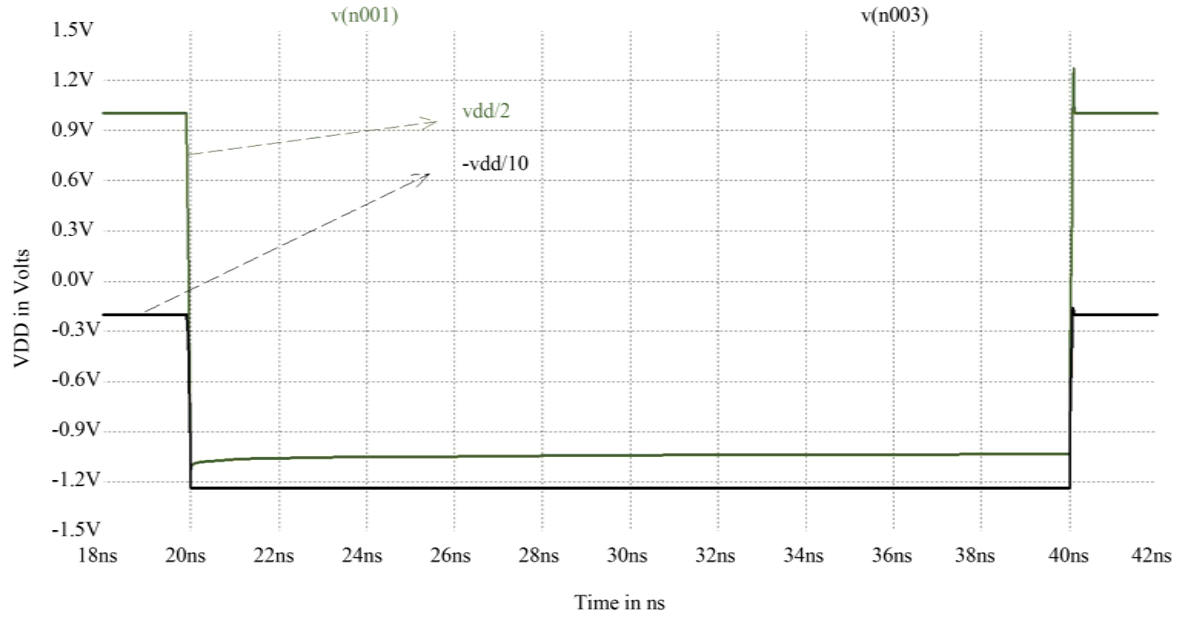

Figure 5. All the power sources switched off during the time interval 20 - 40 ns for investigate nonvolatility of memristor.

This voltage is interpreted as logic 0 and the reading operation does not disturb the internal state of the memory cell.

5.3. Observations

This proposed memristor-CMOS memory cell is nonvolatile in nature. A read operation is done after switching

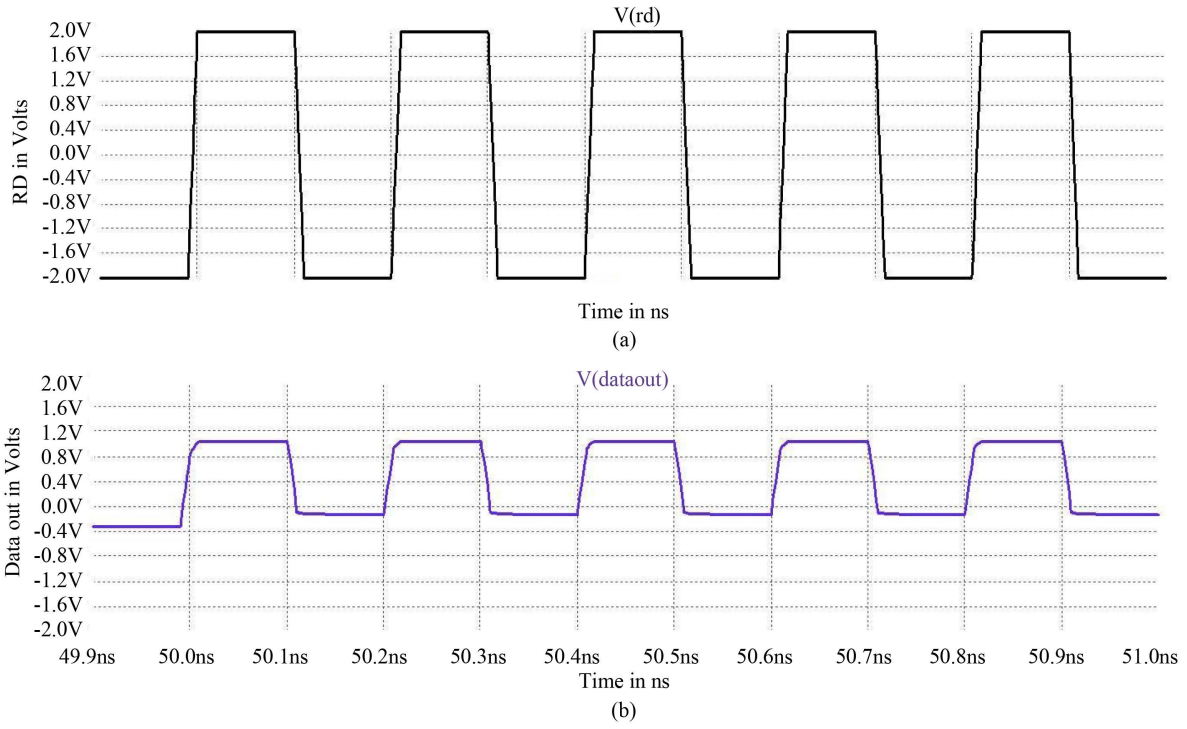

Figure 6. Timing diagram of read operation when Din = 1. (a). Read signal, (b). Data output.

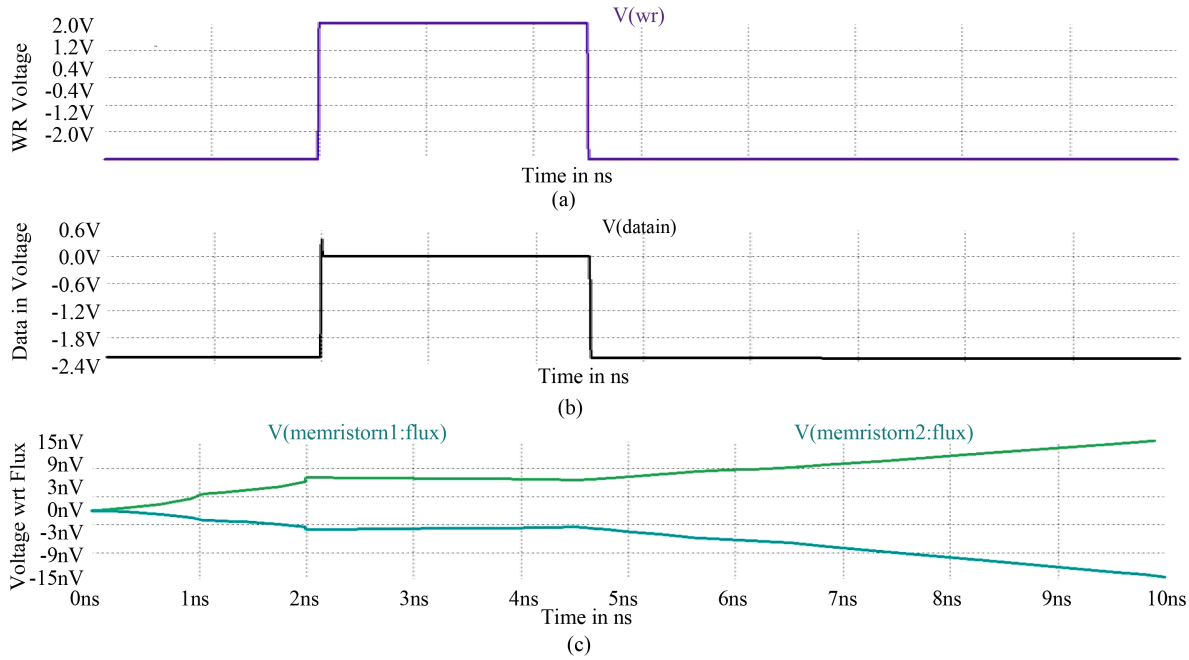

Figure 7. Timing diagram of write operation when Din = 0. (a). Write signal, (b). Data input at memristor, (c). Flux of memristor U1 is higher than U2.

ON the power sources and found “1(0)” in the memory cell. The Write and read time of the proposed memory cell is compared with memristor based memory cell [9] as shown **Table 1**.

The proposed memory cells entails a less read and write time compared with [9] and more write time than the 6T SRAM cell [12]. By further growing the mobility of the memristor [9] and new type of window function

incorporated in memristor modelling, the write time can be considerably reduced. From simulation the power dissipation curve was found and integration was done to get the energy dissipated for write 0, write 1, read 0 and read 1 operation. The corresponding power dissipations are obtained by dividing energy values in particular operation cycle as shown in **Table 2**. The total power dissipation is calculated by averaging the obtained values as given in **Table 3**.

Power consumption is less than memristor based memory SRAM cell and conventional 6T cell. Our proposed memory cell consists of four transistors and two memristors. So the predicted area is less than 6T SRAM cell and higher than the existing memristor based memory cell. The width of the memristor is 3nm, so the area can be further reduced by adopting recent CMOS technologies.

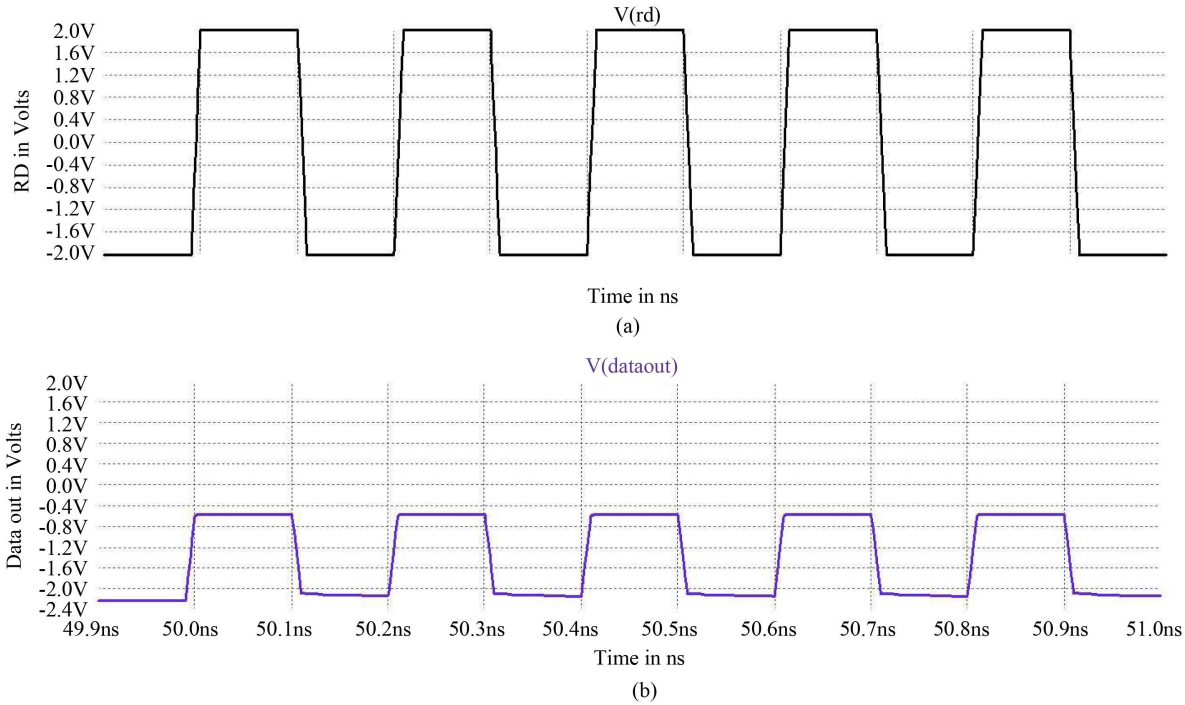

Figure 8. Timing diagram of write operation when Din = 0 (a). Read signal, (b). Data output.

Table 1. Write and read time comparison.

Operation	Proposed SRAM Cell (ns)	Memristor Based SRAM Cell [9]	6T-Cell [10] (ns)
Write time	2.5	5.9	0.85
Read time	0.1	0.2	1.23

Table 2. Power dissipation during write and read operation.

Operation	Write 0	Write 1	Read 0	Read 1
Energy (fj/cycle)	45.271	17.218	10.330	12.545
Average power (μW)	18.108	6.887	103.388	125.448

Table 3. Power comparison.

Operation	Proposed SRAM Cell (mW)	Memristor Based SRAM Cell (mW) [9]	6T-Cell [10] (mW)
Power	0.127	0.407	10.373

6. Conclusion

In this paper, we proposed a memristor-CMOS based nonvolatile SRAM cell and investigated a nonvolatility of memristor. Safety margin left for each output logic will be avoided by DBL method. Power consumption is significantly reduced. Read and write time is much smaller compared with memristor based memory cell but write time is much higher than the conventional SRAM cell. It can be further reduced by incorporating recent memristor modelling and CMOS fabrication technology. There are further scopes to work on design of SRAM array, reduction of write time and power consumption as well.

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