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MMCC Based Electronically Tunable Allpass Filters Using Grounded Synthetic Inductor

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Abstract

New circuit implementations of electronically tunable first and second order allpass filter (AP) structures using a Multiplication Mode Current Conveyor (MMCC) building block are presented. The control voltage (V) of the MMCC tunes the desired phase (θ) while the time constant (τ) is adjustable by a Differential Voltage Current Conveyor Transconductance Amplifier (DVCCTA)-based synthetic lossless grounded inductor (L). The circuits are analyzed taking into account the device imperfections which show low active sensitivity features of the designs. The effects of port transfer error (ε) and that of the parasitic capacitances of the active devices had been meticulously examined which indicated that certain deviations in nominal design equations occur; these however, could be minimized with appropriate choice of the circuit passive components. Readily available AD-844 type Current Feedback Amplifier (CFA) elements are utilized for the topology implementation. Satisfactory test results on electronic θ-tunability, upto about 300 KHz, had been verified by PSPICE simulation and with hardware experimentation.

Keywords

Allpass Filter; MMCC; DVCCTA; CFA; Synthetic Inductor; Electronic Phase Shifter

1. Introduction

AP filters are special purpose function circuits which provide variable phase response [1]-[13] in a prescribed frequency band keeping the transmission gain constant. These filters are widely used in communication systems as phase/delay equalizers, phase injector for stability improvement [14], in phase lock loop (PLL) and in voltage controlled oscillator (VCO) design. The functional versatility improves significantly if the phase could be tuned

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electronically.

The literature indicates that many such variable phase AP filter design schemes had been proposed using various types of active building blocks, e.g., voltage operational amplifier [1]-[3], current conveyor (CC) [4]-[6], DVCCTA [7], fully differential current conveyor (FDCC) [8], differential difference amplifier (DDA) [9], current inverting transconductance amplifier (CITA) [10], operational transconductance amplifier (OTA) [11], voltage differencing differential input buffered amplifier (VD-DIBA) [12], differential voltage current conveyor (DVCC) [12]. While most of these designs are passive tuned, recent attention appears to be on electronic phase tunability aspect [15]-[17]. It is seen that for electronic tuning, usually the bias current of a transconductance (g_m) block is utilized. This involves elaborate current processing circuitry and additional quiescent power requirement along side.

Here we propose that the recently introduced MMCC building block [18] is quite amenable to this purpose if its control voltage terminal is utilized. The use of MMCC device for such AP filters had not yet been reported. The control voltage here may be directly fed ensuring circuit simplicity and suitability for integration. In our design, a four-quadrant multiplier [19] [20] device (ICL-8013 or AD-534) had been coupled at the front end of the MMCC device implementation while its back end is fabricated with AD-844 CFA element [20]-[23].

The phase selective component is a DVCCTA based synthetic lossless grounded inductor (L) as proposed recently by our research group [24]; it is connected to the current source x-terminal of the MMCC. The first order transfer (H_1) is derived by connecting only the synthetic-L while second order function (H_2) is obtained by forming a series LC resonator with a capacitor (C).

The effects of the device imperfections, viz., port tracking error (ε) and parasitic shunt-rC components of both the devices have been carefully analyzed. The findings indicate that through appropriate design and with suitable choice of the active-L component, the deviations could be made insignificant leading to low active-sensitivity realization. All the analytical derivations are supported by experimental verification with PSPICE simulation [25] and by hardware test using the multiplier-CFA composite device implementation. There are several advantageous features of the CFA-AD-844 IC-chip with respect to low noise at extremely small tracking error $\left(|\varepsilon| \ll 1\right)$ and, superior bandwidth and slew rate capabilities [20]-[23].

2. Circuit Analysis and Design

The building blocks and their device implementation schemes are shown in **Figure 1**. The MMCC block in **Figure 1(a)**, is configured with ICL-8013 (and also AD-534 as a variant) and AD-844 CFA. The nodal relations are $V_x = V_{y1}V_{y2}$, $i_z = i_x$ and $I_{y1,2} = 0$. The control voltage (V) is applied at y_2 terminal where k (= 0.1/volt) is the multiplication constant and input signal V_i is applied at y_1 terminal. We verified that polarity of MMCC could be made simply inverting or noninverting by altering the sign of V. The CFA nodal relations are $i_z = \alpha_1 i_x, V_x = \beta_1 V_y$ and $V_o = \delta_1 V_z$ while $I_y = 0$. The port transfer coefficients may be postulated as $\alpha_1 = (1-\varepsilon_{i1}), \beta_1 = (1-\varepsilon_{v1}), \delta_1 = (1-\varepsilon_{o1})$ where $|\varepsilon| \ll 1$. Hence in **Figure 1(b)** we get $i_z = i_x, V_x = kVV_{y2}$ and $V_w = V_z$ which is an additional voltage source output node, not usually depicted in conventional current conveyor; with ± V one gets a ±MMCC block.

The nodal relations of the DVCCTA block as in **Figure 1(c)** are $i_z = \alpha_2 i_x, V_x = \beta_2 (V_1 - V_2)$ and $i_o = \delta_2 g_m V_z$; here also we may define the tracking ratios in terms of finite-ε error. The DVCCTA device implementation using AD-844 CFA element is shown in **Figure 1(d)**.

The electronically tunable allpass filter (ETAF) topology is shown in **Figure 2** while the two synthetic-L simulators are shown in **Figure 3**. The input admittance (Y_i) of these simulators would be connected as the admittance Y_3 in **Figure 2**. The various device parasitics are shown as the shunt-rC arms; typical values of these components [25] [26] are 2 MΩ < $r_{p,z}$ < 6 MΩ and 3 pF < $C_{p,z}$ < 7 pF. Analysis assuming ideal devices in **Figure 2** yields a voltage transfer $H \equiv Vo/Vi$ as

$$H = G_1\{G_2 - kVY_3\}/G_2\{G_1 + kVY_3\} \tag{1}$$

where $G_{1,2}$ are conductances; for proposed design we take $G_1 = G_2 = 1/R$ and Y_3 would be the synthetic admittance of **Figures 3(a)** and **(b)** for the first order AP function. Next we propose two second order ETAF designs by considering Y_3 as the series LC resonator of which the inductance would be utilized from the L-simulators of **Figures 3(a)** and **(b)** along with a passive capacitor.

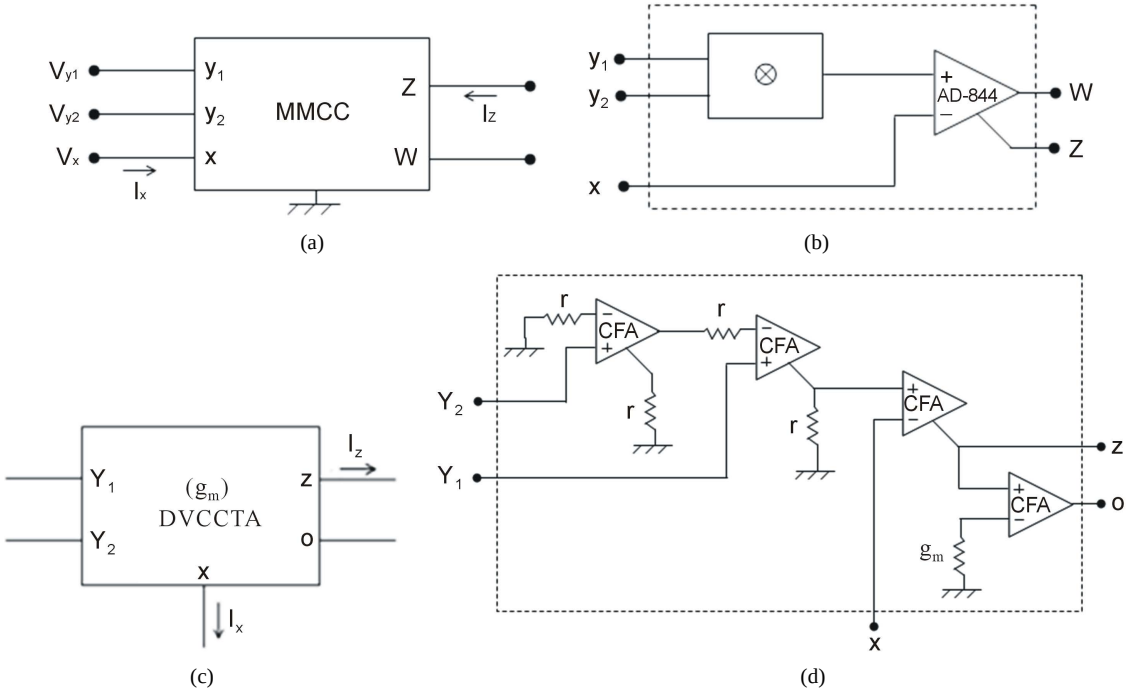

Figure 1. The active building blocks (a) MMCC device (b) MMCC implementation with commercially available IC-chips (c) DVCCTA device (d) DVCCTA device implementation with CFAs.

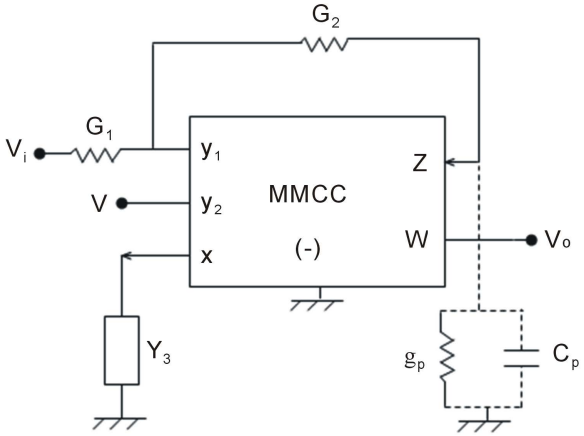

Figure 2. MMCC based AP filter structure.

3. First Order ETAF

We now present the first order ETAF realization in **Figure 2** wherein the grounded admittance Y_3 is being implemented by the input admittance Y_i of **Figures 3(a)** and **(b)**. The analysis is first carried out assuming ideal MMCC and DVCCTA building blocks, *i.e*. parasitics are negligible $\left(C_{p,z}=0=g_{p,z}\right)$ and port errors are insignificant $\left(\varepsilon=0\right)$.

The first order AP function (H_1) is derived assuming $G_{1,2} = 1/R$, as

$$H_1=\{s\tau-1\}/\{s\tau+1\} \tag{2}$$

where $\tau=L/kRV$. For both the topologies of the inductor simulators we have $Y_i=1/sL\equiv Y_3$ and $L=C_oR_oR_m$ if $R_m=1/g_m$. The select frequency is $\omega_o=1/\tau$ and the phase is $\theta=-2\arctan\left(\omega/\omega_o\right)$. Thus the select frequency and the phase response are electronically tunable by the control voltage (V) in a range $0\le\theta\le\pi$. Here no additional current processing circuitry is needed for tuning by g_m.

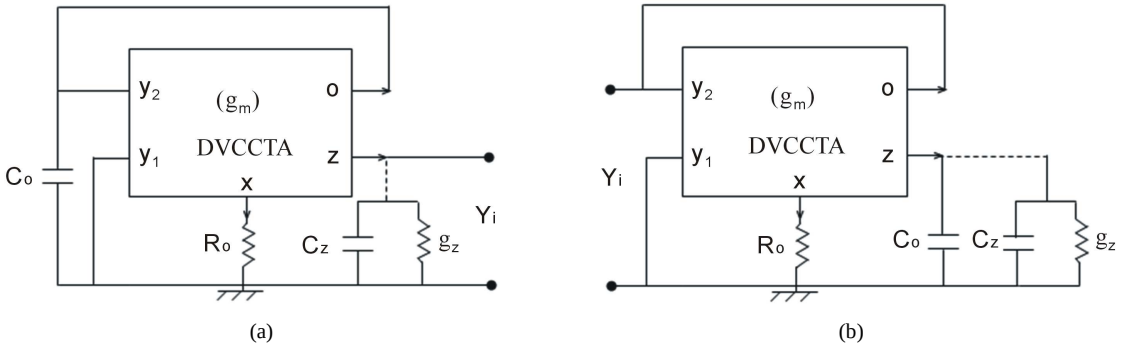

Figure 3. DVCCTA based L-simulators.

4. Second Order ETAF

The synthetic-L is seen to be lossless in **Figure 3** under ideal conditions. For realizing the second order MMCC based ETAFs, we form a series-LC resonator using a passive capacitor with the L so that the series combination yields $Y_3 = sC/\left(s^2LC+1\right)$. Using this in Equation (1) and writing $R = 1/G_{1,2}$ we get the second order (H_2) AP functions while both topologies of **Figure 3** are connected to node-x of **Figure 1**. Therefore H_2 is

$$H_2 = \left\{(s/\omega_o)^2 - (s/\omega_o q)+1\right\}/\left\{(s/\omega_o)^2 + (s/\omega_o q)+1\right\} \tag{3}$$

where $\omega_o = 1/\sqrt{LC}$ and $q = \sqrt{L/C}/kRV$ is quality factor; simplified design equations are obtained if $R_o = R_m = R$ so that $\omega_o = 1/R\sqrt{C_oC}$ and $q = \sqrt{C_o/C}/kV$. Phase variation is given by

$$\theta = -2\arctan\left\{u/\left(1-u^2\right)q\right\}; u = \omega/\omega_o \tag{4}$$

Thus θ is tunable by V while phase slope in the frequency response is adjusted by q. These results are summarized in **Table 1**.

5. Effects of Device Imperfections

The proposed AP circuit topologies have been thoroughly re-examined keeping in view the imperfections of the two types of devices used. These nonidealities are owing to finite port transfer ratio errors $(\varepsilon \neq 0)$ and due to presence of the parasitic components appearing in the form of shunt-$r_{p,z}C_{p,z}$ arms.

First we present the effect finite port error of the MMCC $(\alpha,\beta,\delta)_M$ and the DVCCTA $(\alpha,\beta,\delta)_D$. Analysis shows that transfer function in Equation (1) modifies to

$$H' = \delta_M\left\{1-(\alpha\beta)_M\left(kVY_3/Y\right)\right\}/\left\{1+(\alpha\beta)_M\left(kVY_3/Y\right)\right\}. \tag{5}$$

Similarly L-values are altered:

$$L' = L(\alpha\beta\delta)_D \tag{6}$$

Combining Equations (5) with (6) and replacing Y_3 by Y_i, we observe that albeit the inductance value is slightly altered (L'), it remains lossless in both structures of **Figure 3** which implies that filter time constant is also altered $(\tau' = L'/kRV)$. However, the nonminimum phase property of the filter function remains unaffected while θ will be tunable by V as per prescribed design.

Next we consider the effects of the finite parasitic components at the z-node of MMCC block (C_p, g_p) and the DVCCTA block (C_z, g_z).

The transfer now modifies to

$$H'' = \left\{1-kRVY_3\right\}/\left\{2sRC_p + kRVY_3 + 2b + 1\right\} \tag{7}$$

where $b = R/r_p \ll 1$.

Re-Analysis indicates that admittance in **Figure 3(a)** is

$$Y_{ia} = sC_z + g_z + (1/sL) \tag{8}$$

Table 1. First and second order ETAF design with ideal devices.

Transfer function	Input Impedance Z_i	ETAF Design	
	Figures 3(a) and **(b)**	1st order	2nd order
$H=\frac{1-kVRY_3}{1+kVRY_3}$	$Z_i = sL$ $L = R_0C_0R_m$	$Y_3 = Y_i = 1/sL$ $H_1=\frac{1-\left(\frac{s}{\omega_0}\right)}{1+\left(\frac{s}{\omega_0}\right)}$ $\omega_0=\frac{kVR}{L}$ $\theta_1=-2\arctan\left(\frac{\omega}{\omega_0}\right)$	$Y_i = 1/SL$ $Z_3 = sL+1/sC$ $H_2=\frac{\left(\frac{s}{\omega_0}\right)^2-\left(\frac{s}{\omega_0 q}\right)+1}{\left(\frac{s}{\omega_0}\right)^2+\left(\frac{s}{\omega_0 q}\right)+1}$ $\omega_0=\frac{1}{\sqrt{LC}}$ $q=\frac{\sqrt{L/C}}{kVR}$ $\theta_2=-2\arctan\left(\frac{u/q}{1-u^2}\right)$ $u=\frac{\omega}{\omega_0}$

which is the shunt combination of L with the parasitic components. The simulated impedance in **Figure 3(b)** is

$$Z_i = sL'+r; L' = L(1+\mu); r = aR_o \tag{9}$$

where $\mu = C_z/C_o \ll 1$ and $a = R_m/r_z \ll 1$.

Further detailed analysis had been carried out for examining the effects of these parasitics on the proposed first and second order ETAFs. These derivations are tabulated in a comprehensive manner in **Table 2**.

The findings on the phase calculations are listed in **Table 3**. One may observe that the parasitic capacitors affect the expected phase variation (θ) at higher frequency ranges by introducing a second order term being dominated by ω_z; hence the higher side of the usable frequency will be limited by $f_z \approx 3$ MHz for **Figure 3(a)** and by $f_p \approx 2.1$ MHz for **Figure 3(b)** assuming a set of typical values of L = 1 mH, R = 1 KΩ, $C_p \approx C_z \approx 3$ pF and V ≈ 10 V.d.c. (max.)

$$a_0 = kVR/r_z \ll 1, a_1 = m+\left(\frac{kVR}{r_z}\right) \approx 1, m = 1+2b \approx 1, b = \frac{R}{r_p} \ll 1,$$

$$n = \frac{r}{kVR} \ll 1, \lambda = m+\left(\frac{2rC_p}{kV\tau'}\right) \approx 1, d = \frac{mr}{kVR} \ll 1,$$

$$n_1 = 1-\left(\frac{\tau}{Cr_z}\right) \approx 1, n_2 = 1+\mu-a_0 \approx 1, d_3 = 1+\left\{\frac{2C_p(1+\mu)}{kVC_z}\right\} \approx 1,$$

$$d_2 = \left[m(1+\mu)+2\left(\frac{RC_p}{r_zC}\right)+a_0\right] \approx 1, d_1 = \left[1+\left(\frac{mR_0R_m}{kVRr_z}\right)+\left(\frac{2C_p}{kVC}\right)\right] \approx 1,$$

$$\gamma = 1-n \approx 1, p_1 = 1+d \approx 1, p_2 = m+\left(\frac{2RC_pr}{L'}\right) \approx 1$$

For second order AP function design, the parasitic capacitors introduce a 3rd-order term in the transfer function that is being dominated by ω_e and ω_i; by the same set of values we get $f_e \approx 960$ KHz and $f_i \approx 888$ KHz which are the values of maximum upper operating frequency for the second order ETAF. It may be inferred that with appropriate choice of the nominal circuit components such that $R/r_{p,z} \ll 1$ and $C_{p,z}/C \ll 1$, the proposed

filters would perform as per nominal design. This aspect had been meticulously verified with experimental work based by PSPICE simulation and with hardware circuit tests; the measured response is shown **Figure 4**.

Table 2. Effect of device parasitic on filter function.

Figure	Simulated input admittance	ETAF Transfer	
		1st order	2nd order
3(a)	$Y_i = sC_z + g_z + 1/sL$	$-H_{1a} = \dfrac{s^2LC_z - (1-a_0)s\tau + 1}{s^2LC_za_2 + a_1s\tau + 1}$	$H_{2a} = \dfrac{-s^3LCC_zkVR + s^2LCn_2 - skVRCn_1 + 1}{s^3LCC_zkVRd_3 + s^2LCd_2 + skVRCd_1 + m}$
3(b)	$Y_i = (sL' + r)^{-1}$ $L' = L(1+\mu); \mu = C_z/C_0 \ll 1$ $r = aR_0; a = \dfrac{g_z}{g_m} \ll 1$	$H_{1b} = \dfrac{s\tau' - (1-n)}{2s^2RC_p\tau' + s\lambda\tau' + d + 1}$	$H_{2b} = \dfrac{s^2L'C - skVRC + 1}{2s^3L'CRC_p + s^2L'Cp_2 + skVRCp_1 + m}$

Table 3. Phase calculation under non-ideal condition.

Figure	1st order	2nd order
3(a)	$\theta = \arctan\left\{\dfrac{\omega\tau(1-a_0)}{1-u_z^2}\right\} + \arctan\left\{\dfrac{\omega\tau a_1}{1-a_2u_z^2}\right\}$ $\approx 2\arctan(\omega\tau)$ $\tau = \dfrac{10L}{VR}$ $u_z = \dfrac{\omega}{\omega_z} \ll 1$ $\omega_z = 1/\sqrt{(LC_z)}$	$\psi = \pi - \theta$ $\theta = -\arctan\left[\dfrac{\left\{\left(\dfrac{n_1u}{q}\right) - p^3\right\}}{1-n_2u^2}\right] - \arctan\left[\dfrac{\left\{\left(\dfrac{d_1u}{q}\right) - d_3p^3\right\}}{m-d_2u^2}\right]$ $\approx 2\arctan\dfrac{u/q}{(1-u^2)}$ $u = \dfrac{\omega}{\omega_0}$ $\omega_0 = \dfrac{1}{\sqrt{LC}}$ $p = \dfrac{\omega}{\omega_e} \ll 1$ $\omega_e = \dfrac{1}{\sqrt[3]{LCC_zkVR}}$ $q = \dfrac{\sqrt{\dfrac{L}{C}}}{kVR}$
3(b)	$\theta = \arctan\left\{\dfrac{\omega\tau'}{1-n}\right\} + \arctan\left\{\dfrac{\omega\lambda\tau'}{1+d-u_p^2}\right\}$ $\approx 2\arctan(\omega\tau')$ $\tau' = \dfrac{10L'}{VR}$ $u_p = \dfrac{\omega}{\omega_p} \ll 1$ $\omega_p = 1/\sqrt{2RC_p\tau'}$	$\theta = -\arctan\left[\dfrac{\dfrac{\gamma u'}{q'}}{1-u'^2}\right] - \arctan\left[\dfrac{\left\{\left(\dfrac{p_1u'}{q'}\right) - h^3\right\}}{(1-p_2u'^2)}\right]$ $\approx -2\arctan\left[\dfrac{\left(\dfrac{u}{q}\right)}{(1-u^2)}\right]$ if $\mu \ll 1$ $u' = \dfrac{\omega}{\omega_0'}, \omega_0' = \dfrac{1}{\sqrt{L'C}}$ $h = \dfrac{\omega}{\omega_i} \ll 1$ $\omega_i = \dfrac{1}{\sqrt[3]{2L'CRC_p}}$ $q' = \dfrac{\sqrt{\dfrac{L'}{C}}}{kVR}$

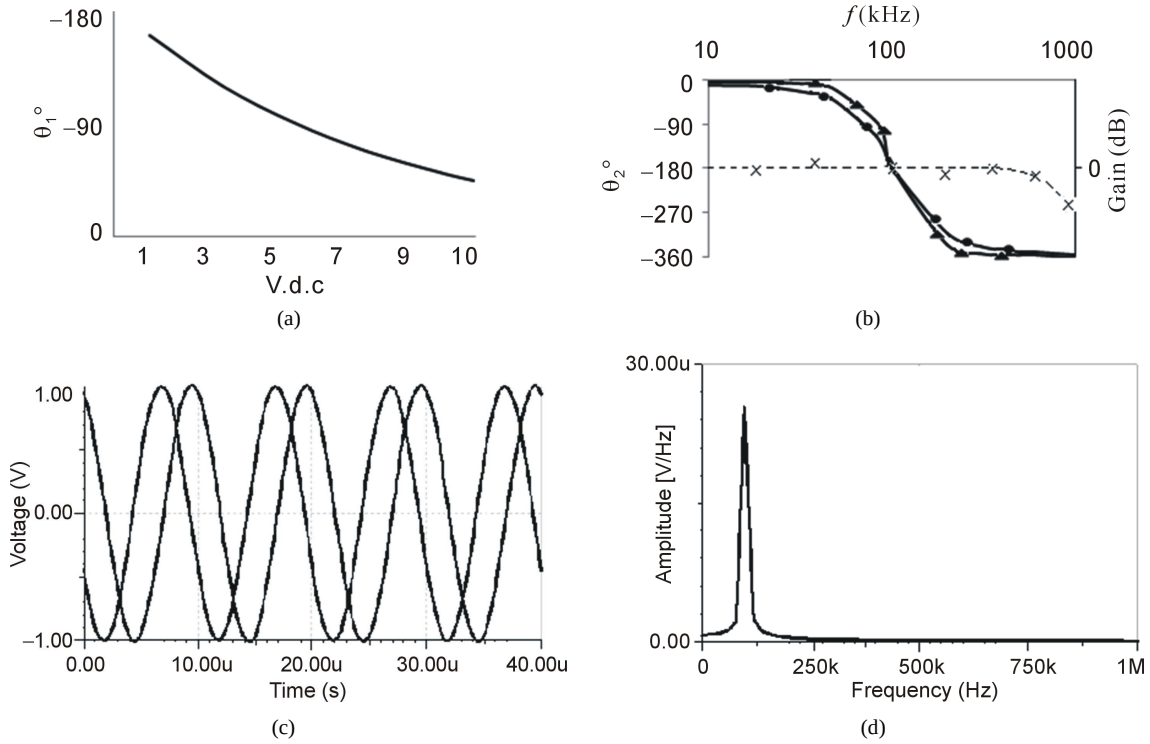

Figure 4. Experimental results on ETAFs (a) 1st order tested at 200 KHz with L_a = 0.4 mH, R = R_o = R_m = 1 KΩ, C_o = 0.4 nF: θ_1-Variation wth V (b) 2nd order θ_2-response for q = 2,V = 5 ( ) and q = 5,V = 2 ( ) with L_b = 2.5 mH, C = C_o = 1 nF, R = 1.6 KΩ; dotted line: magnitude reponse (c) Quadrature wave response of first order AP filter at 100 KHz (d) Spectrum of 90˚ phase shifted output signal.

6. Experimental Results

The proposed MMCC based ETAFs had been designed using the device implementation of **Figure 1**. The aspect of electronic tuning of the variable phase (θ) is achieved by simple adjustment of control voltage (1 V.d.c ≤ V ≤ 10 V.d.c) of the MMCC block. This tuning procedure had been found to be simpler with respect that used in some previous work [15] [17] where additional current control circuitry would be needed for g_m-variation.

The phase selective elements are chosen here are DVCCTA-based synthetic lossless-L for first order AP function, and subsequently a second order AP function using a resonating capacitor in series with the synthetic-L. These component sets are connected at the x-node of the MMCC block. The MMCC device implementation in hardware had been obtained using the AD-844 CFA chip along with a multiplier ICL-8013 (or AD-534) chip. The phase response was measured using both PSPICE [25] simulation and by hardware test; we measured the parasitic capacitor values to be $C_p \approx 4.5$ pF and $C_z \approx 6$ pF at V_{cc} = ± 15 V.d.c. Satisfactory θ-tuning is obtained upto about 300 KHz by varying V for both first and second order ETAFs while transmission gain was observed at unity in this band.

The test results are shown in **Figure 4** where $L_{a,b}$ indicates the simulation of **Figures 3(a)** and **(b)**. We chose the nominal components such that $R \ll r_{p,z}$ and $C \gg C_{p,z}$ so as to minimize the effects of the parasitic.

7. Conclusions

The proposed ETAF can be controlled through external DC voltage V. In this paper we present two new circuit realization schemes of ETAFs using the relatively new MMCC building block to which DVCCTA-based synthetic inductive input admittance [24] is conveniently connected; for the first order function we use only the synthetic-L while for the second order, a capacitor constituting to a series resonator is used. Both the building blocks are implemented with readily available multiplier and CFA IC-chips. Compared to other such schemes [15] [17], here no additional current control circuitry is needed since electronic tuning is achieved by simply applying V to the MMCC control-node. This is an advantage in view of less hardware complexity and avoiding

additional quiescent power dissipation leading to easy integrability.

The effects of device imperfections have been thoroughly analyzed. It is seen that port errors (ε) cause insignificant deviations on phase since active-S^{τ} sensitivity is quite low as $\left|S^{\tau}\right| = \varepsilon/\left(1-\varepsilon_t\right) << 1$ where $\varepsilon_t \approx \left(\varepsilon_i + \varepsilon_v + \varepsilon_o\right)$. However, the parasitics introduce some deviations on θ-characteristics and reveal certain limits on the maximum usable frequency. With appropriate choice of the nominal circuit components, these deviations could be minimized.

The proposed circuit topology is based on the new MMCC device which is identified as a versatile CCCS building block with inherent voltage control functionality [18] offering the designer the distinct advantage of utilizing this attribute by simply connecting a voltage signal at one of its input nodes. Other such phase shifters use transconductance (g_m) as a control parameter which subsequently is derived by a bias current that involves a nonlinear equation [7]; hence limited operating range at the cost of complicated current processing circuitry leading to increased hardware density. Also here we utilized a DVCCTA based high-quality synthetic-L realized by only one grounded-RC section, *i.e.*, the minimal passive count; this L is then connected to the MMCC block that needs also the minimal component count, *i.e.*, only one resistor pair for the realizability. The same topology yields both first and second order functions as per design choice. Our study indicates that all electronic active building blocks devised hitherto contain parasitics [21]-[24] which influence the performance of the function circuit based on these. In the proposed work we had analyzed the parasitic effects extensively and obtained a congregated design based on the judicious choice of circuit components that insures sufficiently accurate voltage tuned phase variation at low sensitivity within the prescribed band as substantiated by the experimental results shown.

The practical performance of these ETAFs had been verified by hardware circuit fabrication and also with PSPICE simulation. Expected range of tunability of θ by V is obtained in a frequency band of upto 300 KHz. Some test results are presented showing the phase variation for two quality factor values (q = 2 and q = 5) of the second order ETAF. We are now studying on the design of linear voltage controlled quadrangle oscillator (VCQO) using these ETAFs as further work.

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References

[1] Ponsonby, J.E. (1966) Active Allpass Filter Using a Differential Operational Amplifier. *Electronics Letters*, **2**, 134-135. http://dx.doi.org/10.1049/el:19660107

[2] Genin, R. (1968) Realisation of an Allpass Transfer Function Using Operational Amplifier. *Proceedings of the IEEE*, **56**, 1746-1747. http://dx.doi.org/10.1109/PROC.1968.6731

[3] Nandi, R. (1977) New Allpass Phase Shifters. *International Journal of Electronics*, **42**, 97-99. http://dx.doi.org/10.1080/00207217708900617

[4] Soliman, A.M. (1973) Inductorless Realization of Allpass Transfer Function Using the Current Conveyor. *IEEE Transactions on Circuits and Systems I*, **20**, 80-81.

[5] Nandi, R. (1992) Novel Current Mode Allpass Phase Shifters Using a Current Conveyor. *IEEE Transactions on Instrumentation and Measurement*, **41**, 553-555. http://dx.doi.org/10.1109/19.155925

[6] Higashimura, M. and Fukui, Y. (1990) Realization of Current Mode Allpass Networks Using a Current Conveyor. *IEEE Transactions on Circuits and Systems I*, **37**, 6660-6661. http://dx.doi.org/10.1109/31.55015

[7] Pandey, N., Pandey, R. and Paul, S.K. (2012) A First Order Allpass Filter and its Application in a Quadrature Oscillator. *Journal of the Electron Devices Society*, **12**, 772-777.

[8] Mohan, J., Maheshwari, S. and Chauhan, D.S. (2010) Voltage Mode Cascadable Allpass Sections using Single Active Element and Grounded Passive Components. *Journal of Circuits and Systems—Scientific Research Publishing*, **1**, 5-11.

[9] Toker, A. and Ozoguz, S. (2004) Novel Allpass Filter Using Differential Difference Amplifier. *AEU—International Journal of Electronics and Communications*, **58**, 153-155. http://dx.doi.org/10.1078/1434-8411-54100221

[10] Biolek, D. and Biolkova, V. (2009) Allpass Filter Employing One Grounded Capacitor and One active Element. *Electronics Letters*, **45**, 807-808. http://dx.doi.org/10.1049/el.2009.0575

[11] Psychaslinos, C. and Pal, K. (2010) A Novel Allpass Current Mode Filter Realized Using a Minimum Number of Sin-

gle-Output OTAs. *Journal of Frequenz*, **64,**123-129.

[12] Biolek, D. and Biolkova, V. (2010) First Order Voltage Mode Allpass Filter Employing One Active Element and One Grounded Capacitor. *Analog Integrated Circuits and Signal Processing*, **65**, 123-129.

[13] Ibrahim, A., Minaei, S. and Yuce, E. (2012) Allpass Sections with Rich Cascadability and IC Realization Suitability. *International Journal of Circuit Theory Applications*, **40**, 461-472.

[14] Wangenheim, L.V. (2012) Phase Margin Determination in a Closed Loop Configuration. *Journal of Circuit System and Signal Processing*, **31**, 1917-1926. http://dx.doi.org/10.1007/s00034-012-9437-7

[15] Herencsar, N., Minaei, S., Koton, S., Yuce, E. and Vrba, K. (2013) New Resistorless and Electronically Tunable realization of Dual-Output VM Allpass Filter Using VDIBA. *Journal of Analog Integrated Circuits and Signal Processing*, **74**, 141-154. http://dx.doi.org/10.1007/s10470-012-9936-2

[16] Nandi, R., Kar, M. and Das, S. (2009) Electronically Tunable Dual-Input Integrator Employing a Single CDBA and a Multiplier. *Journal of Active and Passive Electronic Components*, **2009**, 1-5. http://dx.doi.org/10.1155/2009/835789

[17] Li, Y.A. (2014) Electronically Tunable Current Mode Biquadratic Filter and Four-Phase Quadrature Oscillator. *Microelectronics Journal*, **45**, 330-335.

[18] Hwang, Y.S., Liu, W.H., Tu, S.H. and Chen, J.J. (2009) New Building Block: Multiplication Mode Current Conveyor. *Circuits, Devices and Systems—The IET*, **3**, 41-48.

[19] Intersil Datasheet (1998) File #2477.5 and (Apr.1999) File #2863.4.

[20] Analog Devices (1990) Linear Products Databook. Norwood.

[21] Tammam, A.A., Hayatleh, K., Ben-Esmael, M. and Terzopoulus, N. (2013) Critical Review of the Circuit Architecture of CFOA. *International Journal of Electronics*, **101**, 441-451.

[22] Palumbo, G. and Pennisi, S. (2001) Current Fedback Amplifiers versus Voltage Operational Amplifiers. *IEEE Transactions on Circuits and Systems I*, **48**, 617-623. http://dx.doi.org/10.1109/81.922465

[23] News Updates (2004) Internet Version: Global Signal Processing Times.

[24] Nandi, R., Kar, M. and Das, S. (2011) Synthetic Inductor Based Resonators Using DVCCTA. *Proceedings of International Conference EUROCON*, Portugal, 584-586. http://dx.doi.org/10.1109/EUROCON.2011.5929212

[25] Macromodel of AD-844 AN in PSPICE Library (1992) Microsim Corpn. Irvine.

[26] Venkateswaran, P., Nandi, R. and Das, S. (2012) New Integrators and Differentiators Using a MMCC. *Circuits and Systems*, **3**, 288-294. http://dx.doi.org/10.4236/cs.2012.33040