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Experimental Demonstration of g_m/I_D Based Noise Analysis

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Abstract

Recent studies using BSIM3 models have suggested that noise depends on the transconductance-to-drain ratio (g_m/I_D) of a transistor. However, to the best of our knowledge, no experimental result demonstrating g_m/I_D dependent noise previously observed in simulation is available in the literature. This paper examines the underlying principles that make it possible to analyze noise using g_m/I_D based noise analysis. Qualitative discussion of normalized noise is presented along with experimental results from a 130 nm CMOS process. A close examination of the experimental results reveals that the device noise is width independent from 1 Hz to 10 kHz. Moreover, noise increases as g_m/I_D is reduced. The experiment observation that noise is width independent makes it possible for circuit designers to generate normalized parameters that are used to study noise intuitively and accurately.

Keywords

g_m/I_D Design Methodology; Noise Analysis; Flicker Noise

1. Introduction

In integrated circuits, noise phenomena are caused by small current and voltage fluctuations that are generated within the devices themselves. At low frequencies, the noise spectrum is dominated by the flicker noise. At high frequencies, the noise spectrum is dominated by the thermal noise. The study of noise is important because it ultimately determines the smallest signal that a circuit can amplified without significant deterioration in signal quality [1].

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From a designer's perspective, noise is a property of the circuit that must be designed carefully along with other circuit parameters such as gain, power dissipation, speed, and linearity. Noise analysis is particularly challenging in sub-micron CMOS circuit design because it involves parameters that depend on the bias condition of a transistor as well as the geometry of a transistor. In the absence of an easy-to-use model for accurate back-of-the-envelope noise calculation, designers often explore design space using arduous circuit simulations. Over-reliance on circuit simulator can be problematic, potentially luring inexperienced designers to dive into simulation without understanding basic trade-offs in properly optimized circuits.

1.1. A Brief Overview of Related Work

In 1996, Silveira *et al*. proposed a powerful transconductance-to-drain current $\left(g_m/I_D\right)$ technique that has since become the basis of many later developments in structured analog circuit design [2]. The so-called "g_m/I_D design approach" was originally developed to help designers to size up transistors quickly with good accuracy and to calculate parameters such as small signal gain and bandwidth. Recently, it has found applications in large signal behavior of a power amplifier [3], phase noise optimization of an LC oscillator [4], MOSFET nonlinearity characterization [5], MOSFET variability and ageing degradations [6]. A simple g_m/I_D CAD tool has also been developed recently to optimize analog circuits without lengthy simulations [7]. A book dedicated to g_m/I_D methodology has also been published [8].

A g_m/I_D based noise analysis was reported in 2011 [9]. Bias dependent thermal noise coefficient $\left(\gamma\right)$ and device noise corner frequency $\left(f_{co}\right)$ were used to characterize MOSFET noise. In 2012, Alvarez and Abusleme published a formulation of g_m/I_D based noise analysis using normalized noise power instead of γ and f_{co} [10]. In [10], noise curves for a set of transistors are pre-computed by means of SPICE simulations, scaled for the appropriate device parameters using the g_m/I_D technique, and finally, noise is computed using interpolations within the curves. The work in [10] was applied in the context of charge amplifiers in [11].

1.2. Main Contributions of This Paper

To the best of our knowledge, what is currently known in the literature with respect to g_m/I_D based noise analysis is derived from either HSPICE analysis [10] or BSIM simulation ([9] and [11]). According to a study conducted by Rhayem *et al.* [12], each noise model has a different accuracy with respect to measured data. For example, the SPICE noise model is not accurate for all regions of operation for both NMOS and PMOS. The HSPICE noise model cannot predict noise accurately for PMOS. For NMOS, the model can be used if a subcircuit includes access resistances and their excess noise sources. Even though the BSIM3v3 noise model is more accurate than either the SPICE noise model or HSPICE noise model, the most accurate portrayal of a device's noise is through measurement.

This paper presents an experimental study of g_m/I_D based noise. In particular, we present wafer measurement data from a 130 nm CMOS process utilizing both NMOS and PMOS transistors. Two experimental results are presented. *First*, we present the experimental data to show that the normalized noise is independent of a transistor's gate width. *Second*, we present the experimental data to show that the normalized noise increases as a transistor's g_m/I_D is reduced.

The organization of this paper is as follows: Section 2 provides a review of g_m/I_D analysis, followed by a discussion of thermal noise and flicker noise in the context of g_m/I_D based noise analysis. Section 3 shows the experimental results on g_m/I_D noise. Finally, we present our conclusions.

2. Formulation of Noise Measurement

We begin this section with a review of fundamentals of g_m/I_D analysis. We point out in this section that noise current $\left(\overline{i_n^2}\right)$ of an MOS transistor is width dependent, it is therefore *not* a valid g_m/I_D parameter. In order to make the noise current a valid g_m/I_D parameter, we normalize the noise by dividing $\overline{i_n^2}$ by g_m. The details are shown below.

2.1. Fundamentals of g_m/I_D Analysis

The g_m/I_D principle is applicable to parameters which are independent of the width $\left(W\right)$ of a transistor. **Figure 1** shows a transistor with a transconductance $\left(g_m\right)$, a drain-to-source conductance g_{ds}, and a current

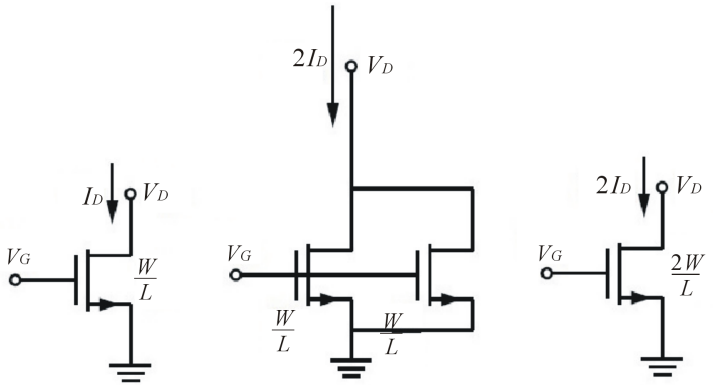

Figure 1. Transistors biased at the same g_m/I_D.

(I_D) biased at a gate-to-source voltage (V_{GS}) and a drain-to-source (V_{DS}). If an identical device is connected in parallel so both devices are biased at the same V_{GS} and V_{DS}, both devices have the same g_m, g_{ds} and the same I_D. Since the devices are connected in parallel, they can be treated as one device with an aspect ratio of $2W/L$. The effective transconductance over current ratio is g_m/I_D for both the merged device and the stand alone device because g_m and I_D are doubled. The drain-to-source conductance is also doubled for the merged device. Therefore the intrinsic gain (g_m/g_{ds}) is identical for both the stand alone device and the merged device. As long as transistors are biased at the same g_m/I_D, they will have the same g_m/g_{ds}. This observation is true for any two parameters whose ratio depend solely on the g_m/I_D and not on the width of a transistor. Once a transistor of a given W is characterized over a range of g_m/I_D, the g_m/I_D based parameters can be generalized to a transistor of an arbitrary W, **assuming that** L **remains constant**. The g_m/I_D methodology will hold as long as the parameter of interest scales with W.

2.2. Thermal Noise

The MOSFET noise arises from thermal noise fluctuations in the channel. It can be shown that the thermal noise at the drain terminal is [13],

$$\overline{i_{n,id}^2} = 4kT\gamma g_m, \tag{1}$$

where k is the Boltzmann constant, T is the temperature, g_m is the transconductance, and γ is the bias-dependent noise parameter. According to this model, the γ approaches 1 when the drain-to-source voltage (V_{DS}) approaches zero and decreases to $2/3$ when the device enters the saturation regime. The saturation value of $\gamma = 2/3$ is valid for long-channel MOS devices built on lightly doped substrates. Early studies have reported γ values between $2/3$ and 4 [14], but recent studies have shown that by accounting for parasitic resistances, γ is approximately $2/3$ for channel lengths equal or greater than 100 nm [15].
The thermal noise $\left(\overline{i_{n,id}^2}\right)$ at the drain terminal of a MOS transistor is

$$\overline{i_{n,id}^2} = 4kT\frac{\mu}{L^2}(-Q_I), \tag{2}$$

where Q_I is the total inversion layer charge underneath the gate oxide, L is the length of the transistor, and μ is the mobility. Equation (2) is valid for all regions of operation [13]. The total inversion layer charge (Q_I) is obtained by integrating the inversion charge per unit length $\left(Q_I'(x)\right)$ over the length of the channel,

$$Q_I = \int_0^L Q_I'(x)W\mathrm{d}x. \tag{3}$$

where $Q_I'(x)$ is a function of V_{GS} and V_{DS}, as well as V_{SB}, and consequently a function of transistor's g_m/I_D. Since Q_I is proportional to W (see Equation (3)), $\overline{i_{n,id}^2}$ is proportional to W according Equation (2). Since g_m is proportional to W, $\overline{i_{n,id}^2}/g_m$ becomes independent of W. Equation (2) also shows that $\overline{i_{n,id}^2}$ is inversely proportional to L^2. Even though the transconductance of a transistor also depends on the L, it is

not inversely proportional to L^2. Therefore, $\overline{i_{n,id}^2}/g_m$ is a function of L. Once $\overline{i_{n,id}^2}/g_m$ of a transistor for a given (W/L) is characterized over a range of g_m/I_D; $\overline{i_{n,id}^2}/g_m$ of the transistor can be generalized to a transistor of arbitrary W as long as L and the g_m/I_D are constant. We will verify this observation in Section 3. This width-independent property is the crucial link to the g_m/I_D design methodology described earlier.

2.3. Flicker Noise

Since MOSFETs are surface-conduction devices, flicker noise is important at low frequencies. The flicker noise present at a MOSFET can be expressed into a noise current at the drain terminal of a transistor with

$$\overline{i_{n,fn}^2} = \frac{K_f}{C_{ox}WL}\frac{g_m^2}{f}, \tag{4}$$

where K_f is a process dependent constant and C_{ox} is the oxide capacitance. Equation (4) can be rewritten to explicitly show its dependence on g_m/I_D parameters as

$$\overline{i_{n,fn}^2} = \frac{K_f}{C_{ox}Lf}\frac{g_m}{I_D}\frac{I_D}{W}g_m. \tag{5}$$

If we divide $\overline{i_{n,fn}^2}$ by g_m, we find

$$\frac{\overline{i_{n,fn}^2}}{g_m} = \frac{K_f}{C_{ox}Lf}\frac{g_m}{I_D}\frac{I_D}{W}. \tag{6}$$

Thus, we have in $\overline{i_{n,fn}^2}/g_m$ a parameter which depends exclusively on the g_m/I_D of a transistor. It should be pointed out that I_D/W (the current density) is also a function of g_m/I_D. Furthermore, Equation (6) implies that any two transistors, regardless of their widths (W), theoretically exhibits the same $i_{n,fn}^2/g_m$ if they are biased at the same g_m/I_D. This is a useful property to compare measured noise of different transistors biased at the same g_m/I_D.

3. Experimental Results

Section 2 identifies $\overline{i_n^2}/g_m$ as a function of g_m/I_D parameter satisfying all characteristics described in Section 2.1. The $\overline{i_n^2}/g_m$ is used here as a parameter to compare noise characteristics of different transistors. In order to experimentally prove such formulations, ten NMOS transistors from a CMOS 130 nm process are chosen from three different wafers. Each transistor has a length of 0.12 μm and a width of 10 μm. The gate of each transistor is biased at 0.45 V and the drain of each transistor is biased at 1.0 V. The source terminal is grounded $(V_{SB}=0)$. We present the noise as a function of g_m/I_D and as a function of the frequency. Both i_n^2 and g_m are determined experimentally without curve fitting.

3.1. Noise as a Function of g_m/I_D

The single-finger and ten-finger NMOS transistors from a 0.13 μm CMOS process are measured, and separated into two sets of data. The noise current at the drain terminal is measured comparing a single-finger $(W=10\ \mu\text{m})$ and ten-finger $(W=100\ \mu\text{m})$ data sets biased at the same voltages.

The average g_m, g_{ds} and I_D of both sets of transistors are shown in **Table 1**. The dimensions of the transistors are shown in the first row of the table using the format: $\text{width}(W)\times\text{length}(L)\times\text{fingers}(Nf)$. The total width of each transistor is obtained by multiplying W by Nf. The transistors shown in the fourth column have ten times the width than the transistors in the third column, and hence have ten times the g_m, g_{ds}, I_{ds}. The g_m/I_D and g_m/g_{ds} are approximately the same since g_m, I_D and g_{ds} are proportional to the width of a transistor. We conclude that g_m/I_D dependent parameters (e.g., g_m/g_{ds}) are independent of W.

Having verified that transistors are biased correctly, we investigate $\overline{i_n^2}/g_m$ as a function of g_m/I_D. The V_{GS} is varied as V_{DS} is held constant in order to change g_m/I_D of a transistor. The drain-current density is measured at 100 Hz as V_{GS} is changed. The $\overline{i_n^2}/g_m$ of a 10 μm device is compared to the $\overline{i_n^2}/g_m$ of a 100

μm device. In **Figure 2**, the average $\overline{i_n^2}/g_m$ (represented with marks) and the standard deviation (represented with error bars) of ten samples are shown.

The $\overline{i_n^2}/g_m$ measured at 100 Hz is dominated by flicker noise. Equation (5) suggests that $\overline{i_n^2}/g_m$ is proportional to g_m/I_D and I_D/W. the current density I_D/W is inversely proportional to $(g_m/I_D)^2$. Therefore, $\overline{i_n^2}/g_m$ increases as g_m/I_D is reduced. The 10 μm device exhibits more process variation than the 100 μm device as expected. The close correlation of the 10 μm device and the 100 μm device measurements (see **Figure 2**) demonstrate that $\overline{i_n^2}/g_m$ are width independent, and therefore g_m/I_D dependent as stated in Section 2.3.

3.2. Noise as a Function of Frequency

The $\overline{i_n^2}/g_m$ of the transistors measured from 1 Hz to 100 kHz are shown in **Figure 3**. The PMOS devices exhibit less noise than the NMOS devices as previously observed and theoretically expected [13]. Good correlation

Table 1. Comparison of g_m/I_D parameters. NFETs are biased at $V_{GS}=0.45$ V and $V_{DS}=1.0$ V; PFETs are biased at $V_{SG}=0.41$ V and $V_{SD}=1$ V. Device dimensions: $W(\mu m)\times L(\mu m)\times$ Fingers.

Device	Parameter	10 × 0.12 × 1	10 × 0.12 × 10
NFET	g_m (mS)	2.253	24.190
	i_{ds} (mA)	0.150	1.679
	g_{ds} (mS)	0.100	1.143
	g_m/I_D (S/A)	13.929	14.347
	g_m/g_{ds}	22.077	20.924
PFET	g_m (mS)	0.383	3.981
	i_{ds} (mA)	0.023	0.242
	g_{ds} (mS)	0.015	0.165
	g_m/I_D (S/A)	16.764	16.398
	g_m/g_{ds}	25.693	23.963

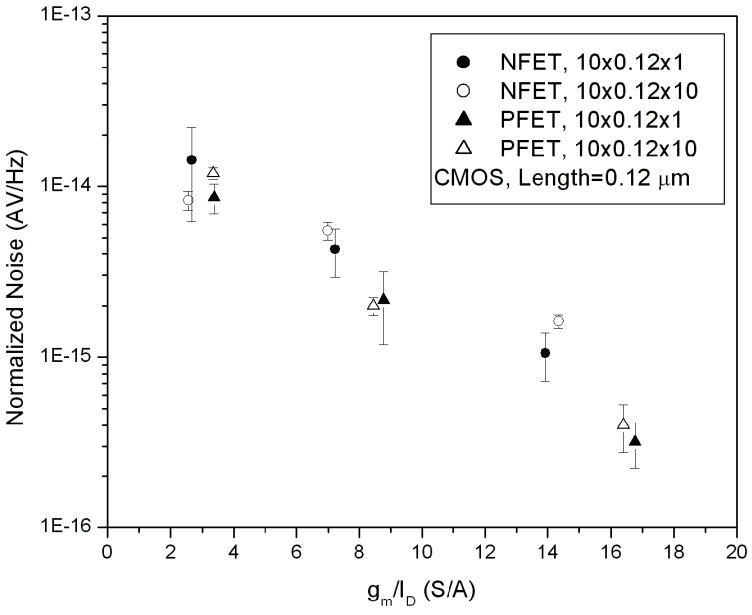

Figure 2. The $\overline{i_n^2}/g_m$ comparison over a range of g_m/I_D for NFET $V_{DS}=1.0$ V, and PFET $V_{SD}=1.0$ V.

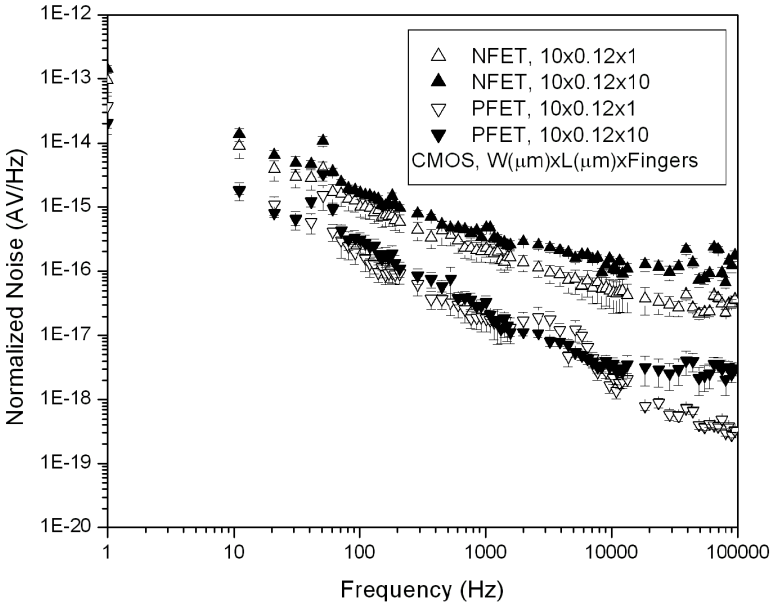

Figure 3. The $\overline{i_n^2}/g_m$ noise compared from 1 Hz to 10 kHz for: NFET $V_{DS} = 0.45$ V, PFET $V_{SD} = 0.41$ V.

between the 10 μm devices and 100 μm devices is presented from 1 Hz to 1 kHz. Our calculation shows that the noise flattening at frequencies higher than 10 kHz is attributed to the noise introduced by the instrumentation amplifier used in the measurement set-up. The close correlation of $\overline{i_n^2}/g_m$ from 1 Hz to 1 kHz demonstrates that device noise is width independent.

4. Conclusion

This paper examines the underlying principles that make it possible to study noise using g_m/I_D based noise analysis. Fundamentals of g_m/I_D analysis were presented, followed by a discussion of normalized thermal noise and normalized flicker noise. Experimental results were shown to demonstrate that noise is indeed width independent from 1 Hz to 10 kHz. Furthermore, noise increases as g_m/I_D is reduced. The experiment observation that noise is width independent makes it possible for circuit designers to generate normalized parameters that are used to study noise intuitively and accurately.

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