Circuits and Systems, **2014, 5, 39-44**
Published Online February 2014 (http://www.scirp.org/journal/cs)
http://dx.doi.org/10.4236/cs.2014.52006

Scientific Research

A Domain Extension Algorithm for Digital Error Correction of Pipeline ADCs

Ting Li[1], Chao You[2]
[1]Electrical and Computer Engineering Department, North Dakota State University, Fargo, USA
[2]Information Engineering School, Nanchang University, Nanchang, China
Email: ting.li@my.ndsu.edu, you.chao@gmail.com

Received 6 January 2014; revised 6 February 2014; accepted 13 February 2014

ABSTRACT

A domain extension algorithm to correct the comparator offsets of pipeline analog-to-digital converters (ADCs) is presented, in which the 1.5-bit/stage ADC quantify domain is extended from a three-domain to a five-domain. This algorithm is designed for high speed and low comparator accuracy application. The comparator offset correction ability is improved. This new approach also promises significant improvements to the spurious-free dynamic range (SFDR), the total harmonic distortion (THD), the signal-to-noise ratio (SNR) and the minor analog and digital circuit modifications. Behavioral simulation results are presented to demonstrate the effectiveness of the algorithm, in which all absolute values of comparator offsets are set to |3Vref/8|. SFDR, THD and SNR are improved, from 34.62-dB, 34.63-dB and 30.33-dB to 60.23-dB, 61.14-dB and 59.35-dB, respectively, for a 10-bit pipeline ADC.

KEYWORDS

Behavioral Simulation; Comparator Offsets; Domain Extension Algorithm; Pipeline ADCs

1. Introduction

ADCs are widely used in many areas, such as music recording, healthcare, radar systems and communication [1]. A trend of the modern ADC design is the use of digital background calibration to compensate for the raw performance of analog circuits [2-9]. However, many digital background calibrations can only correct gain errors [10,11], which are caused by finite op-amp gain and capacitor mismatches. This leaves the comparator offsets corrected by the traditional digital error correction technique or not corrected at all. The traditional 1.5-bit/stage ADC can only correct the comparator offsets within $\pm V_{\text{ref}}/4$ [12]. For small-geometry transistors, typical mismatches in the width, length and threshold voltage can lead to significant comparator offsets [13]. Comparator offsets greatly limit the accuracy of a switched capacitor pipeline ADC. In this paper, a new algorithm is developed to improve the comparator offset correction ability for the 1.5-bit/stage pipeline ADC. This innovative algorithm increases the comparator offset toleration ability by 50%. In addition, the algorithm also provides crucial information on both overflow and underflow situations.

2. Domain Extension Algorithm

Figure 1(a) shows the residue plot of the traditional 1.5-bit/stage ADC. In **Figure 1(a)**, two ideal threshold voltages are $-V_{\text{ref}}/4$ and $V_{\text{ref}}/4$ shown with dotted lines. The coded range is from $-V_{\text{ref}}$ to V_{ref}. The residue plot of a real ADC with comparator offsets is shown using dashed lines. In this case, the maximum comparator offset is $V_{\text{ref}}/4$ and the corresponding maximum output equals to V_{ref}. Since the output of the current stage is the input of the next stage, and the input range is from $-V_{\text{ref}}$ to V_{ref}, the out of range output leads to code loss. In order to prevent the ADC from code loss, the comparator offsets should be within the range of $-V_{\text{ref}}/4 \sim V_{\text{ref}}/4$.

Figure 1(b) shows the residue plot of the proposed 1.5-bit/stage ADC. Here, the ideal threshold voltages are $-3V_{\text{ref}}/4$, $-V_{\text{ref}}/4$, $V_{\text{ref}}/4$, and $3V_{\text{ref}}/4$. This coded

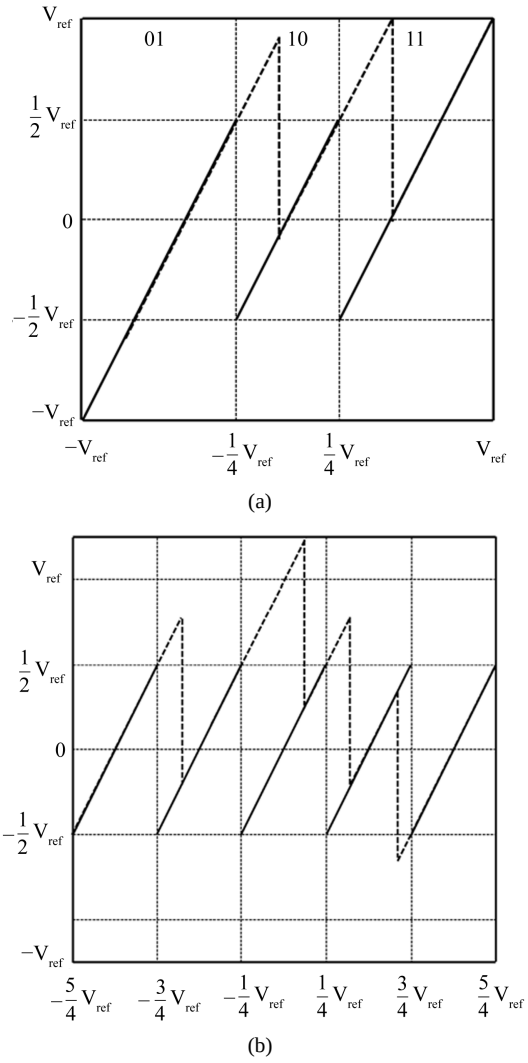

Figure 1. (a) Residue plot of the traditional 1.5-bit/stage ADC and (b) residue plot of the five-domain 1.5-bit/stage ADC.

range is from $-5V_{ref}/4$ to $5V_{ref}/4$. By adding two comparators with comparison voltages of $-3V_{ref}/4$ and $3V_{ref}/4$ to the lower and upper sides of traditional 1.5-bit/stage ADC, the analog quantify domain is a five-domain rather than a three-domain; therefore, this proposed configuration is referred to as a five-domain 1.5-bit/stage ADC. Like in **Figure 1(a)**, the residue plot of a real ADC with comparator offsets in **Figure 1(b)** is shown in the dashed lines. In this case, the maximum comparator offset is $3V_{ref}/8$ and the corresponding outputis $5V_{ref}/4$. Since the input range is changed to $-5V_{ref}/4 \sim 5V_{ref}/4$, the comparator offsets that the developed ADC can tolerate without code loss should be within the range of $-3V_{ref}/8 \sim 3V_{ref}/8$.

However, the traditional 1.5-bit/stage ADC can only correct the comparator offsets within $\pm V_{ref}/4$. In this research, a five-domain 1.5-bit/stage ADC is developed to increase the comparator offset correction ability to $\pm 3V_{ref}/8$ with an added overflow/underflow judgment. Two Matlab behavioral simulations are used to illustrate the improvement of the comparator offset correction ability for the proposed ADC. The first ADC behavioral simulation includes eight traditional 1.5-bit/stage converters followed by a flash ADC, and the second ADC behavioral simulation includes eight trial 1.5-bit/stage converters also followed by a flash ADC. In these simulations, the absolute values of the comparator offsets are set between 0 and $|0.5V_{ref}|$. In order to control and narrow research findings, all 1.5-bit/stage ADCs are only-complicated by the comparator offsets. In addition, the flash ADCs setting are ideal. In these simulations, the total number of conversions is 2^{14}. The total miscode numbers, and their related comparator offsets, are show in **Figure 2**. According to **Figure 2**, for the ADC based on the traditional digital error correction technique, miscodes occur when the absolute values of the comparator offsets are higher than $|V_{ref}/4|$. By comparison, no miscodes occur for the absolute values of the comparator offsets lower than $|3V_{ref}/8|$, for the ADC based on the proposed algorithm.

The transfer function of the traditional 1.5-bit/stage pipeline ADC is given by the following equation [14]:

$$V_{out} = \begin{cases} 2V_{in} + 1V_{ref}, & D = 01 \\ 2V_{in} + 0V_{ref}, & D = 10 \\ 2V_{in} - 1V_{ref}, & D = 11 \end{cases}. \quad (1)$$

The transfer function of the proposed five-domain 1.5-bit/stage pipeline ADC is given by the following equation:

$$V_{out} = \begin{cases} 2V_{in} + 2V_{ref}, & D = 000 \\ 2V_{in} + 1V_{ref}, & D = 001 \\ 2V_{in} + 0V_{ref}, & D = 010 \\ 2V_{in} - 1V_{ref}, & D = 011 \\ 2V_{in} - 2V_{ref}, & D = 100 \end{cases}. \quad (2)$$

This proposed ADC consists of eight 1.5-bit stages followed by a 2-bit flash ADC. There are 12 total output bits, 10usable bits and the first two bits are utilized as overflow/underflow bits. **Figure 3** shows the algorithm process. In order to have the digital output of five-domain 1.5-bit/stage ADC consistent with the traditional 1.5-bit/stage ADC, the subtraction of one operation is needed. Since 000 minus 1 is negative, adding a "1" in front of the digital output of the first stage avoids the negative number. For the same reason, the later stages also need to subtract one operation. In addition, the dislocation addition should be implemented before the subtraction of one. The first two bits are overflow/underflow bits. Therefore, when they are "11" or "01", they will reference to the input signal beyond or below the reference

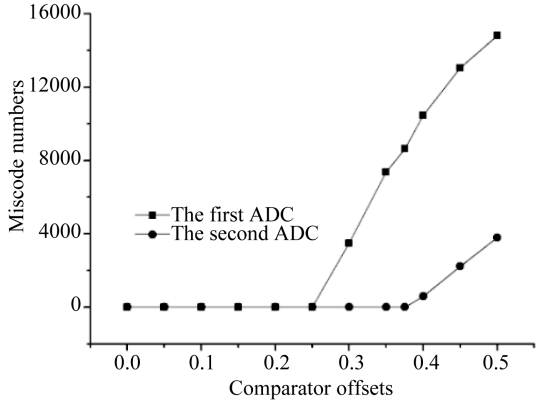

Figure 2. Miscode numbers for various comparator offsets.

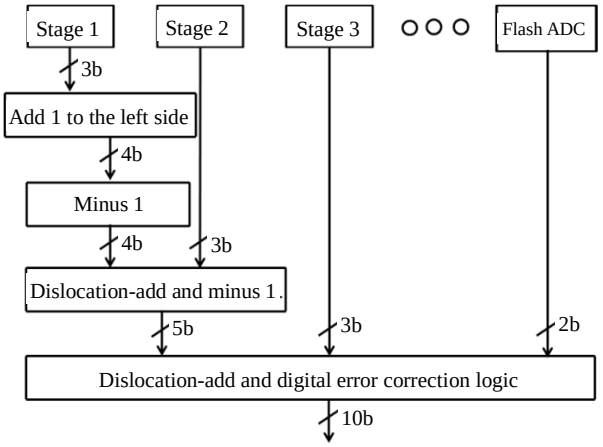

Figure 3. Five-domain 1.5-bit/stage ADC algorithm process.

range; otherwise when they are "10", the remaining ten bits are usable digital output bits.

The proposed algorithm of the ADC, shown in **Figures 4(a)** and **4(b)**, uses V_{ref} of 1 V and the input voltage of 0.4 V. The traditional algorithm is shown in **Figures 4(c)** and **4(d)** uses the same V_{ref} and input values. To prevent the influences from flash-ADCs, all of the threshold voltages are set to be the ideal. In **Figure 4(a)**, the absolute values of comparator offsets are set to be $|3V_{ref}/8|$. In this case, for the first eight stages, the threshold voltages are $(-3/4-3/8)V_{ref}$, $(-1/4-3/8)V_{ref}$, $(1/4+3/8)V_{ref}$, and $(3/4+3/8)V_{ref}$ for all of the comparators. The first two bits are "10" indicating that the remaining ten bits are usable output codes. In **Figure 4(b)**, all the comparators do not suffer from comparator offsets. **Figure 4(c)** shows the processing of output codes based on the traditional digital error correction technique with the comparator offsets the same as **Figure 4(a)**, but the threshold voltages are $(-1/4-3/8)V_{ref}$ and $(1/4+3/8)V_{ref}$. **Figure 4(d)** shows the processing of output based on the traditional technique with the comparator offsets set to be zero. These three cases, **Figures 4(a)**, **4(b)**, and **4(d)**, have the correct digital output, while **Figure 4(c)** is different from the other three because the traditional technique cannot correct the absolute values of comparator offsets higher than $|V_{ref}/4|$.

The circuit level implementation of Equation (2) is given by

$$V_{out}=\begin{cases}\dfrac{C_1+C_2}{C_1}V_{in}+\dfrac{C_2}{C_1}V_{dd}, & D=000\\ \dfrac{C_1+C_2}{C_1}V_{in}+\dfrac{C_2}{C_1}V_{ref}, & D=001\\ \dfrac{C_1+C_2}{C_1}V_{in}+\dfrac{C_2}{C_1}GND, & D=010\\ \dfrac{C_1+C_2}{C_1}V_{in}-\dfrac{C_2}{C_1}V_{ref}, & D=011\\ \dfrac{C_1+C_2}{C_1}V_{in}-\dfrac{C_2}{C_1}V_{dd}, & D=100\end{cases} \quad (3)$$

In Equation (3), the two capacitors are equal. When the required gain is one, the circuit level realization is the same as the traditional technique, and capacitor C_2 connects to the corresponding reference voltage. However, a gain of two for V_{ref} cannot be realized through the traditional technique since one of the capacitors is the feedback capacitor. The maximum gain for V_{ref} is the non-feedback capacitor divided by the feedback capacitor, which is one. To extend the domain, a new method is proposed. In this new method V_{dd} need to be set to twice the V_{ref}. The first and the last equations of (3) are

$$\frac{C_1+C_2}{C_1}V_{in}+\frac{C_2}{C_1}V_{dd}=2\times V_{in}+1\times 2\times V_{ref}. \quad (4)$$

$$\frac{C_1+C_2}{C_1}V_{in}-\frac{C_2}{C_1}V_{dd}=2\times V_{in}-1\times 2\times V_{ref}. \quad (5)$$

Figures 5(a) and **5(b)** are the circuit configurations based on the traditional technique and the proposed algorithm, respectively. V_{ref} is simplified by V_r in the figures. Although the actual configurations are fully differential, the sing-ended the configurations are shown for simplicity. When Φ_1 is high, the converters work on the sample phase, input is sampled on the two capacitors simultaneously. When Φ_2 is high, they work on the amplification phase, the feedback capacitor C_1 connects to the output and the non-feedback capacitor C_2 connects to the corresponding reference voltage.

The proposed algorithm slightly modifies the analog. Two comparators are added to extend the quantify domains, and two references are used to provide a gain of two for V_{ref}. Since the actual configuration is fully dif-

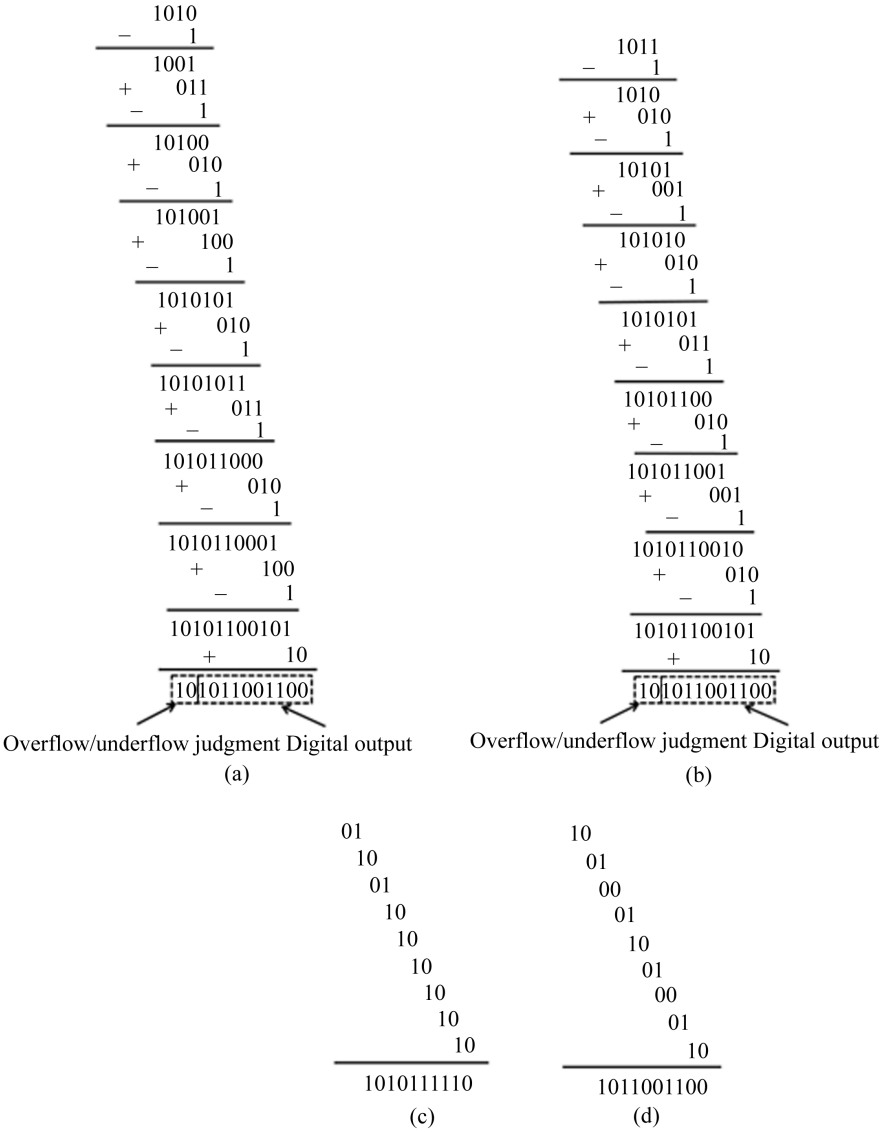

Figure 4. (a) Example of the proposed algorithm with the comparator offset of $3V_{ref}/8$; (b) Example of the proposed algorithm with no comparator offset; (c) Example of the traditional algorithm with the comparator offset of $3V_{ref}/8$; (d) Example of the traditional algorithm with no comparator offset.

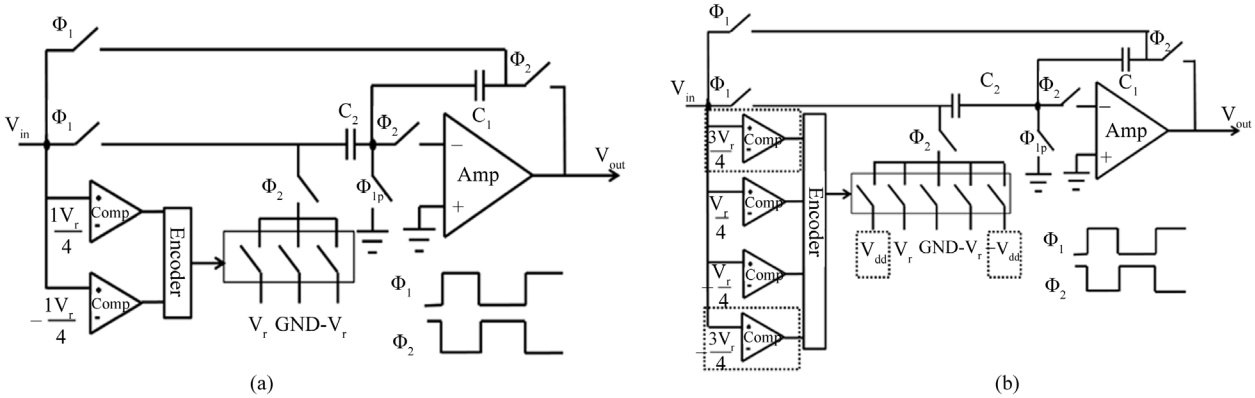

Figure 5. (a) Circuit implementation based on the traditional 1.5-bit/stage ADC and (b) Crcuit implementation based on the five-domain 1.5-bit/stage ADC.

ferential, $-V_{ref}$ can be realized by connecting the ground to the positive input side of the amplifier and the V_{ref} to the negative input side of the amplifier in both configurations. The realization of $-V_{dd}$ is similar to the realization of $-V_{ref}$. In the digital domain, only several dislocation and subtraction blocks need to be added.

3. Simulation Results

In order to demonstrate the effectiveness of the domain extension algorithm, a 10-bit pipeline ADC was simulated in MATLAB. The ADC consisted of eight five-domain 1.5-bit/stage converters and a 2-bit flash ADC. In the simulation, all absolute values of comparator offsets were set to $|3V_{ref}/8|$, input frequency was set to 45-MHz, and sample rate was set to 100-MS/s. The Fast Fourier Transform (FFT) plot of this simulation using the traditional method is shown in **Figure 6(a)**. The dynamic performance as shown in the FFT plot is recorded as 34.62-dB SFDR, 34.63-dB THD, and 30.33-dB SNR. **Figure 6(b)** shows the FFT plot using the domain extension algorithm. In this case, the ADC achieves a dynamic performance of 60.23-dB SFDR, 61.14-dB THD, and 59.35-dB SNR. The resulting improvements are then 25.61-dB, 26.51-dB, and 29.02-dB for SFDR, THD, and SNR respectively.

The simulated dynamic performance of the ADCs at an 100-MS/s sample rate and a 45-MHz input frequency is summarized in **Figure 7**. The absolute values of the comparator offsets are from 0 to $|0.4V_{ref}|$. As shown in **Figure 7(a)**, SFDR, THD, and SNR decrease minimally from the low comparator offsets to the absolute values of comparator offsets of $|V_{ref}/4|$. However, they decrease significantly when the absolute values of comparator offsets are higher than $|V_{ref}/4|$, because the traditional digital error correction technique can only correct the absolute values of compactor offsets lower than $|V_{ref}/4|$. As shown in **Figure 7(b)**, SFDR and THD decrease minimally from the low comparator offsets to the absolute values of comparator offsets of $|3V_{ref}/8|$, because the lease significant bit (LSB) cannot be corrected and the bit error rate (BER) increases with the increased comparator offsets.

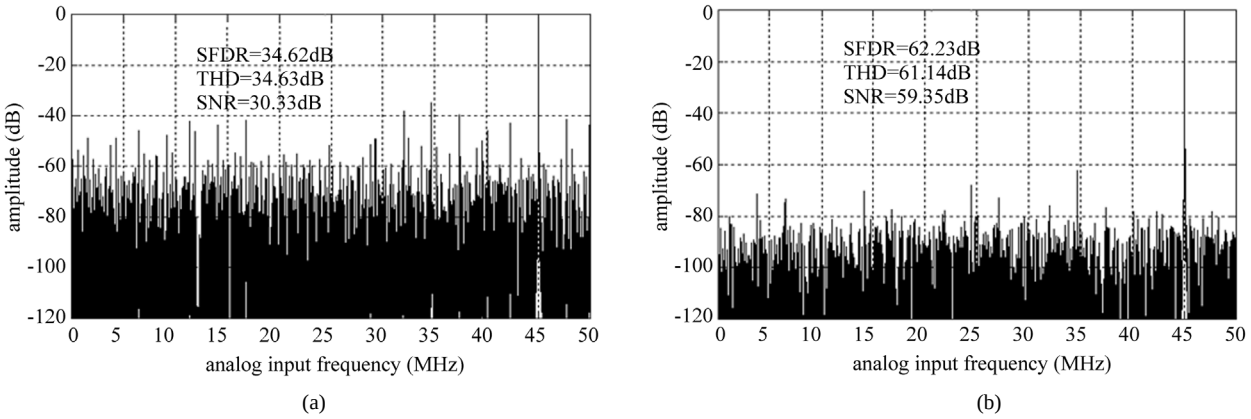

Figure 6. FFT plots of a 10-bit pipeline ADC using (a) the traditional digital error correction technique and (b) the proposed algorithm.

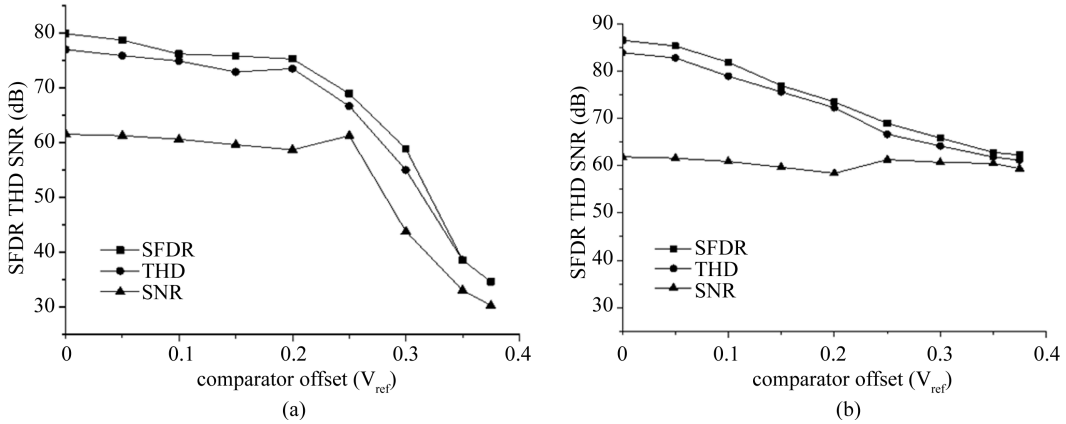

Figure 7. Simulated dynamic performance using (a) the traditional digital error correction technique and (b) the proposed algorithm.

4. Conclusion

The decrease of the transistor geometry causes problematic mismatches in width, length and threshold voltage, which leads to significant comparator offsets. These comparator offsets, in turn, greatly limit the performance of ADCs. However, the traditional digital error correction technique can only correct the absolute value of comparator offsets lower than $\left|V_{\text{ref}}/4\right|$. Therefore, in order to improve the comparator offset toleration ability, a domain extension algorithm has been presented, which can correct the absolute value of comparator offsets within $\left|3V_{\text{ref}}/8\right|$. This new approach involves minor analog and digital modifications and increases the comparator offset toleration ability by 50% with overflow/underflow judgment. Simulation results have revealed significant improvements of SFDR, THD and SNR performance.

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