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Scientific Research

New Electronically-Controllable Lossless Synthetic Floating Inductance Circuit Using Single VDCC

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ABSTRACT

A new electronically-controllable lossless floating inductance (FI) circuit (without any matching condition) has been presented, which employs only one Voltage Differencing Current Conveyor (VDCC), one grounded capacitor and one grounded resistor. The main aim of the paper is to present a new floating inductance simulator using single active device with minimum passive components. The proposed floating inductance simulator can be electronically controllable by changing the bias current. The workability of the new presented FI circuit has been verified using SPICE simulation with TSMC CMOS 0.18 µm process parameters.

KEYWORDS

VDCC; Floating Inductance Simulation; Filters

1. Introduction

Although many circuits for the simulation of grounded and floating inductance using different active building blocks such as operational amplifiers [1-5], current conveyors [6-13], current feedback amplifiers [14,15], current differencing buffered amplifiers [16,17], current differencing transconductance amplifiers [18,19], operational transconductance amplifiers [20,21], operational mirrored amplifiers [22], voltage differencing differential input buffered amplifiers [23,24], and voltage differencing transconductance amplifier [25] have been reported in the literature. In [26], many active building blocks have been presented, and VDCC is one of them. The usefulness of recently introduced active building block "VDCC" is well-defined in [27]. In [27], the authors proposed grounded inductance simulator circuits using single VDCC and two passive components. To the best knowledge of the author, no floating inductance simulator circuit using single VDCC and two passive components has been reported in the open literature so far.

Therefore, the main objective of this paper is to propose a new circuit which employs one VDCC, one grounded capacitor and one grounded resistor to realize electronically-controllable lossless matchless FI circuit. The presented circuit has also the features like only two passive components (*i.e.* one grounded capacitor (as desired for IC implementation) and one grounded resistor) and low active and passive sensitivities. The validity of the presented new circuit has been verified using SPICE simulation with TSMC CMOS 0.18 µm process parameters.

2. The Proposed New Configuration

The symbolic notation of recently proposed active building block, VDCC is shown in **Figure 1**, where P and N are input terminals and Z, X, W_P and W_N are output terminals. All of the terminals exhibit high impedance, except the X terminals [27]. The VDCC is characterized by the Equation (1).

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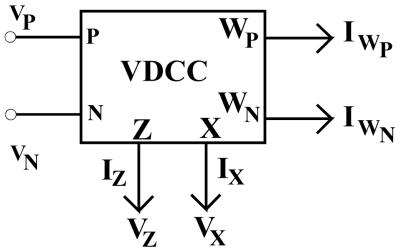

Figure 1. **The symbolic notation of VDCC.**

$$\begin{bmatrix} I_N \\ I_P \\ I_Z \\ V_X \\ I_{W_P} \\ I_{W_N} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \\ I_X \end{bmatrix} \quad (1)$$

The proposed FI circuit is shown in **Figure 2**.

A routine circuit analysis of the new FI circuit shown in **Figure 2** yields

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{g_m}{sCR} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad (2)$$

which shows that the circuit simulates a floating lossless electronically-controllable inductance with the inducbtance value given by

$$L_{eq} = \frac{CR}{g_m} \quad (3)$$

3. Non-Ideal Analysis and Sensitivity Performance

The proposed FI circuit consisting various non-ideal parasitics is shown in **Figure 3**. The X-terminal parasitic impedance consisting of a resistance R_{p_2} in series with inductance L_x, the parasitic impedance at the W_P-terminal consisting of a resistance R_{p_1} in parallel with capacitance C_{p_1}, the parasitic impedance at the W_N-terminal consisting of a resistance R_{p_4} in parallel with capacitance C_{p_4} and the parasitic impedance at the Z-terminal consisting of a resistance R_{p_3}.

For the circuit shown in **Figure 3**, the input-output currents and voltages relationship is given by

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = X \begin{bmatrix} 1+\dfrac{sC_{p_4}+\dfrac{1}{R_{p_4}}}{X} & -1 \\ -1 & 1+\dfrac{sC_{p_1}+\dfrac{1}{R_{p_1}}}{X} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad (4)$$

where

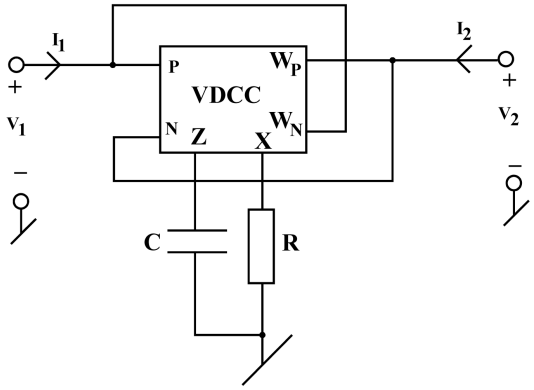

Figure 2. **Proposed FI circuit.**

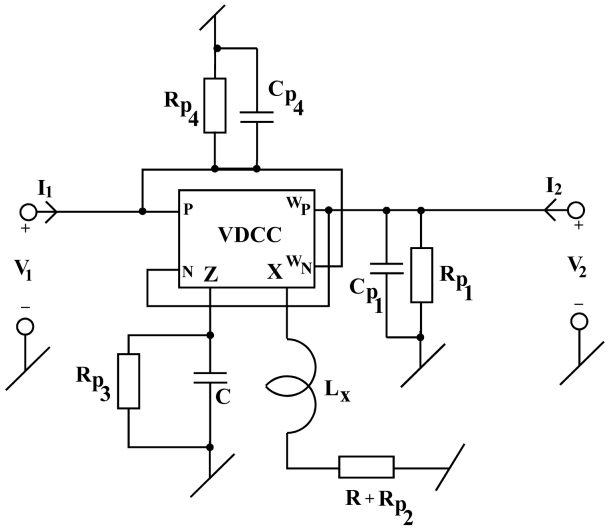

Figure 3. **Proposed FI circuit including parasitic.**

$$X = \left(\frac{1}{s^2 \dfrac{L_x C}{g_m} + s\left(\dfrac{C\left(R+R_{p_2}\right)}{g_m} + \dfrac{L_x}{R_{p_3} g_m} \right) + \left(\dfrac{R+R_{p_2}}{R_{p_3} g_m} \right)} \right)$$

The non-ideal equivalent circuit of FI of **Figure 3** is derivable from Equation (4) and is shown in **Figure 4**.

Where $L_{FI} = \dfrac{CR}{g_m}$ and $R = \dfrac{R+R_{p_2}}{R_{p_3} g_m}$, $D = \dfrac{L_x C}{g_m}$,

$$L = \frac{C\left(R+R_{p_2}\right)}{g_m} + \frac{L_x}{R_{p_3} g_m}$$

The various sensitivities of L_{FI} with respect to active and passive elements are:

$$S_C^{L_{FI}} = 1, S_{g_m}^{L_{FI}} = -1, S_R^{L_{FI}} = 1 \quad (5)$$

Thus, all the passive and active sensitivities of FI circuit are low.

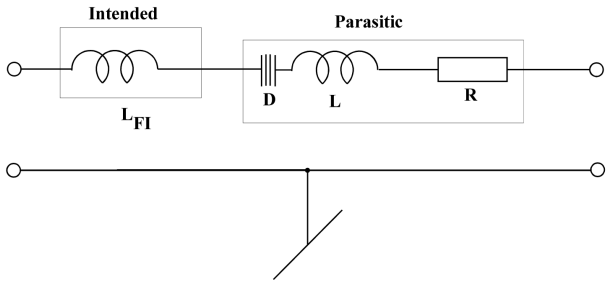

Figure 4. Non-ideal equivalent circuit of Figure 3.

4. Application Examples of New FI Circuit

The workability of the proposed FI circuits are demonstrated by realizing (i) a band pass filter (BPF) (**Figure 5**) and (ii) a fourth order Butterworth low pass filter with a cutoff frequency 500 kHz was designed using the normalised proto-type shown in **Figure 6** [15].

The transfer function realized by the configuration shown in **Figure 5** is given by

$$\frac{V_0}{V_{in}} = \frac{s\left(\frac{g_m}{C_1}\right)}{s^2 + s\left(\frac{g_m}{C_1}\right) + \frac{g_m}{C_1 C_2 R_2}} \qquad (6)$$

From Equation (6), it is clear that centre frequency is tunable by R_2.

The performance of the proposed FI circuit was verified by SPICE simulations. The frequency response of the FI circuit was obtained by using CMOS-based VDCC [27]. The following values were used for FI circuit: C = 0.01 nF, g_m = 277.833 µA/V, R = 10 kΩ. From the frequency response of the simulated FI circuit (**Figure 7**) it has been observed that the inductance value remains constant upto 10 MHz.

The application circuits shown in **Figures 5** and **6** were also been simulated using CMOS VDCCs. The component values used were for **Figures 5**: C_1 = 0.01 nF, C_2 = 0.02 nF, R_1 = 10 kΩ, R_2 = 3.6 kΩ, g_m = 277.833 µA/V and for **Figure 6**: $R_S = R_L$ = 1 KΩ, L_{1d} = 0.2437 mH (g_m = 277.833 µA/V, C_1 = 0.01 nF, R_1 = 6.77 kΩ), L_{2d} = 0.5884 mH (g_m = 277.833 µA/V, C_2 = 0.01 nF, R_1 = 16.225 kΩ), C_{1d} = 0.5884 nF, C_{2d} = 0.2437 nF (after appropriate frequency and impedance scaling). The VDCC were biased with ±0.9 volts D.C. power supplies with I_{B1} = 50 µA (for g_m = 277.833 µA/V). **Figures 8** and **9** show the simulated band pass filter and 4th-order Butterworth filter responses respectively. A comparison of proposed FI with other published floating inductor is shown in **Table 1**.

Thus, the above simulation results confirm the validity of the applications of the proposed FI circuit.

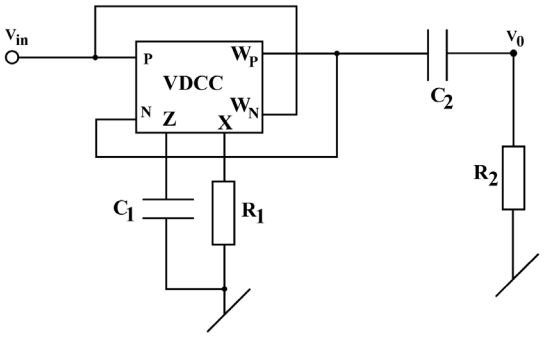

Figure 5. Band pass filter realized by the new FI circuit of Figure 2.

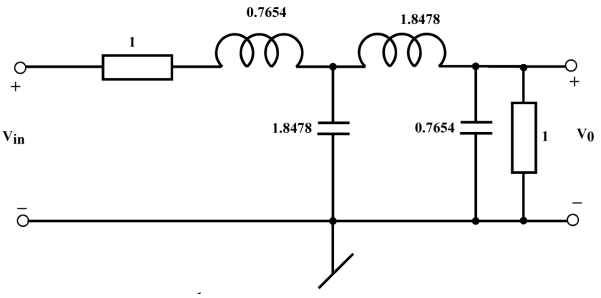

Figure 6. Normalised 4th-order Butterworth Low Pass Filter.

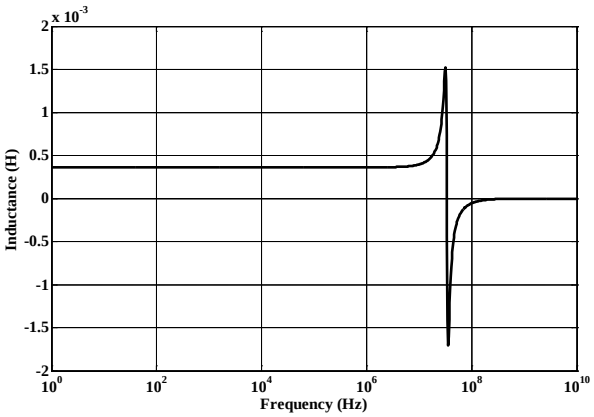

Figure 7. Frequency response of the simulated floating inductor.

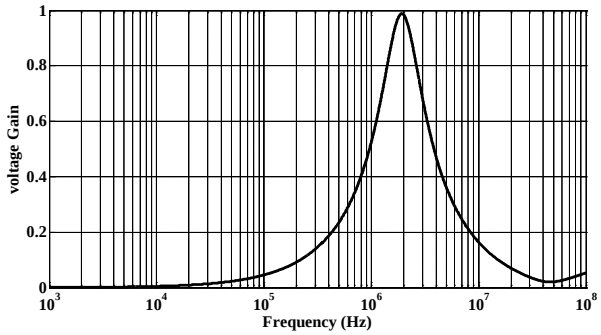

Figure 8. Frequency response of BPF using the proposed simulated FI.

Table 1. Comparison of proposed FI circuit with other previously published floating inductors.

Reference	Induct-ance type	No. of active device used	No. of resistors	No. of capacitors	Matching condition required	Whether electronically controllable
[4]	Floating	3	3	1	Yes	No
[6]	Floating	3/2	2	1	No	No
[7]	Floating	4	4	1	Yes	No
[8]	Floating	4	3	1	Yes	No
[9]	Floating	4	2	1	No	No
[10]	Floating	4	2	1	No	No
[11]	Floating	2	2	1	No	No
[15]	Floating	2	3	2	Yes	No
[16]	Floating	3/4	4	1	Yes	Yes
[17]	Floating	3	0	1	Yes	Yes
[18]	Floating	3	0	1	Yes	Yes
[22]	Floating	3	2	1	No	No
[25]	Grounded	1	0	1	No	Yes
	Floating	2	0	1	Yes	Yes
[23]	Grounded	1	1	1	No	Yes
	Floating	2	2	2	Yes	Yes
Proposed	**Floating**	**1**	**1**	**1**	**No**	**Yes**

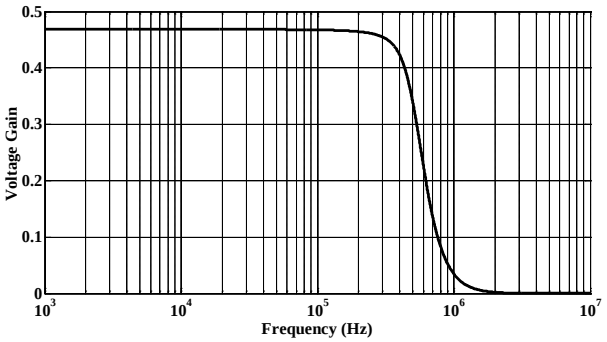

Figure 9. Frequency response of 4th-order Butterworth LPF.

5. Conclusions

A new electronically-controllable loss-less FI circuit without any matching condition has been proposed which employs one VDCC, one grounded capacitor and one grounded resistor. The proposed circuit offers the following advantageous features: 1) only two passive components *i.e.* one grounded capacitor (as desired for IC implementation) and one grounded resistor; 2) no matching condition; 3) fully electronically controllable (by changing bias currents); and 4) low active and passive sensitivities. The SPICE simulation results have confirmed the workability of the new proposed floating inductance circuit.

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