

Design of Low Power Comparator Using DG Gate

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ABSTRACT

In recent studies, reversible logic has emerged as a great scene of research, having applications in low power CMOS circuits, optical computing, quantum computing and nanotechnology. The classical logic gates such as AND, OR, EXOR and EXNOR are not reversible. In the existing literature, reversible sequential circuits designs are offered that are improved for the number of the garbage outputs and reversible gates. Minimizing the number of garbage is very noticeable. In the present paper, we show a design of the reversible comparator based on the quantum gates implementation of the reversible DG gate. The reversible DG gate is designed by using 3×3 quantum gates such as NOT, CNOT, Controlled-V and Controlled-V⁺ gates. Also, we have used the TR gate and various types of quantum gates in the implementation results. Low power three-bit comparator is designed using DG Gate, New Gate and Fredkin Gate. In order to evaluate the benefit of using the DG gate proposed in this paper, one-bit comparator is constructed. The design is useful for the future computing techniques like quantum computers. The proposed designs are implemented using VHDL and functionally investigated using Quartus II simulator.

KEYWORDS

Reversible Logic Comparator; TR and DG Gate; Quantum Cost; Garbage Output

1. Introduction

Conventional combinational logic circuits dissipate heat for every bit of information that is lost during their operation [1]. According to Landauer's principle, each bit of data lost produces $kT \ln 2$ joules amount of heat, where k is Boltzmann's constant and T is the absolute temperature at which the operation is implemented [2]. Moore's law [3] previes exponential growth of the heat generated due to the information loss, which will be a significant amount of heat loss in the next decade.

Bennett [4] illustrated that zero energy dissipation would be possible only if the network based on reversible gates. Hence, reversibility will become a necessary property in future circuit design.

There are two Boolean constants, 0 and 1. Reversible circuits are those circuits that do not lose information.

These circuits can produce single output vector from

each input vector, and conversely, there was a one-to-one mapping between output and input vectors. Hence, an $N \times N$ reversible gate can be represented as:

$$I_v = (I_1, I_2, I_3, I_4, \dots \dots \dots I_N)$$

$$O_v = (O_1, O_2, O_3, \dots \dots \dots O_N)$$

where I_v and O_v can be shown the input and output vectors respectively; the significant cost metrics in the synthesis of reversible logic circuits are the number of garbage outputs, delay and quantum cost [5,6]. Any unitary operation must be reversible. Thus, quantum networks effecting primary arithmetic operations such as addition, multiplication and exponentiation cannot be directly inferred from their classical Boolean counterparts (classical logic gates such as AND or OR or EXOR are irreversible). Therefore, Quantum Arithmetic must be made from reversible logic combinations [7]. Various gates have been proposed over the last decades. Among them are the

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controlled-not (CNOT) introduced by Feynman [8] Toffoli [9], and Fredkin [10] gates. Digital Comparator is a combinational circuit that compares two inputs binary quantities (A and B) and produces outputs to indicate whether the inputs are equal or which input is greater than the other. Therefore, the circuit has three outputs to indicate whether $A = B$, $A > B$ or $A < B$.

In this paper, we present various designs of a three-bit comparator circuit using existing reversible logic gates. The present paper proposed a new gate, called reversible DG gate which was used in the design of comparator. All the comparators have been modeled and investigated using VHDL and Quartus II.

2. Basic Reversible Gates

The detailed cost of a reversible gate associates with any specific realization of quantum logic. A short description of the gates are given below.

A. The NOT Gate

A NOT gate is a 1×1 gate performed as shown in **Figure 1(a)**. It has quantum cost of 1.

B. The Controlled-V and Controlled- V^+ Gates

The Quantum cost of a Reversible gate is computed by counting the number of V , V^+ and CNOT gates [11]. The controlled- V and V^+ gates are shown in **Figures 1(b)** and **(c)**.

The Controlled- V and Controlled- V^+ quantum gates have some properties that are shown below:

$$\begin{cases} V \times V = NOT \\ V \times V^+ = V^+ \times V = I \\ V^+ \times V^+ = NOT \end{cases}$$

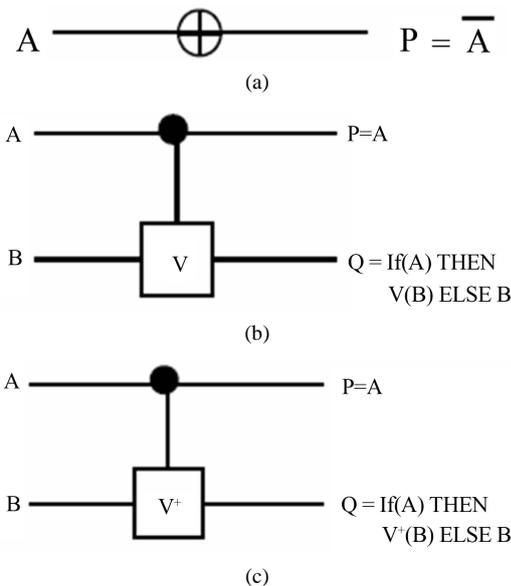


Figure 1. (a) Not gate; (b) Controlled- V gate; (c) Controlled- V^+ gate.

These equations depict that two V or V^+ gates in series are equivalent to a NOT gate; and two V and V^+ in series, are equivalent a BUFFER gate.

C. Feynman Gate

The most popular (2, 2) one-through reversible gate is the Feynman gate [8]. The logical functions performed by a Feynman gate with input vector (A, B) and output vector (P, Q) are represented in **Figure 2**.

The input double (A, B) depends on its output double (P, Q) as follows.

$$P = A; Q = A \oplus B;$$

If $A = 0$ then Q would be equal to B . If $A = 1$ then showed the complement of the input (B).

Hence, it is called as quantum XOR and also called as CNOT (1-NOT).

D. Fredkin gate

Fredkin gate [10], depicted in **Figure 3**, is a (3, 3) reversible gate which penetrates $P = A$, $Q = A'B \oplus AC$ and $R = A'C \oplus AB$ where (A, B, C) is the input vector and (P, Q, R) is the output vector.

Figures 4(a) and **(b)** offer the performance of the Fredkin gate as AND and OR functions respectively.

E. New gate

The New gate [12] is a (3, 3) reversible gate. The most significant aspect of this gate is that it can work as a universal gate.

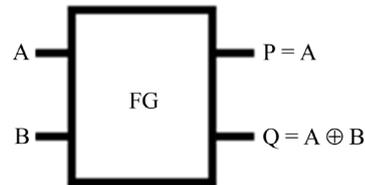


Figure 2. Feynman gate.

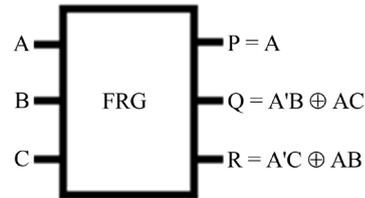


Figure 3. Fredkin gate.

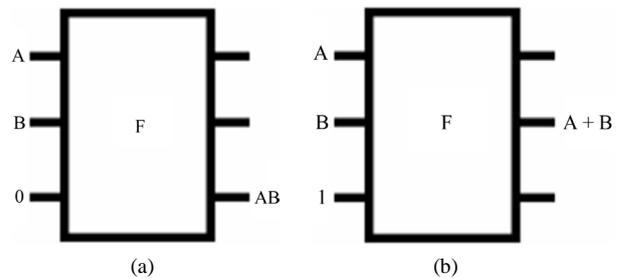


Figure 4. Fredkin gate as (a) AND function; (b) OR function.

The New gate is one of the most popular reversible as represented in **Figure 5**.

F. BVF gate

This is a (4, 4) reversible logic gate [13] shown in **Figure 6** with input vector I (A, B, C, D) and the output vector is O (P, Q, R, S). This can be used for duplication of the required inputs to meet the fan-out requirements. This gate can be specified by $P = A$, $Q = A \oplus B$, $R = C$ and $S = C \oplus D$.

G. TR gate

Recently Thapliyal and Ranganathan in [14] have proposed a new design of the reversible full subtractor based on the offered quantum gates implementation of the TR gate. TR gate with quantum cost of 4. The quantum cost of TR gate is 4 since it requires 1 V^+ gates, 2 V gate and 1 CNOT gate in its structure.

TR gate and Quantum implementation of TR gate have represented in **Figures 7(a)** and **(b)** respectively.

3. Proposed Gate

This paper presents a new (3, 3) reversible gate, “DG”,

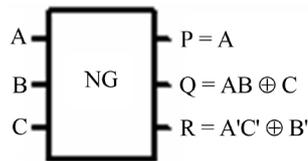


Figure 5. New gate.

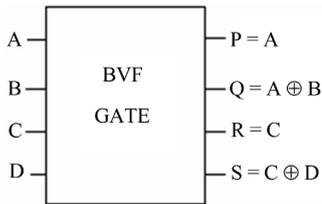


Figure 6. BVF gate [13].

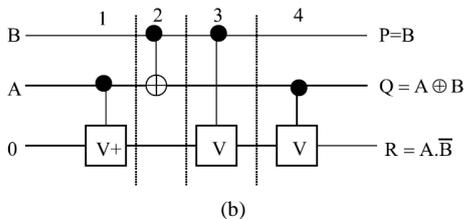
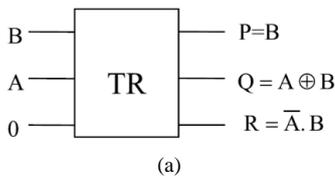


Figure 7. (a) TR gate as a reversible half subtractor; (b) Quantum implementation of TR gate based reversible half subtractor.

with inputs (A, B, C) and outputs $P = A$, $Q = (A \oplus B)'$, $R = AB' \oplus C$ that is shown in **Figure 8(a)**. The gate is one-through, which means one of the input variables is also output. The corresponding truth table of DG gate is shown in **Table 1**. **Figure 8(b)** shows the quantum implementation of the DG with quantum cost of 5. The corresponding truth table of the DG gate is shown in **Table 1**.

4. Design of the Three Bit Comparator

The two numbers are equal if all pairs of significant digits are equal; meaning $A_3 = B_3$ and $A_2 = B_2$ and $A_1 = B_1$.

To check for this equality, we use the XNOR gate as we did previously.

So we have seen three bit comparator ($A = B$) using classical gates as shown in **Figure 9**.

In the same way, the following classical gate $A > B$ can be considered for a three bit comparator which is shown in **Figure 10**.

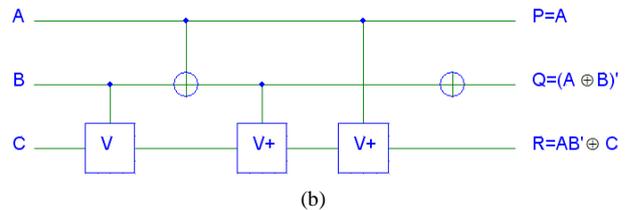
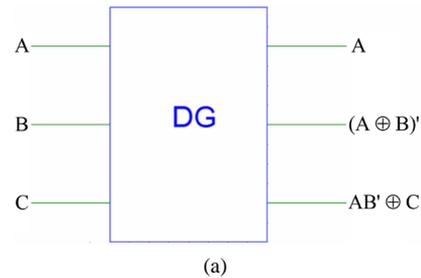


Figure 8. (a) DG gate; (b) Quantum implementation of DG gate.

Table 1. Truth table for the DG gate.

A	B	C	P	Q	R
0	0	0	0	1	0
0	0	1	0	1	1
0	1	0	0	0	0
0	1	1	0	0	1
1	0	0	1	0	1
1	0	1	1	0	0
1	1	0	1	1	0
1	1	1	1	1	1

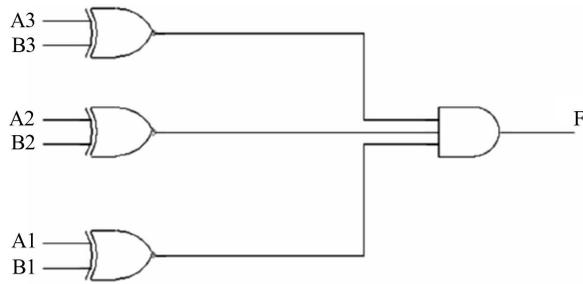


Figure 9. Three bit comparator (A = B) using classical gates.

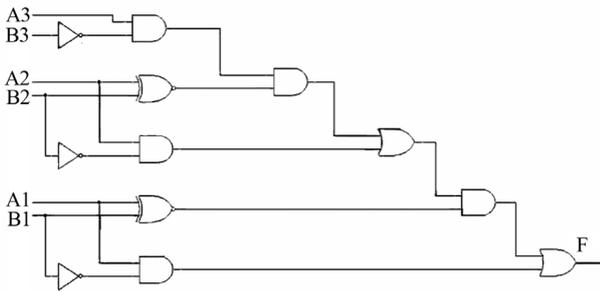


Figure 10. Three bit comparator (A > B) using classical gates.

If we want to have the output $A = B$, DG and BVF Gates can be used. The results are shown in Figure 11. Table 2 shows the evaluation of the mentioned circuit.

Two DG Gates can be put instead of BVF Gate to reduce the number of gates. The results are shown in Figure 12. Table 3 shows the evaluation of the mentioned circuit.

Reversible three bit comparator is implemented with various types of reversible logic gates as shown in Figures 13 and 14 respectively.

The proposed circuit of the three bit comparator is evaluated in terms of number of reversible gates used and garbage outputs generated. Tables 4 and 5 show the evaluation of the proposed circuits.

The results show that DG gate reduces the number of gates and garbage outputs.

In the proposed one-bit comparator design, we have investigated $FA > B$ and $FA = B$ and the third condition $FA < B$ is produced from the first two outputs. Therefore the design recitation leads to

$$FA > B = AB'$$

$$FA = B = (A \oplus B)'$$

$$FA < B = (AB')'((A \oplus B)')$$

The results are shown in Figure 15. DG gate is used in Figure 15 where DG and NG are used in Figure 10.

Figure 16 has less garbage outputs but in Figure 15, there are EXOR and EXNOR gates in outputs concur-

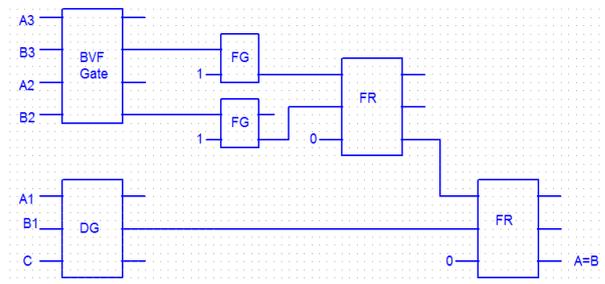


Figure 11. One bit (A = B) using BVF, DG Gates.

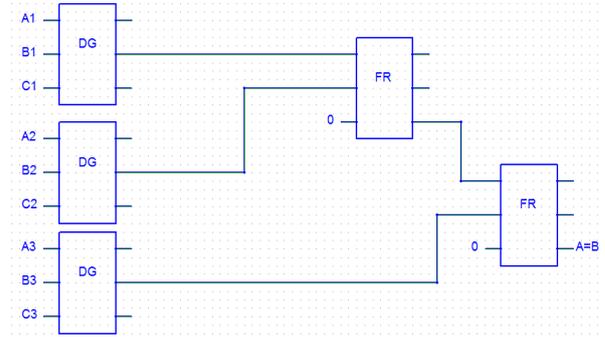


Figure 12. One bit (A = B) using DG gate.

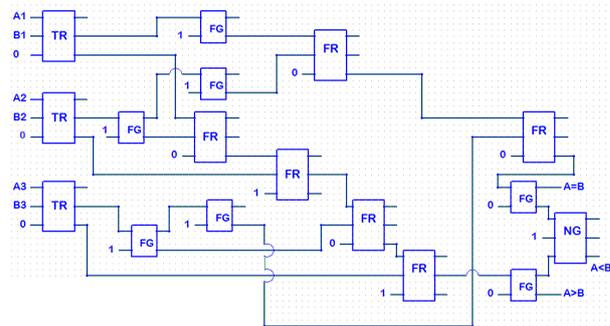


Figure 13. Three bit comparator using TR gate.

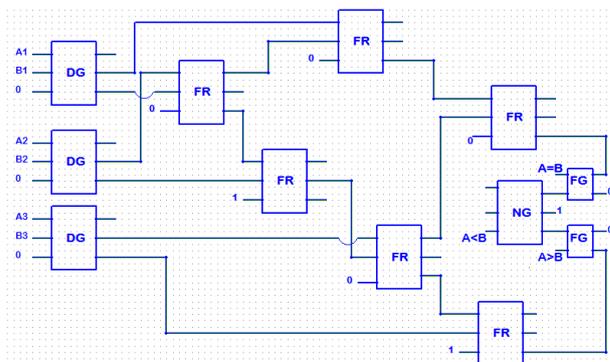


Figure 14. Three bit comparator using DG gate.

Table 2. Evaluation of the proposed comparator.

Figure 11	No of gates	Garbage Outputs
Proposed Circuit	6	10

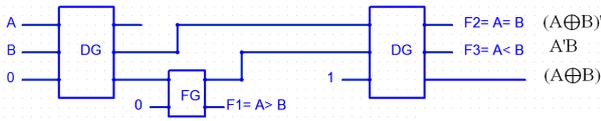


Figure 15. One bit comparator using DG gate.

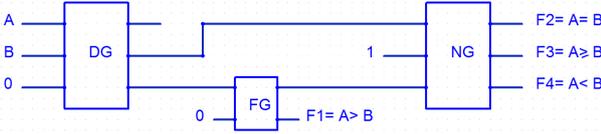


Figure 16. One bit comparator using DG gate and NEW gate.

Table 3. Evaluation of the proposed comparator.

Figure 12	No of gates	Garbage Outputs
Proposed Circuit	5	10

Table 4. Evaluation of the proposed comparator.

Figure 13	No of gates	Garbage Outputs
Proposed Circuit	17	20

Table 5. Evaluation of the proposed comparator.

Figure 14	No of gates	Garbage Outputs
Proposed Circuit	12	15

rently. Tables 6 and 7 show the evaluation of the proposed circuits.

In the mentioned paper one bit comparator has better function in comparison with Nagamani *et al.* Figure 17 is selected as follows, in Nagamani *et al.*

A good synthesis for reversible logic should not create an excessive “garbage” or “waste of outputs”. Hence, the components are chosen so that the designed scheme has the desired characteristics. One bit comparator can be represented by 2 DG gates and 1 FG gate, as shown in Figure 18. This structure can be utilized for testing outputs 1 and 3 (AB'). DG gate operates as a signal copying that shown in Figure 18. The corresponding table of mentioned circuit is shown in Table 8. The (A'B) output of the Figure 18 is given by the equation:

$$F = A'B = [AB' \oplus (A \oplus B)]'$$

Figure 18 has better performance because of similarity gates and two same outputs. Although garbage outputs seems zero. Table 8 shows the evaluation of the mentioned circuit.

Two same outputs of this Figure can be used for concurrent error detection.

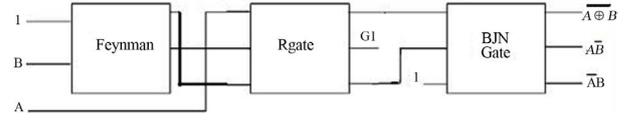


Figure 17. One bit comparator using R gate and BJJ gate [1].

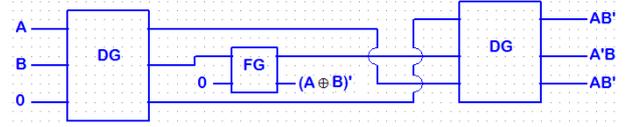


Figure 18. One bit comparator using DG gate.

Table 6. Evaluation of the proposed comparator.

Figure 15	No of gates	Garbage Outputs
Proposed Circuit	3	2

Table 7. Evaluation of the proposed comparator.

Figure 16	No of gates	Garbage Outputs
Proposed Circuit	3	2

Table 8. Evaluation of the proposed comparator.

Figure 18	No of gates	Garbage Outputs
Proposed Circuit	3	0

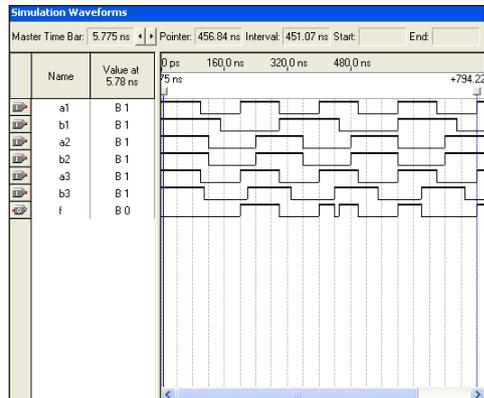
5. Simulation Results

Reversible logic gates are extensively known to be compatible with future computing technologies which approximately dissipate zero heat [15]. For example, Reversible three bit comparators offered using VHDL and Simulated using Quartus II Simulator. Simulation results are shown in Figures 19(a) and (b). For one bit comparator using DG gate result shown in Figure 19(c).

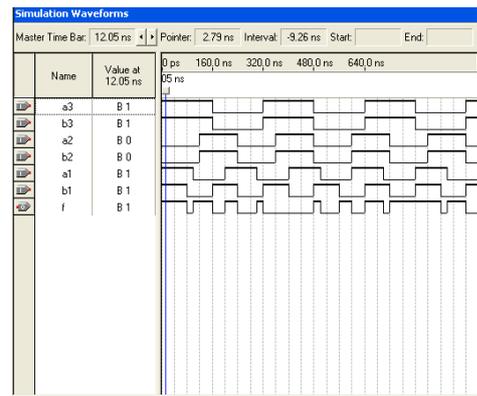
6. Discussions and Conclusions

Conventional computers generate heat and waste much energy. In order to make a computer faster and lower power, consumption proposed reversible logic gates. In this paper, we have presented new designs of reversible one and three-bit comparators based on the quantum gates implementation of the reversible TR and DG. The main goal of this paper is optimized in terms of number of garbage outputs, gate count and quantum cost for comparator designs. The proposed DG gate can be combined with TR gate and various types of reversible logic gates to design minimal quantum cost and garbage less reversible circuits.

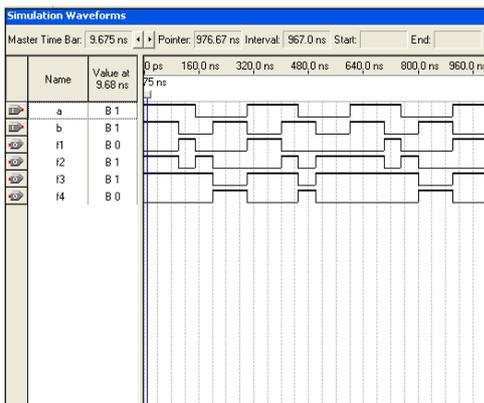
The newly proposed DG gate can be used for imple-



(a)



(b)



(c)

Figure 19. (a) Three bit comparator $a > b$; (b) Three bit comparator $a = b$; (c) one bit comparator using DG gate.

menting concurrent EXOR and EXNOR output functions. Hence, three outputs of DG gate have efficient results for comparator designs. In this paper, one-bit comparator has better performance comparatively.

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