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Current Mode Logic Testing of XOR/XNOR Circuit: A Case Study

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ABSTRACT

This paper investigates the issue of testing Current Mode Logic (CML) gates. A three-bit parity checker is used as a case study. It is first shown that, as expected, the stuck-at fault model is not appropriate for testing CML gates. It is then proved that switching the order in which inputs are applied to a gate will affect the minimum test set; this is not the case in conventional voltage mode gates. Both the circuit output and its inverse have to be monitored to reduce the size of the test set.

Keywords: Current Mode Logic (CML); CMOS; Testing; Stuck-At Faults

1. Introduction

Static CMOS logic style is commonly used in the design of digital integrated circuits due to its advantages such as very low static power dissipation, high packing density and wide noise margins. However, this logic family is highly susceptible to environmental noise sources [1]. Also, its maximum operating frequency is orders of magnitudes less than f_T of the MOS device. It also suffers from large dynamic power dissipation at high frequencies.

High speed logic circuits usually use current mode logic (CML) design. First, bipolar transistors were used to implement this type of logic [2]. Currently, CML is most commonly used.

Designing a high-speed CMOS circuit operating near f_T of the MOS device is very challenging. System blocks in a Giga-bit communication system need to be realized by very simple circuits utilizing minimum number of active devices. High-speed signal processing circuits in a communication transceiver should not use PMOS devices due to their inferior unity-gain frequency. Additional design constraints are needed for very high speed signal processing. On the other hand, buffers are the circuit core of many high-speed blocks within a communication transceiver and a serial link. Front-end tapered buffer chain, serial-to-parallel converters, clock and data

recovery (CDR), multiplexers and demultiplexers all use high-speed buffers with a robust performance in the presence of noise. The electromagnetic coupling causes serious operational malfunctioning in the circuits, particularly single-ended circuits [3,4].

The CML circuits can operate with lower signal voltage and higher operating frequency at lower supply voltage than CMOS circuits can. Due to their superior performance, CML buffers are the best choice for high-speed applications. As a consequence, it is essential to have a systematic approach to optimally test CML gates.

In [5], testing for catastrophic open and short faults has been addressed on analog MOS current mode circuits. A CMOS transconductor testing has been introduced using 0.18 µm technology provided by MOSIS. The circuit was modeled in PSPICE and five faults per transistor are assumed. A single fault was injected into the circuit at a time. The total fault coverage was 93%. In [6], the same circuit has been tested using 90nm technology from MOSIS, modeled in PSPICE. This work considered six faults model per transistor. The total fault coverage was 94.4%.

In this paper, an attempt to test CML circuits is introduced. A 3-input parity checker will be studied and the minimum test set will be determined in order to obtain a 100% coverage. Five faults will be assumed per transis-

tor but only one fault will be assumed at a time [5,7-9]. The minimum test set is then compared to the one obtained in case of a similar circuit implemented with conventional voltage mode gates and assuming a single stuck-at fault at a time. It will first be shown that, as expected, the single stuck-at fault model is not appropriate for CML. It will then be shown (and this is the main contribution of this paper) that the order of input application to an Exclusive-Or gate may affect the size of the minimum test set. It is important to remember, however, that the results of this case study cannot be generalized since only one circuit and one type of gate, have been investigated.

The rest of this paper is organized as follows: Section 2 has the description of the circuit under test. Section 3 describes the testing methodology and the fault model used throughout this study. In Section 4, the ELDO simulation results are presented and the minimum test set is found. Finally, the paper is concluded in Section 5.

2. Description of the Circuit under Test

A three input parity checker circuit using two-input XOR gates is shown in **Figure 1**. For simplicity, the input vector will follow the format CBA and converted to decimal, *i.e.*, input vector 4 will refer to CBA = 100. A CMOS CML two-input XOR/XNOR gate is implemented as shown in **Figure 2** [10]. The circuit produces the output and its inverse. The MOS model uses the 90 nm technology from MOSIS. The supply and bias voltages are +1 V. Note that the third input (C) is connected to the lower transistors of the rightmost XOR gate (XOR2) but it could also be connected to the upper transistors. The

importance of this issue will be addressed later in this paper. In **Figure 1**, *Myx* refers to transistor x (1 - 9) in gate *y* (1 or 2). For example, M12 is transistor 2 in the leftmost XOR gate.

3. Testing Methodology

Several fault models are reported in the literature for MOS transistors [5,7-8]. In this paper, the five fault model will be used: Drain-Gate short circuit (DG), Drain-Source short circuit (DS), Source-Gate short circuit (SG), open circuit at Drain (OD) and open circuit at source (OS). The number of transistors is 9 transistors per gate and the circuit has two gates; hence, the total number of faults considered in this circuit is 90. Only one catastrophic fault is assumed at a time [7]. The two fault-free outputs of the circuit are applied to two CMOS inverters that represent the load. Alternatively, these two inverters can represent the front end of the Automatic Test Equipment (ATE). For every fault, the circuit outputs are compared to the fault-free outputs. The ELDO simulator from MENTOR Graphics is used in the analysis [11]. Both the XOR and XNOR outputs of the second gate are used in the comparison. For any input vector, if at least one output is different from the corresponding fault-free output, the fault is considered to be detectable by this input vector.
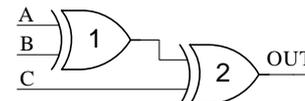
Figure 1. Three bit parity checker.
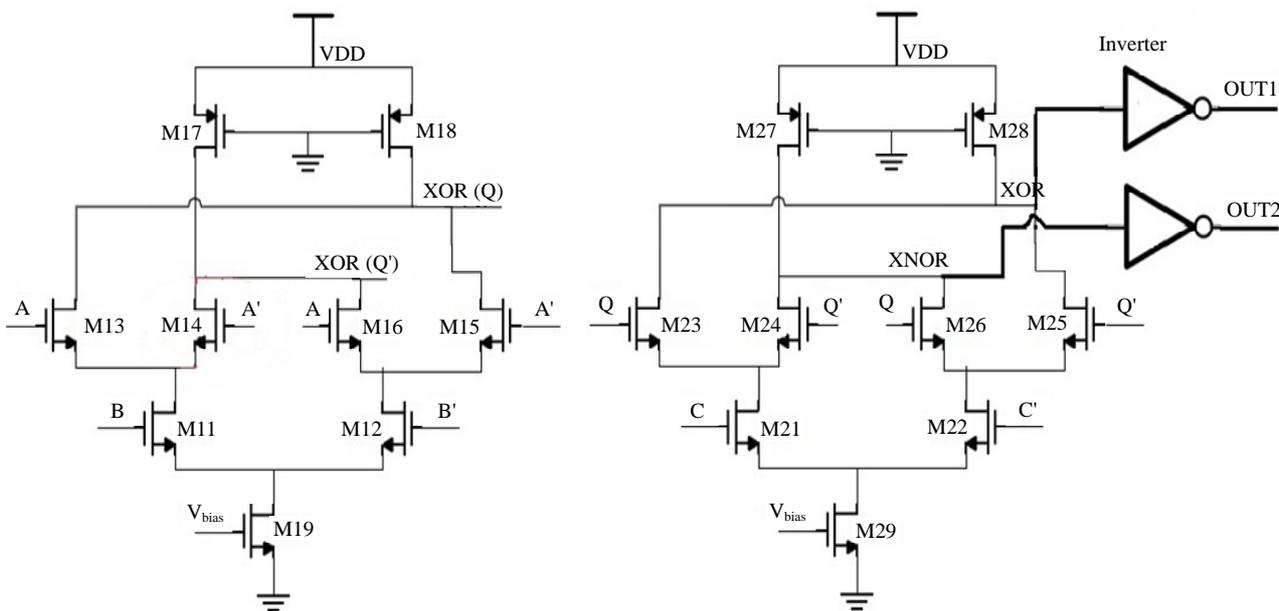
Figure 2. Transistor level circuit diagram.

It is observed that the XOR and XNOR outputs sometimes fall in the undefined region of the inverters representing the test equipment. In other words, the output voltage is higher that V_{il} and lower than V_{ih}. The inverter has $V_{il} = 0.5$ V and $V_{ih} = 0.6$V. Furthermore, the outputs of the circuit under test may be affected by noise. The noise amplitude level is usually $\pm5\%$ of the supply voltage, *i.e.*, 0.05 V in this study [12]. Hence, it will be assumed that any input vector producing an output voltage between 0.5 and 0.6 V for a specific fault cannot be used as a test vector for that fault because noise added to this output may toggle its digital value at the outputs of the inverters (front end of the test equipment). These unsafe input vectors will be excluded from the test set and only safe test vectors will be considered.

For example, **Table 1** has the results of the ELDO simulations for the circuit with faults in transistor M11. C and its inverse C' are connected to the lower transistors M21 and M22. The circuit is simulated with one fault at a time. For every fault, BI is the actual value of the voltage at the XOR/XNOR output and AI is the output of the inverter representing the front end of the test equipment. If AI is the incorrect logic value, the input vector is considered to have detected the fault. The rightmost two columns have the fault-free values for comparison. In **Table 1**, it is observed that there are several unsafe vectors. Any BI with a value between 0.5 V and 0.6 V indicates that the vector producing that value may not detect that specific fault. The SG fault may not be detected by input vector 7 (CBA = 111) because BI/OUT1 is 0.53 V. Noise on this output could increase it and cause the inverter output (AI) to switch from a logic 1 to a logic 0. The fault-free output of the circuit for input vector 7 being a logic 1, the output of the inverter should be a logic 0. Hence, the noise may cause the output of the inverter to be correct and the fault is not detected. Consequently, input vector 7 will be considered as an unsafe test vector that cannot detect the SG fault in M11.

4. Minimum Test Set

Table 2 shows the ELDO simulation results for all faults

Table 1. Simulation results for a sample fault that has unsafe vectors (C & C' connected to M21 & M22).

M11 results at out1 & out2 before Inverter (BI) & after Inverter (AI), all these values are relative to 1 V								
	DG (OUT1)		DS (OUT1)		SG (OUT1)		OD & OS (OUT1)		Fault free OUT1
CBA	AI	BI	AI	BI	AI	BI	AI	BI	AI (BI)
000 (0)	0	1	0	1	1	0.28	1	0.28	1 (0.28)
001 (1)	0	1	0	1	0	1	0	1	0 (1)
010 (2)	0	0.68	0	1	0	0.61	0	0.61	0 (1)
011 (3)	0	0.68	1	0.35	0	0.61	0	0.61	1 (0.28)
100 (4)	0	1	0	1	0	1	0	1	0 (1)
101 (5)	0	1	0	1	1	0.26	1	0.26	1 (0.28)
110 (6)	0	0.65	1	0.3	0.98	0.53	0.98	0.53	1 (0.28)
111 (7)	1	0.65	0	1	0.98	0.53	0.98	0.53	0 (1)
	DG (OUT2)		DS (OUT2)		SG (OUT12)		OD & OS (OUT2)		Fault free OUT2
CBA	AI	BI	AI	BI	AI	BI	AI	BI	AI (BI)
000 (0)	0	1	0	1	0	1	0	1	0 (1)
001 (1)	0	1	0	1	1	0.35	1	0.35	1 (0.33)
010 (2)	0	0.73	1	0.3	0	0.68	0	0.68	1 (0.33)
011 (3)	0	0.73	0	1	0	0.68	0	0.68	0 (1)
100 (4)	0	1	0	1	1	0.3	1	0.3	1 (0.33)
101 (5)	0	1	0	1	0	1	0	1	0 (1)
110 (6)	0	0.61	0	1	0.22	0.57	0.22	0.57	0 (1)
111 (7)	1	0.6	1	0.3	0.22	0.57	0.22	0.57	1 (0.33)

Table 2. Simulation results—OUT1 output (OUT2 output).

	DG	DS	SG	OD	OS
M11	0, 3, 4, 6 (1, 2, 5, 7)	1, 4 (0, 5)	3, 6 (2, 7)	3, 6 (2, 7)	3, 6 (2, 7)
M12	0, 2, 5, 7 (1, 3, 4, 6)	2, 7 (3, 6)	0, 5 (1, 4)	0, 5 (1, 4)	0, 5 (1, 4)
M13	2, 3 (6, 7)	2 (6)	3, 4 (0, 7)	3 (7)	3 (7)
M14	6, 7 (2, 3)	7 (3)	1, 6 (2, 5)	6 (2)	6 (2)
M15	1, 0 (4, 5)	1 (5)	0, 7 (3, 4)	0 (4)	0 (4)
M16	4, 5 (0, 1)	4 (0)	2, 5 (1, 6)	5 (1)	5 (1)
M17 & M27	1, 2 (-)	4, 7 (-)	-	1, 2 (-)	1, 2 (-)
M18 &M28	4, 7 (-)	1, 2 (-)	-	4, 7 (-)	4, 7 (-)
M19 & M29	0, 3, 5, 6 (-)	-	-	0, 3, 5, 6 (-)	0, 3, 5, 6 (-)
M21	1, 2 (5, 6)	0, 3 (4, 7)	1, 2 (5, 6)	1, 2 (5, 6)	1, 2 (5, 6)
M22	4, 7 (0, 3)	5, 6 (1, 2)	1, 2 (5, 6)	4, 7 (0, 3)	4, 7 (0, 3)
M23	- (1, 2, 5, 6)	1, 2 (1, 2)	0, 3 (5, 6)	- (5, 6)	- (5, 6)
M24	1, 2, 5, 6 (-)	5, 6 (5, 6)	1, 2 (4, 7)	1, 2 (-)	1, 2 (-)
M25	- (0, 3, 4, 7)	4, 7 (4, 7)	5, 6 (0, 3)	- (0, 3)	- (0, 3)
M26	0, 3, 4, 7 (-)	0, 3 (0, 3)	4, 7 (1, 6)	4, 7 (-)	4, 7 (-)

with C and its inverse connected to the upper transistors M23, M24, M25 and M26. For every fault and every transistor, this table has the safe input vector(s) that detect the fault at the XOR output (OUT1) followed by the safe input vector(s) that detect the same fault at the XNOR output (OUT2) between brackets.

It is observed that some faults are only detected at the XOR output while others are only detected at the XNOR output. Also, there are four faults in each XOR gate that cannot be detected, namely an SG fault in M17, M27, M18 and M28 as well as SG and DS faults in M19 and M29. An analysis of the SG fault in M17, for example, reveals that this fault forces the transistor to function as a resistor which is the intended function of the transistor. In other words, this SG fault did not affect the functionality of M17; consequently, this fault will be removed from the fault list. The same argument is valid for the other five transistors faults. In total, 8 faults will removed from the 90 faults assumed originally.

Further analysis of **Table 2** shows that the minimum test set consists of the vectors (0, 1, 6 and 7) for 100% coverage. A circuit implemented with conventional voltage mode XOR gates is then analysed. One single stuck-at fault is assumed at a time. A stuck-at-0(1) fault occurs when a signal always produces a 0(1) irrespective of the input vector applied to the circuit inputs. It is found that there are many minimal test sets for 100%coverage but all of them consist of three vectors. An example of a minimum test set is (0, 3 and 7). The obvious conclusion

here is that the single stuck-at fault model is not appropriate for this specific CML circuit, as expected. Remember that the stuck-at fault model treats a gate as a black box and focuses on inputs and outputs; the five fault model used in this paper modeled failures at the transistor level.

In the simulation setup described above, primary input "C" and its inverse were connected to the upper transistors (M23, M24, M25 and M26) of the second XOR gate. Another set of simulations were run where "C" and its inverse were connected to the lower transistors (M21 and M22) of the second XOR gate. It is important to note that, in practice, both two cases of input connections order are used. If high performance design is considered, "C" should be connected to the upper transistors of the second XOR in order to reduce delay. However, connecting "C" to the lower transistors of the second XOR gate is sometimes preferred in VLSI design because critical signals need to be close to the supply in order to decrease the effect of parasitic capacitance.

In this other set of simulations, the minimum test set depends on the aspect ratio of PMOS transistors (M17, M18, M27 and M28) $(W/L)_p$ relative to aspect ratios of NMOS transistors $(W/L)_n$. The relation between aspect ratios can be calculated from Equation (1) for symmetric voltage transfer characteristics and the following equations indicate that the circuit verifies the truth table of the parity checker when Equation (3) satisfied.

$$I_{DPMOS} = I_{DNMOS} \tag{1}$$

$$\frac{1}{2}\mu_p C_{ox}(W/L)_p(V_{GS} - V_{tp})^2$$
$$= \frac{1}{2}\mu_n C_{ox}(W/L)_n(V_{GS} - V_{tn})^2 \tag{2}$$

$$(W/L)_P < 2(W/L)_n \tag{3}$$

By analytical analysis, it is found that the minimum test set consists of input vectors 0, 1, 6 and 7 for the entire range. However, ELDO simulations indicate that, for the range of (*W/L*) indicated in Equation (4), an extra test vector is needed for 100% coverage, namely input vector 2.This is due to non idealities existing on the MOSFET model used in simulation and not considered in analytical analysis. Remember that only safe input vectors are used in the determination of the minimum test set.

$$1.65(W/L)_n < (W/L)_p < 1.73(W/L)_n \tag{4}$$

5. Conclusions

In this paper, a Current Mode Logic (CML) based three-bit parity checker is studied. It consists of two XOR gates. Five catastrophic faults are injected into each transistor, one at a time. The minimum test set is obtained for this circuit and then compared to a minimum test set obtained for the same circuit when implemented with conventional voltage mode gates and assuming one stuck-at fault at a time. It is found that the number of test vectors in the two test sets is different. This is an expected result.

The main contribution of this paper is that it is found that switching the inputs of an XOR gate affects the size of the minimum test set. A particular scenario is simulated and it is shown that the minimum test set consists of 4 vectors. When the inputs of one of the XOR gates are switched, the minimum test set increases from 4 test vectors to 5. All simulations were run on the ELDO simulation tool from Mentor Graphics.

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