Circuits and Systems, **2013, 4, 323-327**
http://dx.doi.org/10.4236/cs.2013.43044 Published Online July 2013 (http://www.scirp.org/journal/cs)

A CMOS 3.1 - 10.6 GHz UWB LNA Employing Modified Derivative Superposition Method

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Received October 19, 2012; revised January 7, 2013; accepted January 15, 2013

ABSTRACT

Low noise amplifier (LNA) performs as the initial amplification block in the receive path in a radio frequency (RF) receiver. In this work an ultra-wideband 3.1 - 10.6-GHz LNA is discussed. By using the proposed circuits for RF CMOS LNA and design methodology, the noise from the device is decreased across the ultra wide band (UWB) band. The measured noise figure is 2.66 - 3 dB over 3.1 - 10.6-GHz, while the power gain is 14 ± 0.8 dB. It consumes 23.7 mW from a 1.8 V supply. The input and output return losses (S11 & S22) are less than –11 dB over the UWB band. By using the modified derivative superposition method, the third-order intercept point IIP3 is improved noticeably. The complete circuit is based on the 0.18 μm standard RFCMOS technology and simulated with Hspice simulator.

Keywords: Broadband; Low-Noise Amplifier (LNA); Noise Figure; Ultra-Wideband (UWB); Modified Derivative Superposition Method

1. Introduction

Development of the high-speed wireless communication systems puts increasing request on integrated low-cost RF devices with multi-GHz bandwidth operating at the lowest power consumption and supply voltage. Ultra wide band (IEEE 802.15.3a) appears as a new technology capable for high data transfer rates (up to 1 Gb/s) within short distances (10 m) at low power. This technology uses for some application such as wireless personal area networks (WPANs), providing an environment for transmission of audio, video, and other high-bandwidth data [1]. The amplifier that is used for this application must meet several requirements. For example to interface with the preselect filter and antenna, the amplifier input impedance should be close to 50 over the desired UWB band. However sufficient gain with wide band width to overtop the noise of a mixer, low noise figure to improve receiver sensitivity, low power consumption to increase battery life, small die area to reduce the cost, unconditional stability and good linearity are important parameters. There is a close trade-off between them. There are some proposed solutions and circuits for each parameter [2-8]. However, some parameters would be ruined by improving the others [4]. In this research a new circuit has achieved via modifying these methods [1,9]. The main parameter in this research is noise figure which has noticeably improved in comparison with the other references. It is 2.66 - 3 dB over 3.1 - 10.6-GHz band width.

2. Input Stage

Common-gate and Cascode configurations are two kinds of methods usually used to design the input stage of LNA in CMOS circuits, while the Common-Gate and Cascode structure provides a wide-band and narrow-band input matching respectively. However Common-gate stage has an intrinsically high noise figure versus Cascode stage and the noise-canceling techniques must be used. In the narrow band application, a shunt inductor is added in the input stage to resonate with C_{gs} to enhance impedance matching at the desired frequency. However in most CMOS narrow band applications, cascode LNA with inductive degeneration is preferable but for isolating from the input to the output and omitting of the C_{gd} path, the Common-Gate LNA performs better reverse isolation and stability versus Common-Source LNA.

Numerical value for the lower bound is about 2.2 dB for long-channel devices and 4.8 dB for short channel devices.

3. Circuit Design and Analysis

The proposed wide-band LNA is shown in **Figure 1**.

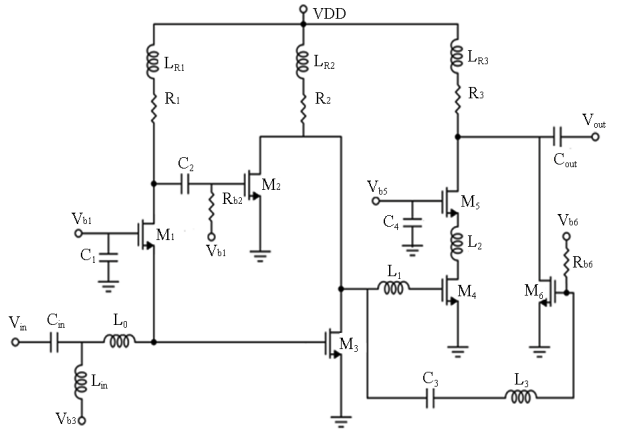

Figure 1. Proposed broadband noise-canceling LNA.

It consists of an input stage and a cascode second stage. An off-chip bias-T provides the gate bias of M_3 and the DC current path of M_1. The series inductors L_1 and L_3 further resonate with the input gate-source capacitance of M_4 and M_6 respectively, resulting in a larger bandwidth and some residual peaking on the frequency response [10]. The parasitic capacitances of M_1 and M_3 make an LC ladder structure with inductor L_0. The DC load resistors R_1 and R_2 are combined with shunt peaking inductors L_{R1} and L_{R2} respectively to extend circuit bandwidth effectively [11]. The series peaking inductor L_{R2} also resonate with the total parasitic capacitances C_{d2} and C_{d3} at the drain of M_2 and M_3. Since the load resistor, R_3, is added to reduce the Q factor of L_{R3} for flat gain and can be directly substitute for a switching quad to form a single-balanced mixer then the output 50 ohm matching is not demanded in an integrated receiver. The minimum channel length of 0.18 μm is considered for all the transistors in the proposed circuit to minimize parasitic capacitances and improve frequency performance. The Cascode stage extends bandwidth, provides better isolation and increases frequency gain. In fact the input stage and the Cascode stage support low-frequency power gain and high-frequency power gain, respectively. The combination of both frequency responses lead to a broadband power gain.

Table 1 shows the design values of the proposed CMOS LNA.

4. Input Common-Gate Stage and Noise Issues

In **Figure 2** the simulated NF and S11 parameter is compared to the case with M_1 is turned OFF. There is a close tradeoff between NF and S11. When M_1 is turned on, the NF is increased by at least 0.6 dB and S21 parameter is decreased 2 dB with the same power dissipation and a similar bandwidth, but on the contrary an acceptable input matching will be achieved. Although the

Table 1. Design values of the proposed CMOS LNA.

L_{in}	4 nH	**(W/L)3**	124/0.18
L_0	0.6 nH	**(W/L)4**	37.5/0.18
L_{R1}	4.5 nH	**(W/L)5**	55/0.18
L_{R2}	2.5 nH	**(W/L)6**	90/0.18
L_{R3}	1.2 nH	C_{in}, C_3, C_4	2PF
L_1	2.76 nH	C_{out}	7PF
L_2	0.7 nH	C_1, C_2	1PF
L_3	2 nH	R_1	320 Ω
(W/L)1	15/0.18	R_2	135 Ω
(W/L)2	24.3/0.18	R_3	80 Ω

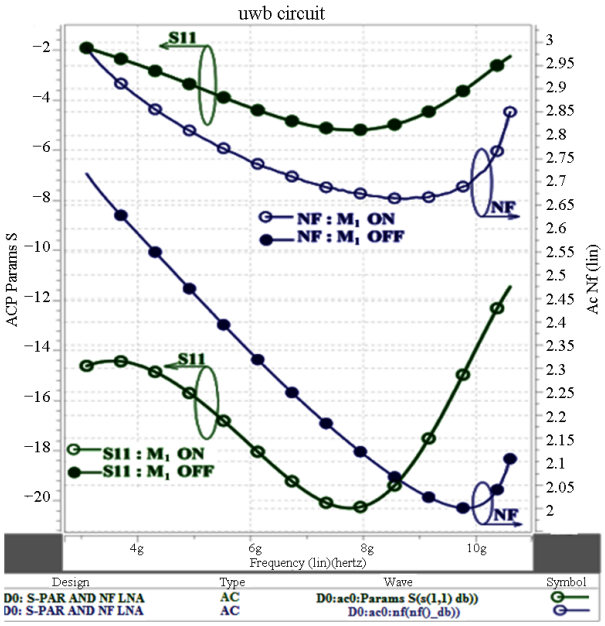

Figure 2. Simulated noise figure and input isolation with M_3 turned ON and OFF.

transistor M_1 provides a wide-Extra band matching, it has an intrinsically high noise figure. In order to investigate the noise performance, the MOS transistor noise model with the channel thermal noise is used. As shown in **Figure 3**, neglecting gate and flicker noises and assuming a perfect match in this analysis, the PSD of the channel thermal noise $i_{n,d}^2$ is given as (1)

$$\overline{i_{n,d}^2} = 4KT\gamma g_{do}\Delta f = 4KT\frac{\gamma}{\alpha}g_m\Delta f \quad (1)$$

where k is the Boltzmann constant, T is the absolute temperature in Kelvin, γ is the MOS transistor's coefficient of channel thermal noise, α is defined as the ratio of the transconductance g_m and the zero-bias drain conductance g_{ds} and Δf is the bandwidth over which the noise figure is measured respectively.

If the condition (2) is established the noise of the M_1 is omitted [1].

$$g_{m_2} R_1 = g_{m_3} R_s \tag{2}$$

The following equations describe the noise figure by R_1, M_2 and M_3 that they contribute to the overall noise figure.

$$F_{R_1} = \frac{4KTR_1 g_{m_2}^2}{KTR_s \left(g_{m_3} + \dfrac{g_{m_2} R_1}{R_s} \right)^2} = \frac{R_s}{R_1} \tag{3}$$

$$F_{M_2} = \frac{4KT\gamma/\alpha g_{m_2}}{KTR_s \left(g_{m_3} + g_{1m_1} \left(Z_{L_{R_1}} \middle\| r_{o1} \right) g_{m_2} \right)^2} = \frac{\gamma}{\alpha} \frac{1}{g_{m_2} R_1} F_{R_1} \tag{4}$$

$$\begin{aligned} F_{M_3} &= \frac{4KT\gamma/\alpha g_{m_3}}{KTR_s \left(g_{m_3} + g_{m_1} \left(Z_{L_{R_1}} \middle\| r_{o1} \right) g_{m_2} \right)^2} \\ &= \frac{4\gamma/\alpha}{g_{m_3} R_s \left(1 + R_s g_{m_1} \right)^2} \end{aligned} \tag{5}$$

Thus, the total noise figure can be approximated as (6)

$$F_{\text{total}} = \frac{R_s}{R_1} \left(1 + \frac{\gamma}{\alpha} \frac{1}{g_{m_2} R_1} \right) + \frac{4\gamma/\alpha}{g_{m_3} R_s \left(1 + R_s g_{m_1} \right)^2} \tag{6}$$

5. Simulation Result

The circuit was simulated with 0.18 μm TSMC library Hspice simulator. All simulations are done considering 50 Ω input and output terminals. In **Figure 4** S parameter are simulated. S11 and S22 are approximately less than −11 dB. The average gain power is approximately 14 dB with 0.8 dB ripple over the frequency range and the reverse isolation is less than −33 dB.

The measured noise figure is 2.66 - 3 dB over 3.1 - 10.6-GHz.

6. Modified Derivative Superposition Method for Linearizing

In this section by using the modified derivative superposition method [9], the linearity of LNA will be improved,

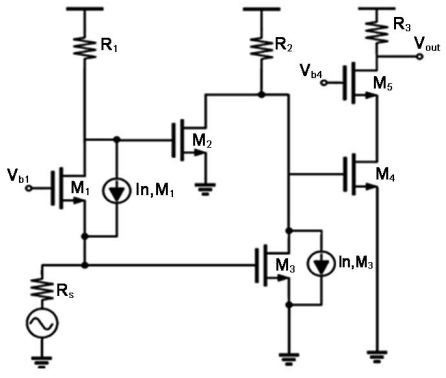

Figure 3. Principle of the noise schematic.

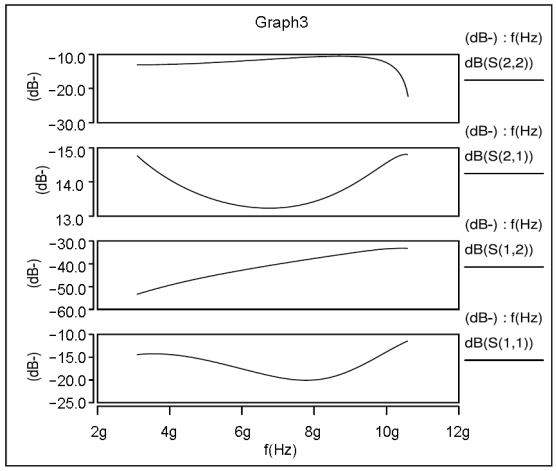

Figure 4. Simulated S parameter.

and IIP3 will be increased over the UWB band. The small-signal output current of a common-source biased in saturation region can be expressed as

$$i_d \left(v_{gs} \right) = g_1 v_{gs} + g_2 v_{gs}^2 + g_3 v_{gs}^3 + \cdots \tag{7}$$

where g_1 is the small-signal transconductance and the higher order coefficients (g_2, g_3, etc.) explain the strengths of the corresponding nonlinearities [9]. Among these coefficients, g_3 is the most important parameter because the third-order inter modulation distortion (IMD3) depends it and thus determines IIP3. The coefficients of (7) can be derived as (8)

$$g_1 = \frac{\partial I_D}{\partial V_{GS}}, g_2 = \frac{1}{2} \frac{\partial^2 I_D}{\partial V_{GS}}, g_3 = \frac{1}{6} \frac{\partial^3 I_D}{\partial V_{GS}} \tag{8}$$

when v_{gs} crosses from the weak and moderate inversion regions to the strong inversion (SI) region, g_3 changes from positive to negative [12]. If a positive g_3 with a specific g_3 (VGS) curvature of one MOSFET is aligned with a negative g_3 with a similar, but mirror-image curvature of another MOSFET by offsetting their gate biases, and the g_3 magnitudes are equalized through a relative MOSFET scaling, the theoretical AIP3 will be efficiently improved in a wide range of the gate biases and the resulting composite g_3 will be close to zero [9].

As shown in **Figure 5** at the optimum gate biases, when two FET are paralleled and one of them operates in the weak inversion (WI) region near the peak in its positive g_3 and another works in the SI region near the dip in its negative g_3, the achieved AIP3 will be improved.

Figure 6 presents the effect of modified derivative superposition method on the similar circuit [9]. By using this method IIP3 increases notably across the UWB band.

Figure 7 shows the effect of using modified DS method on the IIP3 versus frequency respectively. If the M_6 is omitted the IIP3 change as **Figure 7** but other parameters do not change considerably.

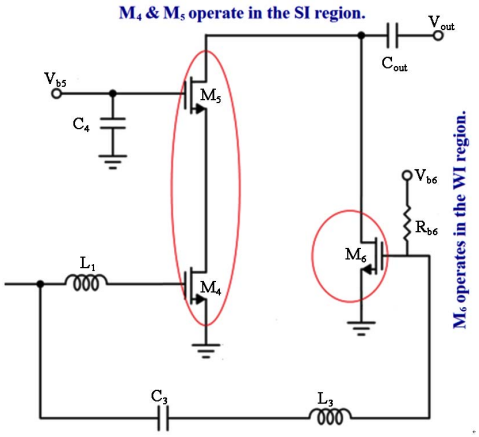

Figure 5. Modified derivative superposition method for linearizing.

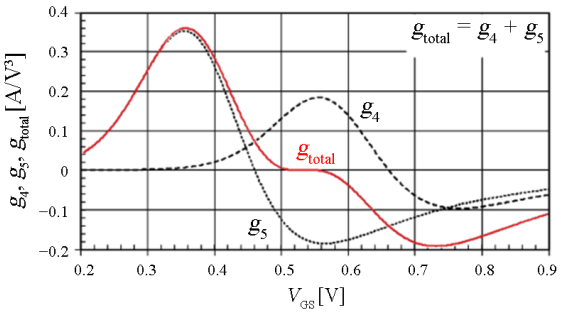

Figure 6. Third-order power series coefficients.

The results of this work are shown in **Table 2** and are compared with recently published CMOS LNAs.

7. Conclusion

This paper presents a new design of an UWB LNA structure based on a standard RFCMOS technology. Satisfactory input matching and noise performance are obtained after regarding the tradeoff between the input impedance of the common-gate stage and its noise performance. The measured noise figure is 2.66 - 3 dB over 3.1 - 10.6-GHz that is noticeable in comparison with the other references. A flat gain is worth mentioning in all LNA design and the simulated power gain is 14 ± 0.8 dB.

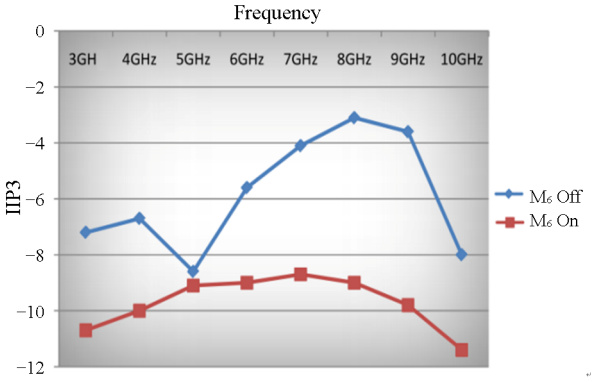

Figure 7. Measured IIP3 versus frequency.

Table 2. Performance summery.

Ref.	CMOS Technology	S11 (dB)	S22 (dB)	S12 (dB)	S21 (dB)	BW3-dB (GHz)	NF (dB)	Power (mw)	IIP3 (dbm)
This work	0.18 µm *CMOS*	<−11.5	<−10.5	<−33	13.2 - 14.8	3.1 - 10.6	<3	23.7	−3.1 - −8.6
[1]	0.18 µm *CMOS*	<−11	<−12	<−32	9.7	1.2 - 11.9	<5.4	20	−6.2
[2]	0.18 µm *CMOS*	<-9.4	<−8	<−40	10.9 - 13.9	3.1 - 10.6	<4.7	14.4	−8.5
[3]	0.18 µm *CMOS*	<−5.7	<−13.7	-	7.6 - 10.8	3.1 - 10.6	3.9 ~ 5.8	6.2	−5
[4]	0.18 µm *CMOS*	<−9	<−13	-	15.9 - 17.5	3.1 - 10.6	3.1 - 5.7	33.2	-
[5]	0.13 µm *CMOS*	<−11	-	-	13.5	2.6 - 10.7	2.7 - 4.2	13.5	+5

It consumes 23.7 mW from a 1.8 V supply. By employing the modified derivative superposition method, the third-order intercept point, IIP3, is improved significantly.

8. Acknowledgements

The author would like to thank for support from research and development section of National Iranian Oil Company (NIOC) and Iranian Offshore Oil Company (IOOC).

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