Logic Picture-Based Dynamic Power Estimation for Unit Gate-Delay Model CMOS Circuits

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ABSTRACT

In this research, a fast methodology to calculate the exact value of the average dynamic power consumption for CMOS combinational logic circuits is developed. The delay model used is the unit-delay model where all gates have the same propagation delay. The main advantages of this method over other techniques are its accuracy, as it is deterministic and it requires less computational effort compared to exhaustive simulation approaches. The methodology uses the Logic Pictures concept for obtaining the nodes' toggle rates. The proposed method is applied to well-known circuits and the results are compared to exhaustive simulation and Monte Carlo simulation methods.

Keywords: Dynamic Power Estimation; Logic Pictures; CMOS Digital Logic Circuits; Toggle Rate; Unit-Delay Model

1. Introduction

Power dissipation is an important parameter for digital VLSI circuits as the excessive power consumption may lead to runtime errors or permanent damages due to overheating. Hence, along with low power design techniques at different levels of the design, accurate power estimation tools are highly needed. Currently, there are many methods for estimating the power consumption; they are mainly categorized as non simulative-based [1-5] and simulative-based methods [6-9]. Non simulative-based methods can either be probabilistic or statistical. They rely on probabilistic measures for the inputs and the switching activities to estimate the power. While being efficient for large circuits with acceptable margins of errors, the power produced is not accurate but only an estimate. For simulative-based methods, the circuit is simulated with different inputs to obtain the power consumption. The main problems in simulative-based methods are the large memory requirements, time consumption and how to find the representative input vector set needed to exercise the circuit. Exhaustive simulations (where all pairs of input vectors are applied to the circuit) are very accurate but, obviously, time consuming, espe-

cially for large circuits.

In [10], an accurate method was introduced for calculating the average and the maximum dynamic power at the gate level. The paper developed the concept of Logic Pictures (LPs) in calculating the average power. As the LP is the status of gates outputs, it was found that the number of LPs was much smaller than the number of inputs patterns; hence, LPs were used instead of input patterns to obtain all the possible transitions for circuit nodes then obtaining the power consumption. The main advantage of this method is that it is deterministic and the simulations required are much less time-consuming than exhaustive simulations. The logic picture concept was modified in [11] to calculate the average power consumption for sequential circuits. In [12], the method was generalized and extended to calculate the maximum power consumption for sequential circuits including all types of Flip-Flops and their internal nodes power consumption; it was also shown how the tool could be used for design space exploration to select the appropriate Flip-Flop that consumed less power. While the method in [10-12] is accurate, it assumed that no propagation delay was associated with logic gates, *i.e.*, zero-delay model.

In this research, a method to calculate an accurate toggle rate assuming unit-delay model, is presented using

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the LP concept. The toggle rate can be directly related to the dynamic power consumption. The proposed method is backward-compatible as it can be easily modified to obtain the power consumption for the zero-delay gate model.

The rest of this paper is organized as follows. Section 2 introduces the methodology to calculate the switching activity of the circuit nodes under unit-delay model assumption for all the gates. Section 3 contains the experimental results while Section 4 has the conclusions.

2. Methodology

For CMOS logic circuits, the average dynamic power can be calculated as follows [13]:

$$P_{avg} = \frac{1}{2} V_{dd}^2 f_{clk} \sum_N \alpha_i c_i \qquad (1)$$

where V_{dd} is the supply voltage, f_{clk} is the clock frequency, N is the number of gates outputs (circuit nodes), α_i is the toggle rate of the output of gate i and c_i is the output capacitance of gate i. From this equation, it can be seen that V_{dd} and f_{clk} depend on the fabrication technology while c_i is linearly proportional to the gate fan-out; the only parameter that depends on the circuit operation is α_i. Therefore, the toggle rate of the nodes is a good indicator of power dissipation [14].

Consider the circuit in **Figure 1** and assume that all inputs have equal probabilities to be 0 or 1.

The circuit has 2 gate outputs (nodes): d and e. As shown in the truth table in **Table 1**, column 3 indicates that the circuit has 3 LPs for the output nodes: 00, 01 and 11. Each LP is associated with a Logic Group (LG) composed of the input vectors that leads to this picture. For LP_1, LG_1 contains 3 input vectors that lead to LP_1: 000, 010 and 100. Hence, $\|LG_1\| = 3$. Similarly, $\|LG_2\| = 3$ and $\|LG_3\| = 2$.

Now, if the unit-delay model is assumed, a propagation delay δ is assigned for each gate and **Table 2** can be easily constructed.

Starting from an initial LP at time $t = 0$, if the input vector is from the LG that leads to the same initial LP, then it is not considered as there is no transition and hence no power consumption, while all the input vectors that belong to other LGs must be applied to get different LPs. The status of the nodes temporarily changes into other transient LPs at $t = \delta$ and finally change into a third, and final, LP at $t = 2\delta$ since there are 2 gates in the critical path. The transient LPs and the final LP are merged into one LP in the rightmost column of **Table 2**.
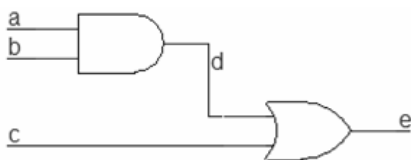
Figure 1. A simple 3-input circuit.

Table 1. Circuit logic pictures with zero-delay model.

Inputs			Outputs		Logic pictures	Logic groups
a	b	c	d	e		
0	0	0	0	0	LP_1 = "00"	LG_1
0	0	1	0	1	LP_2 = "01"	LG_2
0	1	0	0	0	LP_1	LG_1
0	1	1	0	1	LP_2	LG_2
1	0	0	0	0	LP_1	LG_1
1	0	1	0	1	LP_2	LG_2
1	1	0	1	1	LP_3 = "11"	LG_3
1	1	1	1	1	LP_3	LG_3

The number of transitions between the initial LPs and the merged LPs is calculated in **Table 3**. As an example, the transition between $LP_{1,0}$ and LP_1 can be obtained as follows: from **Table 1**, the number of inputs that leads to $LP_{1,0}$ is 3 (remember that $\|LG_1\| = 3$) while from **Table 2**, LP_1 appeared after $LP_{1,0}$ for 3 different inputs; hence, the number of different combinations of inputs that could lead from $LP_{1,0}$ to LP_1 is $3 \times 3 = 9$. LP_2 and LP_3 appeared only once in **Table 2** after $LP_{1,0}$; hence, the number of different input combinations that leads to LP_2 and LP_3 is $1 \times 3 = 3$. Finally, there is no input that leads from $LP_{1,0}$ to LP_4 or LP_5 which means zero direct transition between them.

To obtain the node transitions, if a node in the logic picture toggles from 1 to 0 or 0 to 1, then it is considered as a toggle. Then, this toggle is multiplied by the number of all possible input vectors that lead to this toggle. The same is done for all LPs through time. The possible number for transition for each node is then accumulated and divided by 2^{2n} to obtain the toggle rate. For example, $LP_{3,0}$ is "11"; the logic picture changes to $LP_{1,\delta}$ which is "01". This means that node d toggles from 1 to 0. All possible input transitions from $LP_{3,0}$ to $LP_{1,\delta}$ can be obtained from **Table 3** as $LP_{1,\delta}$ is a part of LP_1 and LP_5, then the input transitions are $6 + 6 = 12$. In addition, there are toggles at node d from $LP_{1,0}$ to $LP_{2,\delta}$, $LP_{1,0}$ to $LP_{3,\delta}$, $LP_{2,0}$ to $LP_{2,\delta}$ and $LP_{2,0}$ to $LP_{3,\delta}$ with 3 possible input transitions for all 4 transitions cases. This leads to 12 other possible transitions. Hence, for node d, the number of transitions is 24. The same can be done with node e resulting into 36 transitions.

To conclude, the following equation can be used to obtain the toggle rate α_i with the unit-delay model:

$$\alpha_i = \frac{\sum_{t=1}^{s} \sum_{l=1}^{k_1(t)} \sum_{m=1}^{k_2(t+\delta)} R_{l,m} tr_t(P_l, P_m)}{2^{2n}} \qquad (2)$$

where s is the number of stages in the critical path, K_1 and K_2 are the LPs in each state where the two states must be consecutive with respect to gates delay, *i.e.*, a

Table 2. All possible logic pictures for the unit-delay model.

Logic Group	Applied Inputs			Initial LP $t = 0$			Transient LP $t = \delta$			Final LP $t = 2\delta$			Merged LP				
	a	b	c	d	e		d	e		d	e						
LG_2	0	0	1	0	0	"$LP_{1,0}$"	0	1	"$LP_{1,\delta}$"	0	1	"$LP_{1,2\delta}$"	0	1	0	1	"LP_1"
LG_2	0	1	1	0	0	"$LP_{1,0}$"	0	1	"$LP_{1,\delta}$"	0	1	"$LP_{1,2\delta}$"	0	1	0	1	"LP_1"
LG_2	1	0	1	0	0	"$LP_{1,0}$"	0	1	"$LP_{1,\delta}$"	0	1	"$LP_{1,2\delta}$"	0	1	0	1	"LP_1"
LG_3	1	1	0	0	0	"$LP_{1,0}$"	1	0	"$LP_{2,\delta}$"	1	1	"$LP_{2,2\delta}$"	1	0	1	1	"LP_2"
LG_3	1	1	1	0	0	'$LP_{1,0}$'	1	1	"$LP_{3,\delta}$"	1	1	"$LP_{2,2\delta}$"	1	1	1	1	"LP_3"
LG_1	0	0	0	0	1	"$LP_{2,0}$"	0	0	"$LP_{4,\delta}$"	0	0	"$LP_{3,2\delta}$"	0	0	0	0	"LP_4"
LG_1	0	1	0	0	1	"$LP_{2,0}$"	0	0	"$LP_{4,\delta}$"	0	0	"$LP_{3,2\delta}$"	0	0	0	0	"LP_4"
LG_1	1	0	0	0	1	"$LP_{2,0}$"	0	0	"$LP_{4,\delta}$"	0	0	"$LP_{3,2\delta}$"	0	0	0	0	"LP_4"
LG_3	1	1	0	0	1	"$LP_{2,0}$"	1	0	"$LP_{2,\delta}$"	1	1	"$LP_{2,2\delta}$"	1	0	1	1	"LP_2"
LG_3	1	1	1	0	1	"$LP_{2,0}$"	1	1	"$LP_{3,\delta}$"	1	1	'$LP_{2,2\delta}$'	1	1	1	1	"LP_3"
LG_1	0	0	0	1	1	"$LP_{3,0}$"	0	1	"$LP_{1,\delta}$"	0	0	"$LP_{3,2\delta}$"	0	1	0	0	"LP_5"
LG_1	0	1	0	1	1	"$LP_{3,0}$"	0	1	"$LP_{1,\delta}$"	0	0	"$LP_{3,2\delta}$"	0	1	0	0	"LP_5"
LG_1	1	0	0	1	1	"$LP_{3,0}$"	0	1	"$LP_{1,\delta}$"	0	0	"$LP_{3,2\delta}$"	0	1	0	0	"LP_5"
LG_2	0	0	1	1	1	"$LP_{3,0}$"	0	1	"$LP_{1,\delta}$"	0	1	"$LP_{1,2\delta}$"	0	1	0	1	"LP_1"
LG_2	0	1	1	1	1	"$LP_{3,0}$"	0	1	"$LP_{1,\delta}$"	0	1	"$LP_{1,2\delta}$"	0	1	0	1	"LP_1"
LG_2	1	0	1	1	1	"$LP_{3,0}$"	0	1	"$LP_{1,\delta}$"	0	1	"$LP_{1,2\delta}$"	0	1	0	1	"LP_1"

state at δ and the other state at 2δ. $R_{l,m}$ are the repetition of the LPs p_l and p_m within a state and $tr(p_l, p_m) = 1$ if there is a node transition between p_l and p_m and equals 0 otherwise.

3. Experimental Results

The circuit used in [10] is shown in **Figure 2**. It was studied with the unit-delay model and it was noticed that the number of nodes transitions increased (compared to the zero-delay model) due to the glitches arising from the gates delays as shown in **Table 4**.

To validate the results of the proposed method, exhaustive and Monte Carlo simulations (as in [8]) are applied to the ISCAS-85 C17 benchmark circuit, the 7483 4-bit binary adder and the 74157 Quad 2-input multiplexer. The characteristics of these circuits are shown in **Table 5**. The resulting power is compared to that obtained using the proposed method. It is found that the difference between the obtained results from the proposed method and the Monte Carlo approach is negligible. Moreover, the results obtained are identical to those obtained using exhaustive simulations.

Since the simulation requires building the truth table

(with size of 2^n), the tool running time is less than the time required for the exhaustive simulation approach. The memory saving ratio can be calculated as the ratio between the memory space required to store the LPs and the memory space needed for the exhaustive simulations [10]. For exhaustive simulations, $\left[2^n * (2^n - 1)\right]/2$ vectors must be stored; each vector represents a circuit input transition and consists of all the possible values for all circuit nodes; hence its size, in bits, is equal to the number of circuit nodes times the number of LPs. In the methodology proposed in this research, only $2^n * (K - 1)$ vectors are required where k is the number of LGs. The size of each vector is identical to that mentioned in the exhaustive simulation method.

Finally the proposed method could be used to obtain the power consumption for the zero-delay model considering only the initial and final states; the power consumption obtained is found to be identical to the one calculated using the technique in [10].

4. Conclusion

This paper discussed a deterministic and accurate method to calculate the node toggle rate, hence dynamic power

**Table 3. All transitions between initial LPs and merged LPs.**

	$LP_{1,0}$	$LP_{2,0}$	$LP_{3,0}$
LP_1	9	0	6
LP_2	3	3	0
LP_3	3	3	0
LP_4	0	9	0
LP_5	0	0	6

Table 4. Node transitions with different delay models.

Node transitions	E	F	G	H
Zero-delay model	96	120	110	126
Unit-delay model	96	144	152	144

Table 5. Test circuit characteristics.

Circuit	Inputs	Nodes	LPs count	Critical path gates	Memory saving
ISCAS85-C17	5	6	10	3	1.7
7483	9	36	162	4	1.6
74157	10	15	34	4	15.5
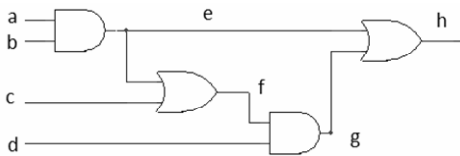
Figure 2. 4-input combinational circuit.

consumption, under the unit-delay model assumption for CMOS combinational circuits. The method is based on the logic picture concept and takes into account intermediate logic pictures that may appear due to gate delays. The proposed method was compared with both Monte Carlo and exhaustive simulations and applied to several circuits: ISCAS85-C17, 7483 4-bit binary adder and 74157 quad 2-input multiplexer. The results are identical but with much lower complexity.

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