

Performance Prospects of Fully-Depleted SOI MOSFET-Based Diodes Applied to Schenkel Circuit for RF-ID Chips

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ABSTRACT

The feasibility of using the SOI-MOSFET as a quasi-diode to replace the Schottky-barrier diode in the Schenkel circuit is examined by device simulations primarily and experiments partly. Practical expressions of boost-up efficiency for *d. c.* condition and *a. c.* condition are proposed and are examined by simulations. It is shown that the SOI-MOSFET-based quasi-diode is a promising device for the Schenkel circuit because high boost-up efficiency can be gained easily. An *a. c.* analysis indicates that the fully-depleted condition should hold to suppress the floating-body effect for GHz-level RF applications of a quasi-diode.

Keywords: RF-ID; Schenkel Circuit; SOI-MOSFET; Quasi-Diode; Low-Power

1. Introduction

Since RF-ID chips have no internal power supply, they need a way of using the received signal as an energy source; a common approach is the Schenkel circuit [1,2]. The basic Schenkel circuit is shown in **Figure 1**. It usually consists of capacitors and pn diodes (PND's) or Schottky-barrier diodes (SBD's). Modern RF applications such as RF-ID chips often use Schottky-barrier diode (SBD) in this circuit [2-4]. Unfortunately, generally speaking, the reverse-biased current (I_R) of an SBD is not significantly lower than the forward-biased current (I_F) because the requirement for high drive currents results in a low barrier height. The reverse-biased current should be extremely low because the *a. c.* signal voltage received is very small in RF-ID systems. Overall, generally speaking, Schenkel circuits that use SBD's fail to offer high boost-up efficiency, resulting in many stages of boost-up circuit block.

Recently, RF-ID chips are applied to various systems without limitation of production costs because applications to social security including living safe attract attention [5]. In these cases, performance and reliability are primarily important. So, a new market of RF-ID chips is growing up.

On the other hand, SOI MOSFET is one of promising devices that can be applied to RF circuit applications [6]

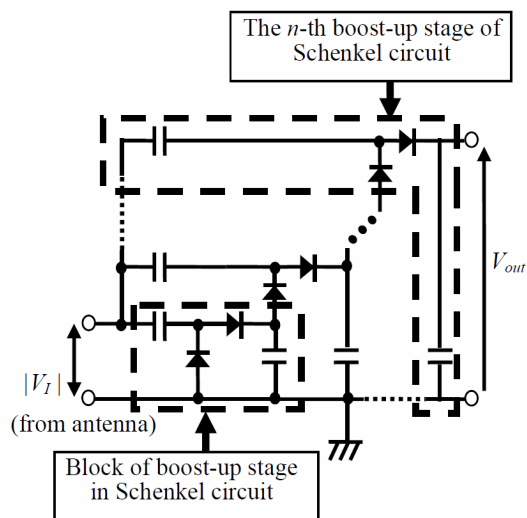


Figure 1. Schematic of Schenkel circuit.

because high-resistivity substrate can be easily introduced [7]. Since the high-resistivity substrate presents not only a low-loss transmission of RF signal [7], but also a low cross-talk in digital circuits [8], various applications are already reported [9,10].

In this paper, we discuss using the SOI-MOSFET-based quasi-diode (SOI-QD) to replace that SBD in Schenkel circuits. First we propose the expression of boost-up

efficiency for a low-frequency range using experimental *d. c.* characteristics of SOI-QD made from various SOI MOSFET's, and *a. c.* analyses of SOI-QD are conducted using a two-dimensional (2D) device simulator (ISE *DESISS* [11]) to investigate operation stability in the RF band. We also define another expression of boost-up efficiency in the RF band, and examined its availability on the basis of *a. c.* simulation results. RF-band potential of SOI-MOSFET-based quasi-diode is addressed from the viewpoint of future RF applications.

2. Remaining Issues of Conventional Schenkel Circuit and an Advanced Proposal

At first, we used the circuit simulator PSPICE [12,13] to examine the performance of a Schenkel circuit that used Schottky barrier diode (SBD), pn-junction diode (PND) or conventional bulk MOSFET-based quasi-diode (CB-QD); in the CB-QD variant, the gate terminal and the drain terminal are connected and the source terminal and the substrate terminal are connected. We assumed that the SBD and PND had a junction area of $46.1 \mu\text{m}^2$, and that the gate width and the gate length of the bulk MOSFET were $20.6 \mu\text{m}$ and $0.32 \mu\text{m}$. All devices had identical active areas; the junction area of bulk MOSFET is $39.5 \mu\text{m}^2$. The circuit simulations employed the empirical model (Level = 3) for simplicity [12]. To acquire realistic device performance from the PND and SBD variants, we introduced the minority carrier lifetime model shown in Appendix A.

Figure 2 shows simulated rectifier characteristics of the various diodes in a low voltage range of input anode voltage (V_A). We can see that SBD with the barrier height (ϕ_b) of 0.15 eV has the largest driving current among the three diodes, but it has the highest reverse-biased current ($4.43 \mu\text{A}$). **Figure 3** shows the performance of 5-stage Schenkel circuits that use the three different diodes for an input voltage $|V_I|$ of 100 mV. It is shown that the conventional bulk-MOSFET-based quasi-diode (CB-QD) successfully boosts the input signal from a very low level to an acceptable level, while SBD and pn-junction diode fail to do so. SBD failed to match this despite its large driving current; since current SBD designs have a high I_R value, almost identical to I_F , in the low voltage range of 100 mV, the high leakage current (I_R) degrades the signal boost process. On the other hand, the I_F and I_R values of CB-QD are much smaller than those of SBD. However, CB-QD offers an acceptable level of boost. The main reason is that I_F of CB-QD is larger than own I_R , which means that the effective boost efficiency (η) of a Schenkel circuit should not be determined by the direct value of driving current, but by the ratio of I_F to I_R defined as

$$\eta = I_F / (I_F + |I_R|). \quad (1)$$

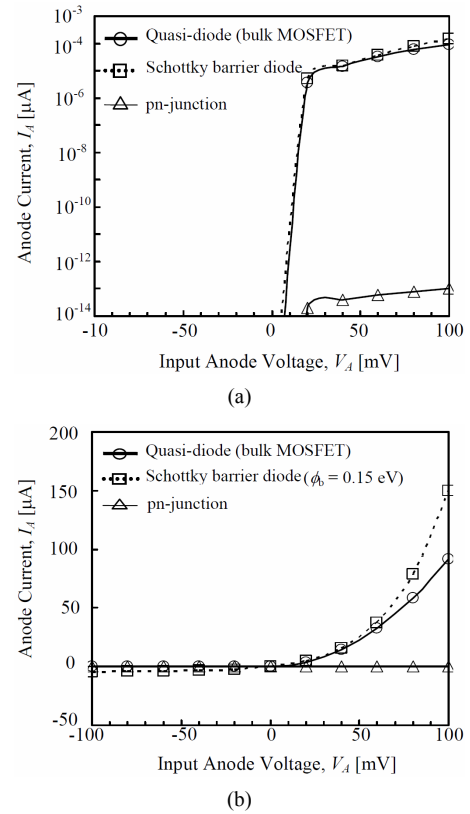


Figure 2. Forward and reverse characteristics of various diodes (Pspice simulation results). (a) Log scale plot; (b) Linear scale plot.

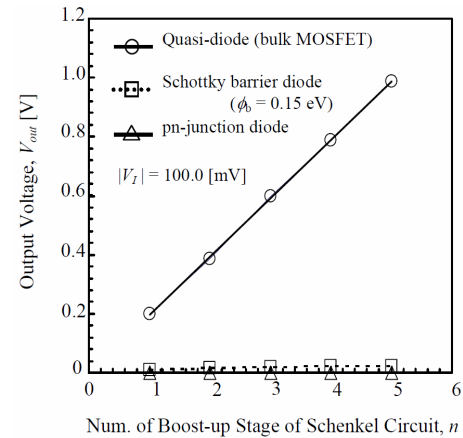


Figure 3. Boost-up performance of Schenkel circuit with various diodes (Pspice simulation results).

In mechanism of voltage boost-up, a large I_R value loses a part of charge stored in a capacitor connected in series. So, the above definition of boost-up efficiency is available independently of the number of boost stages on low-frequency conditions where non-local effects are negligibly small. In addition, the voltage across the capacitor rises when the capacitance of the rectifier is larger than that of the capacitor connected in series; however, this

results in a low-level current source in contrast to the purpose. Therefore, we have to optimize the capacitance of the capacitor so as to fit the performance request.

Unfortunately, we can not apply the above CB-QD to a practical Schenkel circuit as is because it has a crucial drawback; a CB-QD made on an n-channel bulk MOSFET has a parasitic pn-junction diode between the drain and the substrate that can work when the drain is negatively biased. This effective reverse current I_R of CB-QD that passes through the parasitic pn-junction diode degrades the η value.

Our solution is to base the quasi-diode on an SOI MOSFET instead of a bulk MOSFET to raise the η value. **Figure 4** shows the device structure assumed here and the terminal nodes of an SOI-MOSFET-based quasi-diode (SOI-QD). The n-channel fully-depleted (FD)-SOI MOSFET's used here for evaluation of device performance had channel lengths (L) of 0.32 and 1.0 μm (see **Table 1**); these devices are used only for a feasibility test and they are not well tempered for the present purpose. Later we perform *a. c.* simulations for SOI-QD. In this case, it is anticipated that the gate-to-source capacitance and the gate-to-drain capacitance play important roles in the *a. c.* analyses because they yield various parasitic

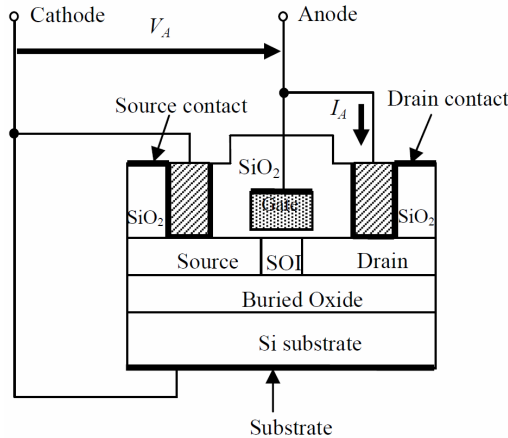


Figure 4. SOI-MOSFET and terminal nodes for quasi-diode operation. Device structure is also assumed for *a. c.* analyses. Device parameters are carefully designed to take account of practical evaluate gate overlap capacitance, S/D parasitic resistance, fringing capacitance, and other parasitic effects in the device.

Table 1. Device parameters used in experiments.

Parameters	Values [Units]
L	0.32 (or 1.0) [μm]
W	20.6 [μm]
t_{SOI}	50.0 [nm]
t_{BOX}	80.0 [nm]
t_{OX}	7.0 [nm]
$N_{a, \text{ch}}$	3.0×10^{17} [cm^{-3}]

capacitances including fringing capacitances [14]. So, we consider a realistic device structure to get reliable *a. c.* simulation results. All physical parameters to draw the cross-section of device are determined on the basis of 0.4- μm CMOS design rule [15]; they are identical to those of the device used in the present experiments. In simulations described later, the doping level of the SOI layer, $N_{a, \text{ch}}$, was changed from $6.0 \times 10^{16} \text{ cm}^{-3}$ to $3.0 \times 10^{17} \text{ cm}^{-3}$ to adjust the threshold voltage.

Figure 5 shows the I_D - V_G characteristics of the FD-SOI MOSFET's ($L = 0.32$ and 1.0 μm) measured at $V_D = 50$ mV; the substrate bias was 0 V. The subthreshold swing (S) values of the two devices are quite different. It can be seen that, because of short channel effects, the S value is larger at $L = 0.32$ μm than at $L = 1.0$ μm .

Since it is anticipated that the device characteristics are sensitive to substrate bias (V_{SUB}) because of the thin buried oxide layer, we can produce SOI-QD's with various rectification characteristics by modifying the substrate bias (V_{SUB}) applied to the FD-SOI MOSFET. It should be noted that this technique is introduced to examine how the threshold voltage of FD-SOI MOSFET modulates the η value through the change of I_F and I_R . By the substrate bias, we can easily vary the S value and the current level as well as the threshold voltage. As a result, we can find the best solution of the SOI-QD's rectification characteristics to be tuned. In practical applications, we cannot assume the substrate bias to the device because the assumed RF-ID chip has not a voltage supplier; at the stage of device design, the threshold voltage must be tuned by positive voltage parameter if possible. In this paper, as an attempt, we apply a negative, zero or a positive V_{SUB} value to the device; these conditions are labeled by "A", "B" or "C" (see **Table 2**), respectively. It should be noted that V_{SUB} value at different L value is not identical when the threshold voltage (V_{TH}) is adjusted to be the same. **Figure 6** shows the I_A - V_A characteristics of SOI-QD "A", "B" and "C".

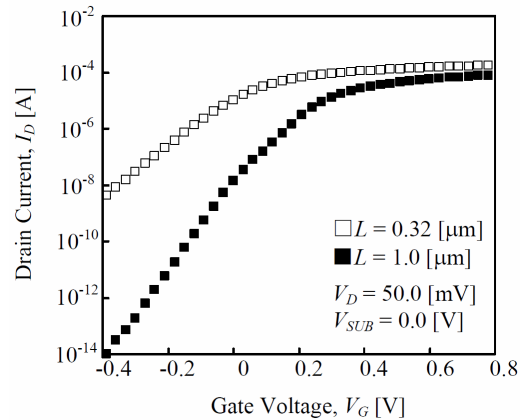
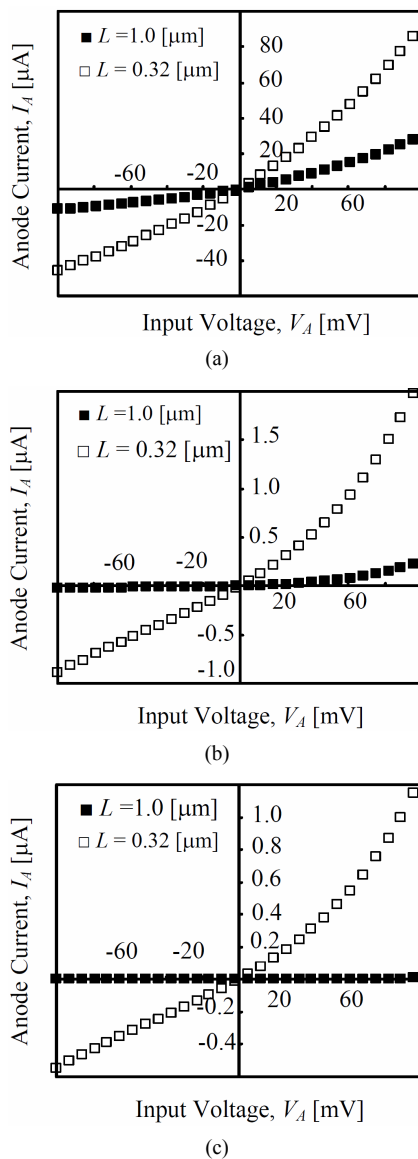


Figure 5. I_D - V_G characteristics of fully-depleted SOI MOSFET (experimental results).

Table 2. I_F , I_R , R_{ch} , and η values of SOI-QD at various operation conditions (*Amplitude of input signal is 100 mV).

	$L = 0.32$ [μm]	S [mV/dec.]/ V_{th} [V]	Forward bias		Reverse bias		η [%]*
			I_F [μA]	R_{ch} [$\text{k}\Omega$]	I_R [μA]	R_{ch} [$\text{k}\Omega$]	
A	$V_{BS} = 0.25$ [V]	211/0.01	90.0	1.1	-47.0	2.2	64.4
B	$V_{BS} = 0.0$ [V]	142/0.1	2.1	47.0	-0.89	110	70.7
C	$V_{BS} = -1.5$ [V]	132/0.27	1.2	81.0	-0.55	180	69.3
	$L = 1.0$ [μm]	S [mV/dec.]/ V_{th} [V]	Forward bias		Reverse bias		η [%]*
			I_F [μA]	R_{ch} [$\text{k}\Omega$]	I_R [μA]	R_{ch} [$\text{M}\Omega$]	
A	$V_{BS} = 3.0$ [V]	169/0.01	29.0	3.4	-11.0	$8.8\text{e-}3$	72.0
B	$V_{BS} = 0.0$ [V]	71.8/0.20	0.25	401.0	-0.016	6.2	94.0
C	$V_{BS} = -3.0$ [V]	71.5/0.92	$7.2\text{e-}3$	$1.39\text{e}4$	$-2.6\text{e-}4$	$3.9\text{e}3$	96.6

**Figure 6.** Rectifier I - V characteristics of SOI-QD (experimental results). (a) Operation condition “A” ($V_{SUB} > 0$); (b) Operation condition “B” ($V_{SUB} = 0$ V); (c) Operation condition “C” ($V_{SUB} < 0$).

At first, we consider the impact of L value as shown in **Figure 6**. In condition “A”, the SOI-QD works near the threshold voltage (V_{TH}) because V_{SUB} is positive. S value is large in condition “A” than in condition “B”, resulting in a smaller ratio of I_F/I_R and thus a smaller η value (see **Table 2**, and **Figures 6(a)** and **(b)**). In condition “A”, however, since the channel resistance (R_{ch}) is reduced due to the lowering of the threshold voltage (V_{TH}), the driving current of the device increases. In contrast, in condition “C”, the device works in the subthreshold region because of the negative substrate bias (V_{SUB}). The S value is smaller in condition “C” than in condition “B”; the channel resistance (R_{ch}) in condition “C” increases due to the raising of the threshold voltage (V_{TH}), resulting in a lower drive current, but identical η value to that seen in condition “B” (see **Figure 6(c)**).

Next we compare the performance of the two devices ($L = 1.0$ and 0.32 μm) shown in **Figure 6**. As mentioned above, the S value with $L = 1.0$ μm is smaller than that with $L = 0.32$ μm . Accordingly, I_F/I_R is larger with $L = 1.0$ μm than that with $L = 0.32$ μm , and the η value with $L = 1.0$ μm is larger than that with $L = 0.32$ μm as shown in **Table 2**. It should be noted that the difference in forward current level (I_F) at the same bias comes from not only the different W/L value but also the different S value. This means that we must take account of the trade-off between η and I_F ; that is, it is necessary to select the most suitable operation bias condition and to reduce the S value. **Table 2** suggests that the S value should be less than 75 mV/dec to reduce I_R value and threshold voltage should be ranging from 0.1 V to 0.2 V to simultaneously gain a high η value.

Finally, we briefly compare the performance of SBD, pn-junction diode and SOI-QD; **Table 2** shows I_F , I_R and η of SOI-QD at various operation conditions when the input signal amplitude ($|V_A|$) is 100 mV. According to a recent report [3], when $V_A = 100$ mV, the SBD has an I_F value of about 1.0 nA and the pn-junction diode has an I_F value of about 0.1 pA; this indicates that the SOI-QD has identical I_F to the other devices or has larger I_F at all

conditions for the two L values examined. In addition, since the SOI MOSFET has lower leakage current than the SBD and subthreshold characteristic of well-tempered SOI MOSFET is excellent, a high boost efficiency can be expected when the SOI-QD is used.

3. Simulation-Based Consideration of RF Performance of SOI-QD

In order to investigate of the feasibility of using SOI-QD's in RF applications [16], we conducted extensive *a. c.* analyses using a 2D device simulator [11]. **Figure 7** shows the simulated rectifier characteristics of the SOI-QD for various $N_{a, ch}$ values. Since the threshold voltage (V_{th}) rises sharply with the increase in doping level of the SOI layer ($N_{a, ch}$), the forward-biased anode current (I_F) decreases greatly and the reverse-biased anode current (I_R) also decreases. However, η increases on the basis of Equation (1) as $N_{a, ch}$ increases because the reduction of I_R overwhelms that of I_F , which is as is expected. A simple estimation method of η value of SOI MOSFET is shown in Appendix B.

When a high-frequency operation is considered, *a. c.* response to applied signal amplitude should be evaluated; this is very important in SOI MOSFET because it is anticipated that the floating-body effect delays the current response to the applied signal [17]. We think that anode conductance $g_A (=dI_A/dV_A)$ successfully traces response capability of SOI MOSFET because g_A is extracted from a small signal analysis; we think a large signal analysis is not always required because Fourier transformation results of signals are effectively considered. Then we define the boost-up efficiency to *a. c.* signals as

$$\eta = \frac{\{\Delta I_{AF}(f)/\Delta V_A(f)\}}{\{\Delta I_{AF}(f)/\Delta V_A(f) + \Delta I_{AR}(f)/\Delta V_A(f)\}}, \quad (2)$$

$$= g_{AF}(f)/\{g_{AF}(f) + |g_{AR}(f)|\}$$

where g_{AF} and g_{AR} mean the anode conductance at the forward and the backward bias conditions, respectively;

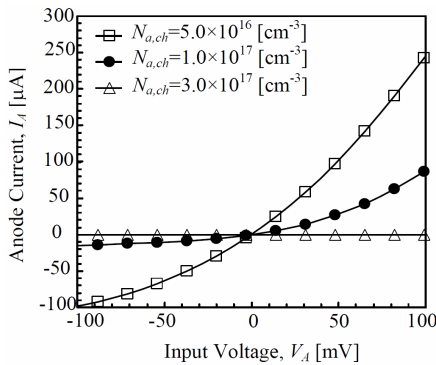
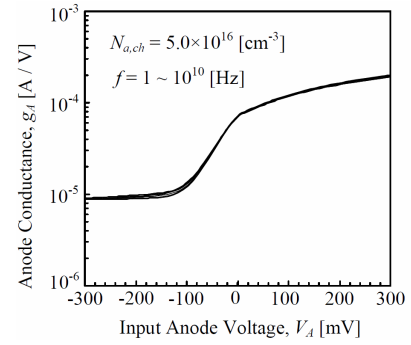
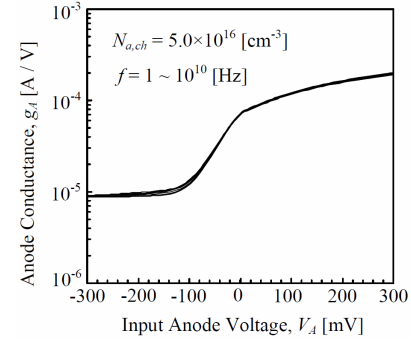


Figure 7. Simulated I - V characteristics of quasi-diodes (device simulations).

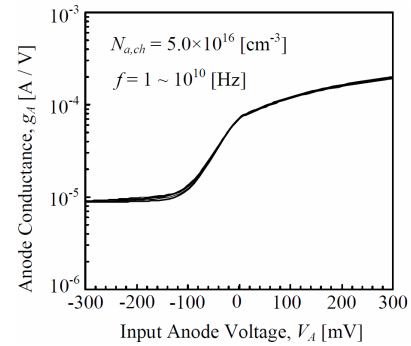
I_{AF} and I_{AR} are the anode current at the forward and the backward bias conditions, respectively. Some **Figure 8** shows the simulated g_A - V_A curves for various $N_{a, ch}$ values, where $g_A (=dI_A/dV_A)$. **Figure 8(a)** is for $N_{a, ch} = 5.0 \times 10^{16} \text{ cm}^{-3}$, **Figure 8(b)** for $N_{a, ch} = 1.0 \times 10^{17} \text{ cm}^{-3}$, and **Figure 8(c)** for $N_{a, ch} = 3.0 \times 10^{17} \text{ cm}^{-3}$. Frequency f was changed from 1 Hz to 10 GHz. In the case of $N_{a, ch} = 5.0 \times 10^{16} \text{ cm}^{-3}$ (see **Figure 8(a)**), the g_A - V_A characteristic is not sensitive to frequency (1 Hz to 10 GHz). In the cases of $N_{a, ch} = 1.0 \times 10^{17} \text{ cm}^{-3}$ (see **Figure 8(b)**) and $3.0 \times 10^{17} \text{ cm}^{-3}$ (see **Figure 8(c)**), however, the g_A - V_A characteristic is sensitive to frequency. In particular, for $N_{a, ch} = 3.0 \times 10^{17} \text{ cm}^{-3}$, the g_A - V_A characteristic reacts strongly to frequency.



(a)



(b)



(c)

Figure 8. Simulated g_A - V_A characteristics (device simulations). (a) $N_{a, ch} = 5.0 \times 10^{16} \text{ cm}^{-3}$; (b) $N_{a, ch} = 1.0 \times 10^{17} \text{ cm}^{-3}$; (c) $N_{a, ch} = 3.0 \times 10^{17} \text{ cm}^{-3}$.

Since the SOI layer is 50 nm thick, the fully-depleted condition is satisfied in two cases (**Figures 8(a)** and **(b)**) [18]. Majority carriers (holes) are basically not responsible for device operation, and so the parasitic bipolar action is not expected at the bias condition used ($|V_A| < 0.3$ V). Since the threshold voltage is very low (~ 0 V), electrons in the inversion layer rule device operation; in this case, the frequency dependence of the dielectric response of electrons (“majority carriers” near the surface) limits the g_A - V_A characteristic. The limit of the frequency response of electrons in Si is higher than 100 GHz [16], so the simulation results shown in **Figures 8(a)** and **(b)** are acceptable. The smaller variation in g_A - V_A characteristics seen in **Figure 8(b)** is related to the remaining hole density near the bottom of SOI layer, which should be higher than that in **Figure 8(a)**.

We note that the fully-depleted condition is not satisfied in the case of $N_{a,ch} = 3.0 \times 10^{17} \text{ cm}^{-3}$ [18]. That is, the majority carriers (holes), remaining near the SOI/buried oxide interface, play an important role in determining device operation, which corresponds to the typical floating body effect [17]. Since the g_A - V_A characteristics at frequencies above 10 MHz differ from those below 10 MHz as seen in **Figure 8(c)**; in other words, the g_A - V_A characteristics at frequencies above 10 MHz are not normal. In the present case, it is easily anticipated that the generation process of majority carriers (holes) (around the junction and inside the depleted body) rules the dynamic operation of SOI-QD. Since the generation-recombination time constant is about 0.1 μsec in the present simulations (see Appendix A), the hole generation process does not respond at frequencies above 10 MHz, resulting in the body floating effect [17].

Figure 9 shows the simulated η - f characteristics of the SOI-QD from $f = 1$ Hz to 1 THz with the parameter of $N_{a,ch}$, although the simulated value of η is not reliable for $f > 100$ GHz because physical models for devices in the device simulator [11] are not proposed for such a high frequency; we simply focus on the behavior of η . η values shown in **Figure 9** are calculated by Equation (2).

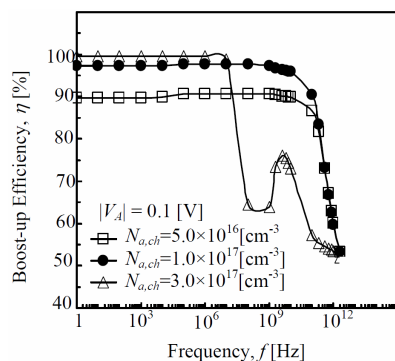


Figure 9. η - f characteristics for various body doping levels (device simulations).

In **Figure 9**, it should be noted that η values calculated by g_A (Equation (2)) at low frequency region are almost identical to η values calculated from d . c . current (experimental results) for $L = 1.0 \mu\text{m}$ by Equation (1). So this suggests that η value can be estimated using Equation (2) at RF region. In **Figure 9**, we can see that the η value remains higher than 90% independently of $N_{a,ch}$ up to 10 MHz; this is supported by the fact that S value in the active range of I_A of SOI-QD is sufficiently small. However, when f is higher than 100 MHz, especially when $N_{a,ch} = 3.0 \times 10^{17} \text{ cm}^{-3}$, η falls to 60%. This comes from the body-floating effect as mentioned previously. On the other hand, at $N_{a,ch} = 5.0 \times 10^{16} \text{ cm}^{-3}$ and $1.0 \times 10^{17} \text{ cm}^{-3}$, η remains high up to 10 GHz. As a result, SOI-QD's with $N_{a,ch} = 5.0 \times 10^{16} \text{ cm}^{-3}$ and $1.0 \times 10^{17} \text{ cm}^{-3}$ can be used in RF applications; when $N_{a,ch} = 3.0 \times 10^{17} \text{ cm}^{-3}$, the SOI-QD is no longer suitable because of the significant body floating effect.

Figure 10 shows the simulated η - $N_{a,ch}$ characteristics of the SOI-QD at 1 MHz and 4 GHz. In the low frequency range (~ 1 MHz) η slightly increases with $N_{a,ch}$ because of the reduction of S at the driving point, and finally reaches its upper limit when the reduction in S value ceases. Since $N_{a,ch}$ increases, driving current (I_A) decreases because the threshold voltage of FD-SOI MOSFET rises. Thus, the doping level of the SOI layer of SOI-QD must be optimized to realize a high performance Schenkel circuit. In the radio frequency range (~ 4 GHz), η peaks because of the floating body effect mentioned above. This strongly suggests that the value of $N_{a,ch}$ must be selected so as to hold the SOI layer in the fully-depleted condition of the SOI layer. As for the present simulation, $N_{a,ch} = 1.0 \times 10^{17} \text{ cm}^{-3}$ yields the best SOI-QD performance in RF applications up to 100 GHz; when SOI layer is thinned to a range of sub-50 nm, $N_{a,ch}$ value higher than $1 \times 10^{17} \text{ cm}^{-3}$ can be applied to devices [19].

In the above simulations, we assumed $V_A = 0.1$ V because we considered the case of short-distance communications. Since the above simulations show that the pro-

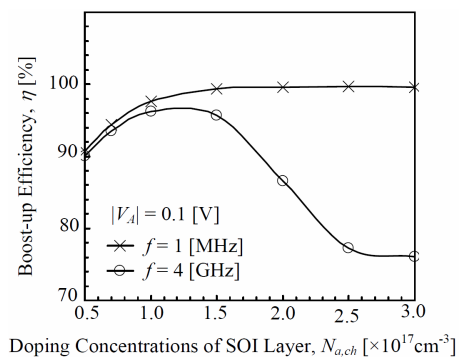


Figure 10. η - $N_{a,ch}$ characteristics for various frequencies (device simulations).

posed SOI-QD produces almost identical performance at $V_A < 0.1$ V, we think that Schenkel circuits with SOI-QD's are also applicable to long-distance communications.

4. Conclusion

The feasibility replacing SBD's in the Schenkel circuit with SOI-MOSFET's as quasi-diodes was examined by experiments and simulations. The reverse-biased current (I_R) of the SOI-QD is much lower than its forward-biased current (I_F) and the driving current (I_F) is high because of the excellent S value provided by the SOI-MOSFET arrangement; we noted that the trade-off between boost efficiency (η) and I_F should be taken into account. In addition, *a. c.* analyses using a two-dimensional device simulator showed that the body doping concentration ($N_{a,cb}$) of the SOI layer should be optimized so as to hold the fully-depleted condition for RF applications up to 100 GHz.

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Appendix A: Simulation Model for Minority Carrier Lifetime

Here we introduce the model for minority carrier lifetimes [11] used in *PSpice* simulations to ensure consistency with *DESSIS* simulation results.

$$\tau = \tau_{\max} + \frac{\tau_{\max} - \tau_{\min}}{1 + \left(N/N_{\text{ref}}\right)^\gamma}, \quad (\text{A1})$$

where N is the doping density, N_{ref} is the doping parameter, γ is the fitting parameter, τ_{\max} and τ_{\min} are lifetime parameters. Parameter values used here are summarized in **Table 3**.

Appendix B: On the Design Guideline of SOI-QD's

We rewrite the expression of boost-up efficiency given by Equation (1).

$$\eta = I_F / (I_F + |I_R|), \quad (\text{B1})$$

When no short-channel effect is assumed, I_F and I_R can be expressed approximately as

$$I_F = \left(\frac{W}{2(1+\alpha)L} \right) \mu_n C_{\text{ox}} (V_A - V_{\text{TH}})^2 + I_{\text{TH}} \quad (V_A > V_{\text{TH}}), (\text{B2})$$

$$I_R = I_{\text{TH}} 10^{\frac{V_A - V_{\text{TH}}}{S}} \quad (V_A < V_{\text{TH}}), \quad (\text{B3})$$

where most of notations are conventional, and S stands for the subthreshold swing for the fully-depleted SOI MOSFET [17]. Parameters α and I_{TH} (threshold current) are given by

$$\alpha = \frac{C_{\text{SOI}} C_{\text{BOX}}}{C_{\text{ox}} (C_{\text{SOI}} + C_{\text{BOX}})}, \quad (\text{B4})$$

$$I_{\text{TH}} = \mu_n \left(\frac{W}{L} \right) q N_A \left(\frac{kT}{q} \right)^2 \frac{1}{E_s}, \quad (\text{B5})$$

where C_{SOI} is the SOI layer capacitance [17], C_{BOX} is the buried oxide layer capacitance [17], and E_s is the surface electric field. The derivation of α is given in [17], and that of I_{TH} is given in [20,21].

Table 3. Physical parameters assumed in device simulations (DESSIS).

Parameters	Values [units]	Comments
τ_{\max}	1.0×10^{-5} [s]/ 3.0×10^{-5} [s]	Electrons/Holes
τ_{\min}	0.0 [s]/0.0 [s]	Electrons/Holes
N_{ref}	1.0×10^{16} [cm ⁻³]	-
γ	1.0	-