

Leakage Reduction Using DTSCCL and Current Mirror SCL Logic Structures for LP-LV Circuits

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ABSTRACT

This paper presents a novel approach to design robust Source Coupled Logic (SCL) for implementing ultra low power circuits. In this paper, we propose two different source coupled logic structures and analyze the performance of these structures with STSCL (Sub-threshold SCL). The first design under consideration is DTPMOS as load device which analyses the performance of Dynamic Threshold SCL (DTSCCL) Logic with previous source coupled logic for ultra low power operation. DTSCCL circuits exhibit a better power-delay Performance compared with the STSCL Logic. It can be seen that the proposed circuit provides 56% reduction in power delay product. The second design under consideration uses basic current mirror active load device to provide required voltage swing. Current mirror source coupled logic (CMSCL) can be used for high speed operation. The advantage of this design is that it provides 54% reduction in power delay product over conventional STSCL. The main drawback of this design is that it provides a higher power dissipation compared to other source coupled logic structures. The proposed circuit provides lower sensitivity to temperature and power supply variation, with a superior control over power dissipation. Measurements of test structures simulated in 0.18 μm CMOS technology shows that the proposed DTSCCL logic concept can be utilized successfully for bias currents as low as 1 pA. Measurements show that existing standard cell libraries offer a good solution for ultra low power SCL circuits. Cadence Virtuoso schematic editor and Spectre Simulation tools have been used.

Keywords: CMOS Integrated Circuits; CMOS Logic Circuit; Dynamic Threshold MOS (DTMOS); Power-Delay Product; Source-Coupled Logic (SCL); Sub-Threshold CMOS; Sub-Threshold SCL; Ultra-Low-Power Circuits; Weak Inversion LP-LV(Low Power-Low Voltage)

1. Introduction

The ever increasing attention on power consumption in circuit design has motivated a significant investigation of optimum design for minimizing energy or power for a given performance constraint. Technology scaling results in a significant increase in leakage current of CMOS device. Various methods and techniques, such as voltage scaling, clock gating, etc. [1-3] have been applied successfully in the medium power, medium performance region of the design spectrum for lower power consumption. Nevertheless, in some applications where ultra-low power consumption is the primary requirement and performance is of secondary importance, a more aggressive approach is warranted. Special circuit techniques have been implemented to enable operation at very low current levels and to achieve the desired performance specifications. The demand for implementing ultra-low-power digital systems in many modern applications such as mobile systems [4], sensor networks [5,6], and implanted

biomedical systems [7], has increased the importance of designing logic circuits in sub-threshold regime [8].

The power dissipation is a crucial parameter in ultra-low power application. The supply voltage V_{DD} is generally reduced below the threshold voltage V_T of metal-oxide-semiconductor (MOS) devices [9]. Reducing the supply voltage or choosing high-threshold-voltage (HVT) devices results in a smaller $V_{eff} = V_{DD} - V_T$ value and, hence, less power consumption [10]. However, reducing V_{eff} results in reduction in the ratio of the ON-current of a logic gate I_{ON} to its leakage current I_{OFF} . Reduction in $\gamma = I_{ON}/I_{OFF}$ results in degradation of reliability and power efficiency of the circuit, requiring special design techniques to implement robust logic operations [9]. Sub-threshold operation (where $V_{DD} < V_T$) is currently used for some low-power applications such as watches and hearing aids. Emerging ultra-low-power applications such as distributed sensor networks are a natural fit with sub-threshold circuits. Special circuit techniques for improving robustness in deep sub-threshold have been ex-

plored [9]. In mixed mode integrated circuits the crucial parameters that affect the performance of the digital system are supply noise and substrate noise. Source coupled logic (SCL) are widely used to reduce the output voltage swing compared to CMOS logic gates for high frequency application. This paper explores performance comparison of two source coupled logic structures with previously available Sub Threshold Source Coupled Logic (STSCCL) gates for implementing ultra-low-power digital systems. In this approach, the power consumption and maximum speed of operation can be adjusted linearly through the tail bias current of each gate over a very wide range [11,12], thus, efficiently decoupling the decision of output voltage swing from power dissipation and delay. To enable the operation at very low tail bias current and to achieve the desired performance, we have to use a special circuit technique for implementing very low power Source Coupled Logic circuit. In first design, the intrinsically limited output impedance of deep-submicron, dynamic threshold PMOS devices have been used to implement very high value load resistances for SCL topology. In second design an active load current mirror has been used to implement very high value of load resistance called Current Mirror Source Coupled Logic (CMSCCL). Here, a more general approach with much less sensitivity to process and technology variations will be introduced [12]. This paper presents two different techniques, one for implementing Dynamic Threshold Source Coupled Logic (DTSCCL) gates where the bias current of each cell can be set as low as 0.1 pA and another for implementing Current Mirror source coupled logic gates where the bias current of each cell can be set as high as 1 mA. In Section 2, after a brief review of SCL circuits, the proposed techniques for implementing different SCL gates will be introduced. Section 3 discusses about the load device concept applied to SCL circuits. Section 4 discusses about the experimental results and implementation of the proposed circuits. Section 4.4 discusses the power-delay performance of the proposed circuit configurations and comparison of different SCL logic structures, followed by conclusions in Section 4.5 and finally Acknowledgement in Section 5.

2. Different Source-Coupled Logic Structure

2.1. DTMOS Topology

In DTMOS logic, gates of transistors are tied to their substrates to achieve the same stability with direct substrate biasing without using additional control circuitry as in case of VTCMOS logic (**Figure 1**) [11]. As the substrate voltage in DTMOS logic changes with the gate input voltage, the threshold voltage is dynamically changed. In the off-state, *i.e.*, $V_{in} = 0$ ($V_{in} = V_{DD}$) for NMOS (PMOS), the characteristics of DTMOS transistor is exactly the same as regular MOS transistor. Both have

the same properties, such as the same off-current, sub-threshold slope, and threshold voltage. In the on-state, however, the substrate-source voltage (V_{bs}) for NMOS (PMOS), the characteristics of DTMOS transistor is exactly the same as regular MOS transistor. When the DTMOS is in off state then it offers higher threshold voltage which in turn reduces the leakage current of the MOS device. In the on state, the substrate-source voltage (V_{bs}) increases which in turn reduces threshold voltage of the DTMOS. Reduction in threshold voltage is due to the reduction in body charge which again leads to an advantage of higher carrier mobility because the reduced body charge causes a lower effective normal field. The reduced threshold, lower normal effective electric field, and higher mobility results in higher on current drive in DTMOS than that of a simple MOS transistor.

The sub-threshold slope of DTMOS improves and approaches the ideal 60 mV/decade which makes it more efficient in sub threshold logic circuits to obtain higher gain.

2.2. Current Mirror Topology

A current mirror is a circuit designed to copy a current through one active device by controlling the current in another active device of a circuit, keeping the output current constant regardless of loading. The current being ‘copied’ can be, and sometimes is, a varying signal current. Conceptually, an ideal current mirror is simply an ideal current amplifier. The current mirror is used to provide bias currents and active loads to circuits. High-performance current mirrors with low input and output voltages are required as building blocks of mixed-mode VLSI systems that operate from a single supply of 1.8 V or below. High accuracy requires very high output resistance and low input resistance. Low-voltage operation requires low input and output voltages as well as low supply requirements for the control circuitry used to improve the mirror’s input and output resistance. There are three main specifications that characterize a current mirror. The first is the current level it produces. The second is its AC output resistance, which determines how much the output current varies with the voltage applied to the mirror. The third specification is the minimum voltage drop across the mirror necessary to make it work properly. This minimum voltage is dictated by the need to keep the output transistor of the mirror in active mode.

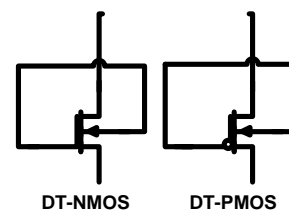


Figure 1. DT-NMOS and DT-PMOS.

The range of voltages where the mirror works is called the compliance range and the voltage marking the boundary between good and bad behavior is called the compliance voltage. There are also a number of secondary performance issues with mirrors, for example, temperature stability.

2.3. Basic SCL Topology

The source coupled logic (SCL) topology has been a modern approach for designing of ultra low power circuits. This topology is very suitable for very low bias current operations as it provides accurate control on power consumption of each gate, whereas the power dissipation of conventional static CMOS circuits is limited by their sub-threshold leakage current. Simultaneously, the gate delay in this configuration does not depend on the supply voltage and hence, there is low sensitivity to supply voltage variations.

Figure 2 shows that the switching part can be composed of a network of NMOS source-coupled pairs to implement more complex logic functions [2]. The load resistances can be implemented using PMOS devices biased in triode region.

In an SCL gate, the logic operation takes place mainly in current domain. Therefore, the speed of operation can be inherently high. The voltage swing at the output node ($V_{SW} = I_{SS} \cdot R_L$) should be $V_{SW} > 4n_n \cdot U_T$ (n_n is the sub-threshold slope factor of NMOS differential pair devices, and U_T is the thermal voltage). To achieve the required voltage swing at very low trail bias current the load resistance should be very high, and also occupy a small area with a very good control to adjust their resistivity with respect to their trail bias current. In first design, DT-PMOS transistor can be used to provide high resistance with a relatively high voltage swing at the output, the proposed topology can operate properly as logic device. In the second design, current mirror active load is used as a load device to provide higher resistance with a relatively high voltage swing.

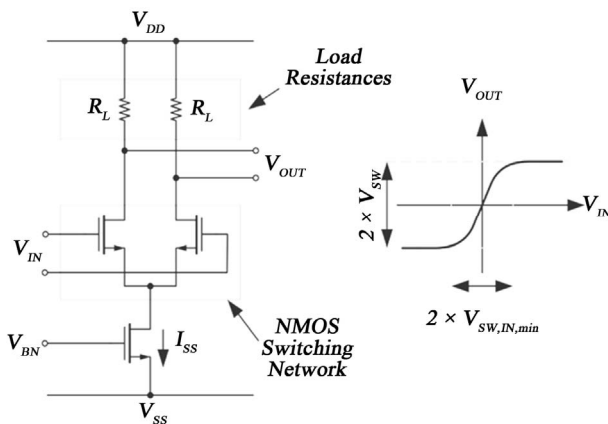


Figure 2. A conventional SCL-based inverter/buffer circuit.

In SCL topology the main leakage currents are due to the p-n junctions of the MOS devices, whereas in CMOS logic circuits the sub-threshold channel leakage current is the dominant leakage component. The speed of operation in an SCL gate is mainly limited by the time constant at the output node which is calculated as Equation (1):

$$T_{SCL} = R_L \times C_L = V_{SW} \times CL / I_{SS} \quad (1)$$

Based on the above, the propagation delay is inversely proportional to the tail bias current. Meanwhile, the circuit power-delay product (PDP) is independent of I_{SS} [12-14].

3. Load Device Concept

To maintain the required voltage swing at very low trail bias current it is necessary to increase the load resistance in inverse proportion to the reducing trail bias current. In sub-threshold region, the trail bias current would be in the order of few pA or even less. Therefore, to obtain a required output voltage swing, the load resistance should be of the order of few G Ω . Meanwhile, this resistance should be controlled very accurately based on the value of trail bias current I_{SS} . Hence, a well controlled high resistivity load device with a very small area is required. For this range of resistivity, conventional PMOS devices biased in triode region cannot be utilized since the required channel length of the transistor would be impractically large. **Figure 3(a)** shows the proposed load device, where the gate of the PMOS device is connected to its bulk where as **Figure 3(b)** is the conventional device. In this way, the load device provides accurate control on the resistance, which, associated with the transconductance of the differential pair will provide a controlled, limited gain and amplitude with relatively small size PMOS load device.

Figure 3(c) shows the I-V characteristics of the conventional PMOS and the proposed PMOS load device.

In the proposed load device the gate and substrate of PMOS load device are shorted. When $V_{SG} = V_{SD}$ then it will behave as conventional PMOS load device as we vary the gate voltage V_{SG} the voltage across the substrate terminal also varies as a result the threshold voltage of the device changes and also the resistance of the PMOS load device varies. In this way the proposed load device will be used as a controlled resistance.

The basic current mirror can also be implemented using MOSFET transistors, as shown in **Figure 4**. Transistor M_1 is operating in the saturation or active mode, and so is M_2 . In this setup, the output current I_{OUT} is directly related to I_{REF} . The drain current of a MOSFET I_D is a function of both the gate-source voltage and the drain-to-gate voltage of the MOSFET given by

$I_D = f(V_{GS}, V_{DG})$, a relationship derived from the functionality of the MOSFET device. In the case of transistor

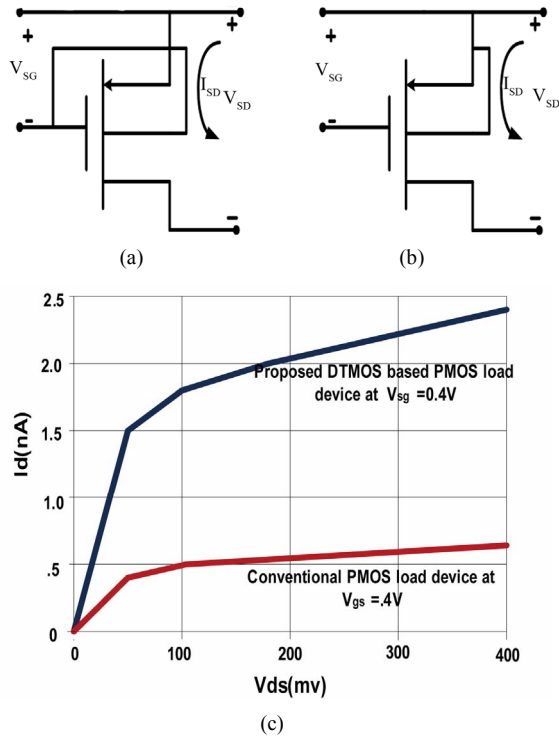


Figure 3. (a) Conventional PMOS load device; (b) DT-PMOS load device; (c) I-V characteristics of the conventional PMOS load in comparison to the proposed DT-PMOS device.

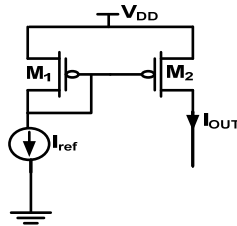


Figure 4. Basic Current Mirror Structure.

M_1 of the mirror, $I_D = I_{REF}$. Reference current I_{REF} is a known current, and can be provided by a resistor as shown, or by a “threshold-referenced” or “self-biased” current source to ensure that it is constant, independent of voltage supply variations.

Using $V_{DG} = 0$ for transistor M_1 , the drain current in M_1 is $I_D = f(V_{GS}, V_{DG} = 0)$, so we find: $f(V_{GS}, 0) = I_{REF}$, implicitly determining the value of V_{GS} . Thus I_{REF} sets the value of V_{GS} . The circuit in the diagram forces the same V_{GS} to apply to transistor M_2 . If M_2 also is biased with zero V_{DG} and provided transistors M_1 and M_2 have good matching of their properties, such as channel length, width, threshold voltage etc., the relationship $I_{OUT} = f(V_{GS}, V_{DG} = 0)$ applies, thus setting $I_{OUT} = I_{REF}$; that is, the output current is the same as the reference current when $V_{DG} = 0$ for the output transistor, and both transistors are matched.

The drain-to-source voltage can be expressed as $V_{DS} = V_{DG} + V_{GS}$. With this substitution, the Shichman-Hodges model Equation (2) provides an approximate form for function $f(V_{GS}, V_{DG})$:

$$I_d = f(V_{GS}, V_{DG}) = \frac{1}{2} K_p \left(\frac{W}{L} \right) (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}) \quad (2)$$

$$= \frac{1}{2} K_p \left(\frac{W}{L} \right) (V_{GS} - V_{th})^2 (1 + \lambda (V_{DG} + V_{GS}))$$

where, K_p is a technology related constant associated with the transistor, W/L is the width to length ratio of the transistor, V_{GS} is the gate-source voltage, V_{th} is the threshold voltage, λ is the channel length modulation constant, and V_{DS} is the drain source voltage. Because of channel-length modulation, the mirror has a finite output (or Norton) resistance given by the r_o Equation (3) of the output transistor, namely

$$R_N = r_o = \frac{(1/\lambda + V_{DS})}{I_D} \quad (3)$$

where λ is the channel-length modulation parameter and V_{DS} is the drain-to-source bias.

4. Proposed Implementation of DTSCl & Current Mirror SCL Gates & Results.

4.1. DTSCl Gates

The proposed DTPMOS load device can be utilized to implement an SCL gate biased in sub-threshold regime. **Figure 5** shows the basic structure of the proposed DTSCl gate. The **Figure 5** includes the replica bias circuit which is used to control the output voltage swing. Replica bias circuit consist of two major component one is op-amp and another is a current mirror circuit which

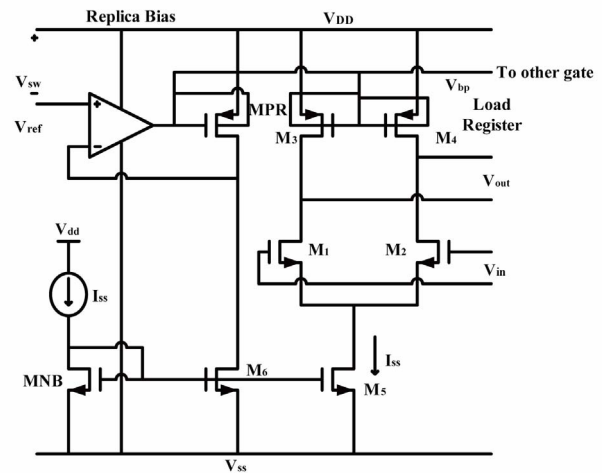


Figure 5. DTSCl gate and the replica bias circuit used to control the output voltage swing.

will maintain a constant tail bias current I_{SS} . This circuit also tracks the variations on temperature and supply voltage and, hence, compensates their effect on the circuit performance.

A simplified circuit diagram of the replica bias circuit used to control the output voltage swing is also shown. In this schematic, all devices operate in sub-threshold regime and the tail bias current can be reduced until it becomes comparable in magnitude to the leakage currents that exist in the circuit. **Figure 6(a)** illustrates the DC transfer characteristics of a DTSCl gate. The stage gain of DTSCl gate is as shown in **Figure 6(b)**. The measured stage gain of DTSCl gate is approximately 42. The measured input-output transfer characteristics of a DTSCl buffer stage at different tail bias current are shown in **Figure 6(c)**. As all the devices are operating in sub-threshold regime hence the transfer characteristic of the circuit is independent of the tail bias current.

In the plot above, the deviation from the ideal DC characteristics is mainly due to the leakage currents in the test circuit coming from electrostatic discharge (ESD) protection circuitry. To measure the DC characteristics, output voltage swing has been adjusted manually.

The variation in power dissipation and gate delay of a DTSCl gate is as shown in **Figures 7(a) and (b)** simultaneously. It is seen that the stabilized output of is achieved at tail bias current $I_{SS} = 1$ pA. At this tail bias current, DTSCl provides lowest power delay product of the order of 569.71×10^{-18} W-Sec.

The **Table 1** above describes the variation in delay with different tail bias current with subsequent power dissipation and the corresponding PDP.

4.2. Current Mirror SCL Gates

The proposed current mirror active load device can be utilized to implement an SCL gate biased in sub-threshold regime. **Figure 8** shows the basic structure of the proposed Current Mirror SCL gate.

In this schematic given below, all devices operate in sub-threshold regime and the tail bias current can be reduced until it becomes comparable in magnitude to the leakage currents that exist in the circuit.

Figure 9(a) illustrates the DC transfer characteristics of a Current Mirror SCL gate. The stage gain of Current Mirror SCL gate is as shown in **Figure 9(b)**. The measured stage gain of Current Mirror SCL gate is approximately 8.2. The measured input-output transfer characteristics of a Current Mirror SCL buffer stage at different tail bias current are shown in **Figure 9(c)**. As all the devices are operating in sub-threshold regime hence the transfer characteristic of the circuit is independent of the tail bias current.

The variation in power dissipation and gate delay of a

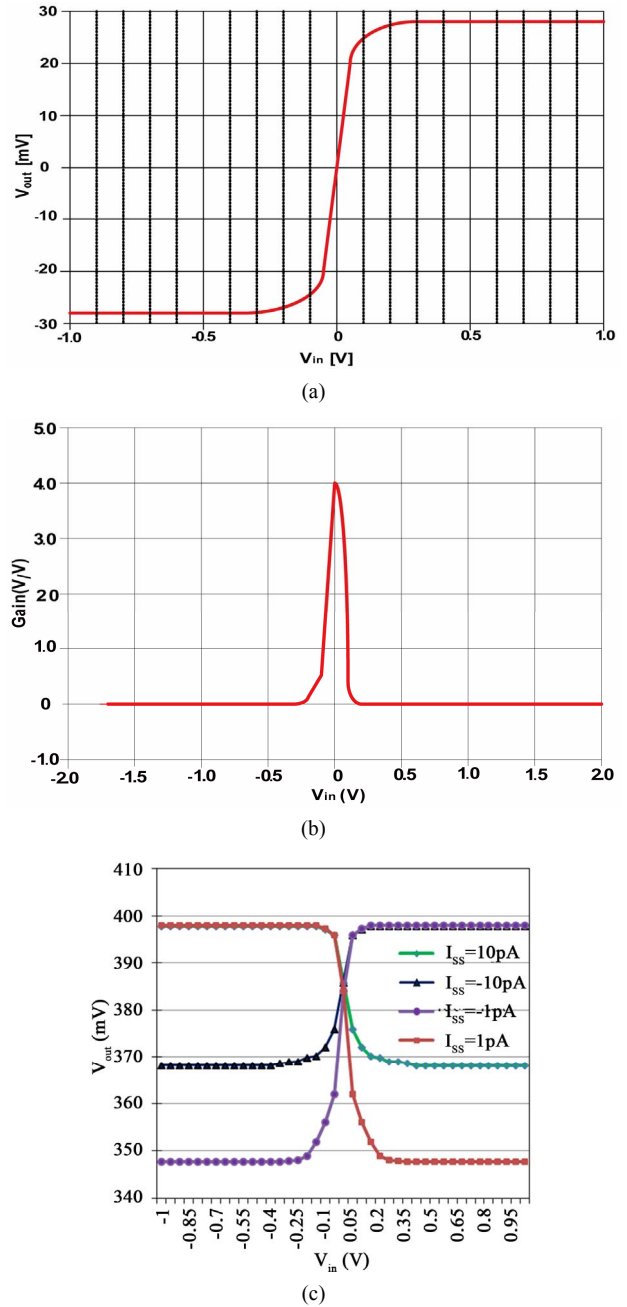


Figure 6. (a) Simulated DC transfer characteristics of a DTSCl gate biased at I_{SS} of 1 Pa; (b) DC gain of a DTSCl gate biased at I_{SS} 1 pA; (c) Measured transfer characteristics of a DTSCl buffer stage for different bias currents ($I_{SS} = 1$ pA, and 10 pA).

Table 1. Variation in delay with tail bias current.

Bias current I_{SS} (pA)	Power Dissipation (nW)	Delay (n sec)	PDP(10^{-18} Wsec)
1	0.1096	5200	569.71
10	1.5232	900	1370.88
100	5.23	56	2928.8

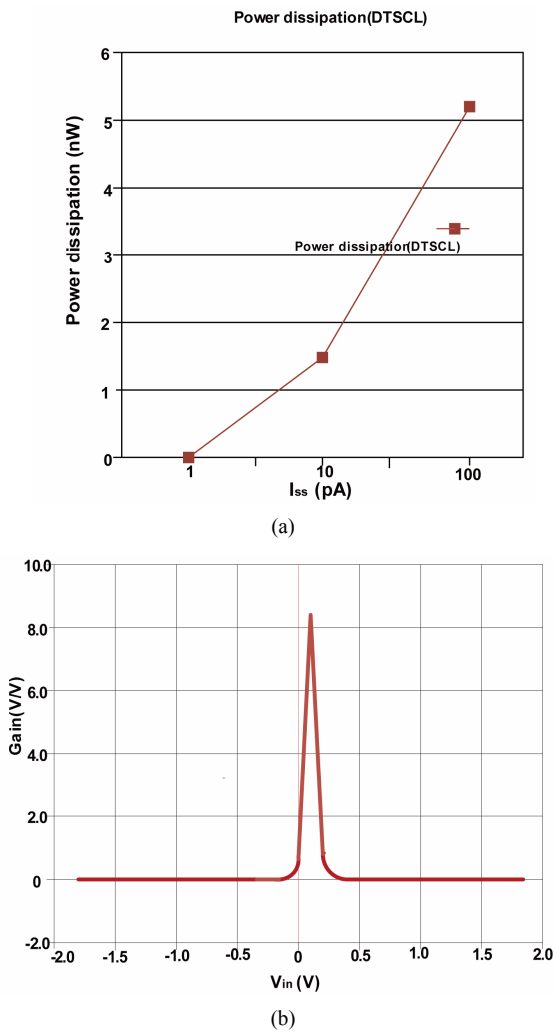


Figure 7. (a) Variation in power dissipation with trail bias current; (b) Variation in delay with trail bias current.

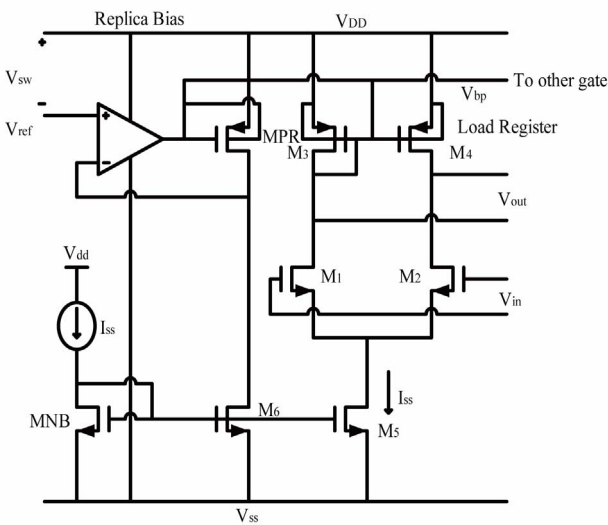
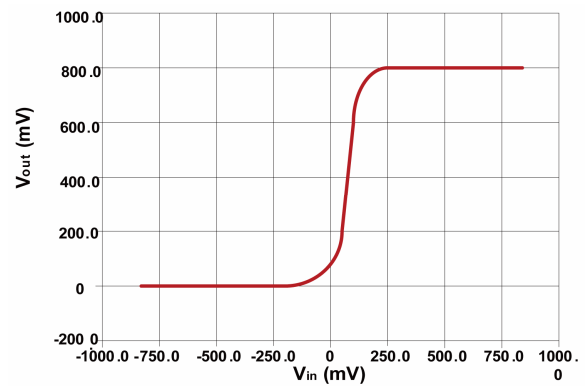
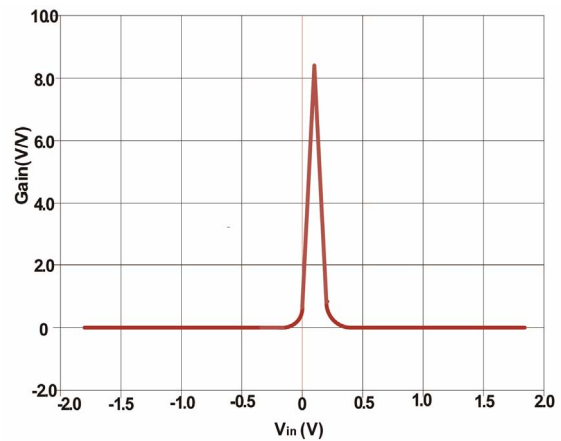


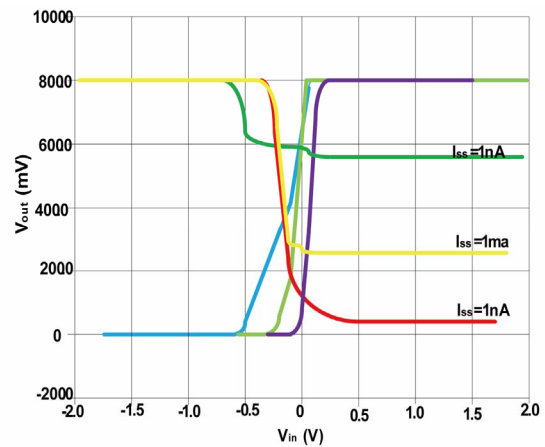
Figure 8. Current Mirror SCL gate and the replica bias circuit used to control the output voltage swing.



(a)



(b)



(c)

Figure 9. (a) Simulated DC transfer characteristics of a Current Mirror SCL gate biased at I_{SS} of 1 mA; (b) DC gain of a Current Mirror SCL gate biased at I_{SS} of 1 mA; (c) Measured transfer characteristics of a Current Mirror SCL buffer stage for different bias currents (I_{SS} = 1 nA, 1 μA and 1 mA).

Current Mirror SCL gate is as shown in Figure 10(a) and (b) simultaneously. It is seen that the stabilized output of is achieved at trail bias current I_{SS} = 1 mA. At this trail bias current, Current Mirror SCL provides lowest power

delay product of the order of 592.238×10^{-18} W-Sec.

The **Table 2** Describes the PDP and power consumption at different trail bias currents.

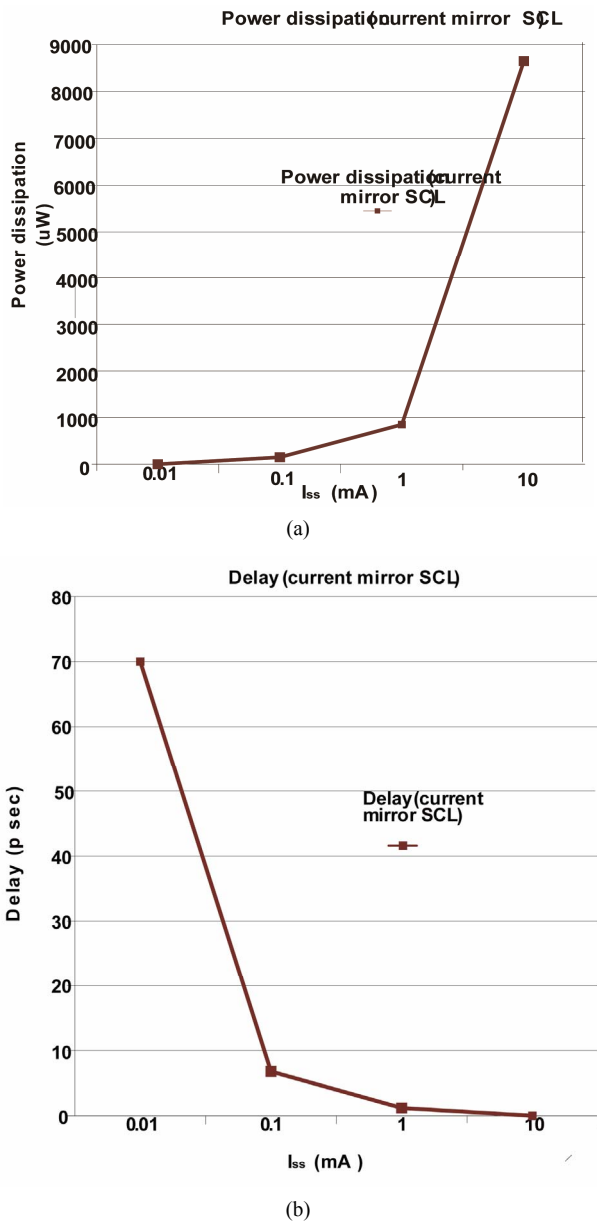


Figure 10. (a) Variation in power dissipation with trail bias current; (b) Variation in delay with trail bias current.

Table 2. Variation in delay with trail bias current.

Bias current I_{SS} (mA)	Power Dissipation (μ W)	Delay (p sec)	PDP(10^{-18} Wsec)
0.01	16.44	70	1150.8
0.1	111.147	7.5	833.60
1.0	832.73	0.716	592.238
10	8426.12	0.0731	615.949

4.3. Voltage Swing Control

To achieve the required voltage swing at the output, a controlling circuit is used. **Figure 11** shows a simplified schematic of replica bias circuit to control the output voltage swing. The Replica bias circuit consists of a high performance current mirror circuit that can maintain a constant current I_{SS} at the output to provide accurate control on the output voltage swing. The replica bias circuit should be well matched to the SCL gates to have very low deviation in operating point. Meanwhile, amplifier should provide enough gain with a very low offset to have the desired accuracy.

In this work, a folded-cascode amplifier has been used to provide a large swing at the output node and to be able to test the SCL gates in a very wide range of bias current values. Any mismatch in the bias current of the devices of the SCL gates and RB circuit will result in variation of the desired output voltage swing.

4.4. Performance Analysis and Observation

4.4.1. Power-Speed Trade-Off in SCL Circuits

In contrast to the CMOS gates, where there is no static power consumption (neglecting the leakage current), each SCL gate draws a constant bias current of I_{SS} from a supply source (**Figure 2**). Therefore, the power consumption of each SCL gate can be calculated by Equation (4) as

$$P_{diss,SCL} = V_{DD} \times I_{SS} \quad (4)$$

Meanwhile, the time constant at the output node of each SCL gate, is given as Equation (5) *i.e.*,

$$\tau = R_L \times C_L \approx (V_{SW}/I_{SS}) \times C_L \quad (5)$$

is the main speed-limiting factor in this topology (C_L is the total output loading capacitance). Based on (5), one

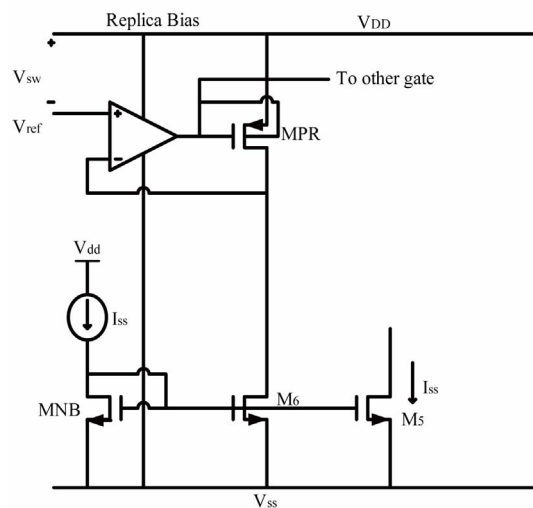


Figure 11. Replica bias circuit to control o/p voltage swing.

can choose the proper I_{SS} value to operate at the desired frequency. This circuit exhibits a very low sensitivity to the process variations because the power consumption and delay of each gate only depend on I_{SS} , which can very precisely be controlled. Meanwhile, it is not necessary to use special process options to have low threshold voltage devices, as frequently used for static CMOS [1,2,8]. Therefore, it is necessary to use the DTSCl circuits at their maximum activity rate to achieve the maximum achievable efficiency. It is also important to note that the gate delay does not depend on the supply voltage, whereas it linearly varies with the tail bias current. This property can be exploited for applications in which the supply can vary during the operation. Based on Equations (4) and (5), the power-delay product (PDP) of each gate can be approximately calculated by Equation 6 given below:

$$PDP_{DTSCl} = \ln 2 \times V_{DD} V_{SW} C_L \quad (6)$$

Observation 1: The delay of a logic block can be controlled without influencing PDP as the delay of DTSCl gate depends on tail bias current (I_{SS}), but not on supply voltage V_{DD} .

Observation 2: To reduce the power to frequency ratio, α should be kept as large as possible. This observation does not contradict with similar results for conventional CMOS.

4.4.2. Tabulated Comparison of Different SCL Circuit

Shown below is the comparison of the power consumption, delay and power delay product of different SCL structures (STSCl, DTSCl, Current Mirror SCL) as shown in **Table 3**. The table shows that if we wish to design a circuit with low power dissipation than proposed DTSCl is preferred over other SCL techniques and if we choose to design a circuit with higher speed than proposed Current Mirror SCL is preferred over other SCL techniques.

4.5. Conclusion

In this paper, an analytical approach for studying and comparing the performance of ultra low power STSCl, DTSCl, and Current Mirror SCL has been presented.

Table 3. Comparison of various SCL circuits.

Logic circuit	Stabilized bias current	Power dissipation	Delay	PDP (10^{-18} Wsec)
STSCl inverter	1 nA	3.136 nW	410 ns	1285.76
DTSCl inverter	10 pA	0.1523 nW	900 ns	569.71
C-M STSCl inverter	1 mA	832.73 μ W	0.7 ps	592.238

While there is a tight tradeoff among the power consumption, speed of operation, and supply voltage in design of CMOS digital circuits, the SCL topology provide a more flexible design option for ultra low power applications. In this work, two new source coupled logic design has been discussed. The first design uses a high resistance DT-PMOS load device to provide the required voltage swing at the output. The measurement result shows that the DTSCl topology provides 56% reduction in PDP compared to STSCl, using 0.18 μ m CMOS technology. The second design uses basic current mirror load device to provide required voltage swing at the output. This design can be used for high speed operation at the cost of higher power dissipation. Hence this design can be used for high speed operation at the cost of power dissipation. The measurement result shows that the Current Mirror SCL provides 54% reduction in PDP compared to STSCl, using 0.18 μ m CMOS technology. The trail bias current of each gate can be reduced to less than 0.1 pA, while the power delay product of the gate remains less than 1 fJ. The bias current of a SCL gate can be scaled over several decades, which makes this topology very suitable for ultra low power applications. The main advantage of this topology is that there is no effect of process and temperature variation and it can operate in a wide range of frequency. The author has used **Cadence Virtuoso** Schematic Editor [15] and **Spectre** as simulation platform. All the results and their verification has been done by using cadence tools.

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