

A New Design Technique of CMOS Current Feed Back Operational Amplifier (CFOA)

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ABSTRACT

A new design technique employing CMOS Current Feedback Operational Amplifier (CFOA) is presented. This design approach applies CFA OTA as input stage cascaded with class AB cross-coupled buffer stage. The performance parameters of CMOS CFOA such as bandwidth, slew rate, settling time are extensively improved compared with conventional CFOA. These parameters are very important in high frequency applications that use CMOS CFOA as an active building block such as A/D converters, and active filters. Also the DC input offset voltage and harmonic distortion (HD) are very low values compared with the conventional CMOS CFOA are obtained. P-Spice simulation results using 0.35 μm MI-ETEC CMOS process parameters shows considerable improvement over existing CMOS CFOA simulated model. Some of the performance parameters for example are DC gain of 67.2 dB, open-loop gain bandwidth product of 104 MHz, slew rate (SR+) of +91.3 V/ μs , THD of -67 dB and DC input offset voltage of -0.2 mV.

Keywords: Synthesis CFA OTA and CMOS CFOA; Cross Coupled Buffer Stage; High Performance CFOA; Low Input Offset Voltage CFOA; Low Distortion CFOA

1. Introduction

The role of analog integrated circuits in modern electronic systems remains important, even though digital circuits dominate the market for VLSI solutions. Analog systems have always played an essential role in interfacing digital electronics to the real world in applications such as analog signal processing and conditioning, industrial process, motion control and biomedical measurements [1]. However, the conventional CMOS CFOA design is still facing certain problems, first, the offset voltage on the current feedback can not be made zero. CFOA usually adopts an analog buffer as the input stage. As a result, the non-inverting input has very high impedance, while the inverting input has very low impedance. Hence, the CFOAs offset is higher than folded cascade voltage amplifier (VFA) Design. Second, the constant bandwidth feature of the CFOA is only approximate if the inverting input impedance is not small enough [2,3]. The low-input offset voltage is considered as an important aspect of the performance of an amplifier especially when signals are in the range of few hundred micro volts [4]. Several CMOS realizations for the CFOA have been reported in the literature [5-12]. The design still suffers from many drawbacks such as high distortion, high noise, high consumption of power and complex circuitry. The CFOA has been always seen as an extension of the CCII, therefore, the design approach

was cascade with CCII+ with a voltage follower to realize a complete circuit. The obtained bandwidth was always the degraded version of CCII+.

The current feedback operational amplifier (CFOA), a two-port (four-terminal) network. The CFOA could be realized by using second generation current conveyor CCII+ cascaded with a voltage follower [13].

This paper describes an alternative approach to CMOS CFOA design which provides symmetrical high impedances (infinite for DC) inputs together with high performance parameters in high frequency operation. This design approach applies CFA OTA as input stage cascaded with class AB cross-coupled buffer as output stage. The symmetrical input stage of CFA OTA will reduce the DC offset voltage of CMOS CFOA with improvement of high frequency parameters. Moreover, class AB cross coupled buffer stage provide high current drive capability. P-Spice simulation results confirm the theoretical calculations.

2. Theoretical Background of CFB OTA

The two output terminals are not seen as one port each, but as four independent terminals that can have different impedance levels. As a consequence, hybrid stages appear, namely a H input stage and a H output stage. The H input stage, which has become well known through the CFB opamp, can also be understood as an extended input

stage whose analogue ground voltage is not fixed, but can be set through an additional terminal. The V output can also be extended to a hybrid stage. It copies the current flowing into the voltage output terminal to an additional current output terminal. This technique, which is called output current sensing or supply current sensing, has played an important role in the development of new opamps, e.g. the current-feedback opamp [14], or its extension, the operational floating conveyor (OFC) which has both a H input and H output.

All operational amplifiers are already known, with exception of hybrid input (e.g. current and voltage) to output current (*H-I amplifier*). We decided to call it *current-feedback OTA (CFB OTA)*, although it is a current amplifier with an additional voltage input [14]. The mean idea behind this decision was to maintain the symmetry in the classification.

It should be mentioned here that the same functionality can also be described from a completely different theoretical back-ground. One can show that the so-called *infinite-gain second-generation current conveyor (CCII ∞)* from [15] is essentially the same as the CFB OTA. The background from which it came is, however, different, the CCII ∞ was developed on the transistor level in order to optimize the trade-off between speed and distortion in current amplifiers. The CFB OTA shown in **Figure 1** is described by:

$$i_1 = 0, v_2 = v_1, i_3 = -A_i i_2, i_4 = A_i i_2, A_i = \infty. \quad (1)$$

3. Proposed of CMOS CFOA

Our design technique of CMOS CFOA consists of two stages, the first stage is the CFB OTA cascading with class AB cross-coupled buffer as second stage as shown in **Figure 2** to provide high current drive capability as mention in Section 1. We start by designing fully differential folded cascode OTA using Gm/Id technique in strong inversion region [16]. The current equation of OTA signifies that the transconductance of OTA strongly depends on the bias current [16] and is given by

$$I_d = G_m \{V_{in}(+) - V_{in}(-)\} \quad (2)$$

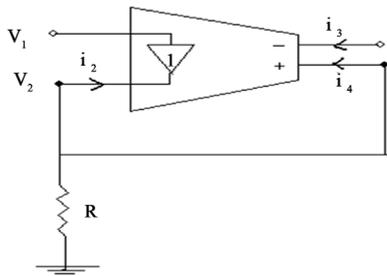


Figure 1. Block diagram of current feedback operational transconductance amplifier (CBA OTA).

The operation of folded cascode OTA consists of one differential pair consisting of NMOS transistors M_1 and M_2 . MOS transistors M_{12} and M_{13} provide the DC bias voltage to M_{11} transistor. The folded cascode OTA characterized by performance such as high DC voltage gain, wide gain bandwidth product, low noise and consumption power [17]. The gain of the folded cascode OTA is given by:

$$V_o/V_{in} = G_{m1}R_o \quad (3)$$

and the gain bandwidth product is given by:

$$GBW = G_{m1}/C_L \quad (4)$$

where G_{m1} is the transconductance of transistor M_1 and R_o (output resistance) = (R_o looking into drain of M_4)/(R looking into transistor into drain of M_8). After applying the design strategy clarified previously, the design parameters in strong inversion region, the gate-dimensions, biasing currents, and overdrive voltages of MOS transistors are summarized in **Table 1**.

4. Simulation Results

A new alternative CMOS CFOA with high performance operation, very low input offset voltage and low distortion is proposed in this paper. Since, the high frequency parameters such as voltage gain, (-3 dB) bandwidth, slew rate (SR), settling time (t_s) and gain bandwidth product (GBW) are improved. **Figure 3** clarifies the improvement in the open loop voltage gain and gain bandwidth product (GBW) of the proposed CMOS CFOA. In addition, the magnitude curve shows the frequency response (variation of frequency against the voltage gain and phase curve show the variation of frequency against the phase shift between input and output voltage. The value of output impedance of buffer stage is decreased drastically due to using cross-coupled buffer stag we note

Table 1. Gate dimensions and biasing currents of MOS transistors of proposed CMOS CFOA.

Transistors no.	Gate dimensions and biasing currents		
	W (μm)	L (μm)	Biasing current (μA)
M_1, M_2	12.0	0.35	50.0
M_3, M_4	16.1	0.35	50.0
M_5, M_6	11.59	0.35	100.0
M_7, M_8, M_9, M_{10}	6.21	0.35	50.0
M_{11}, M_{12}	2.51	0.35	100.0
M_{15}	9.5	0.35	100
M_{16}	2.0	0.35	100
M_{17}	23.8	0.35	100
M_{18}	6.0	0.35	100

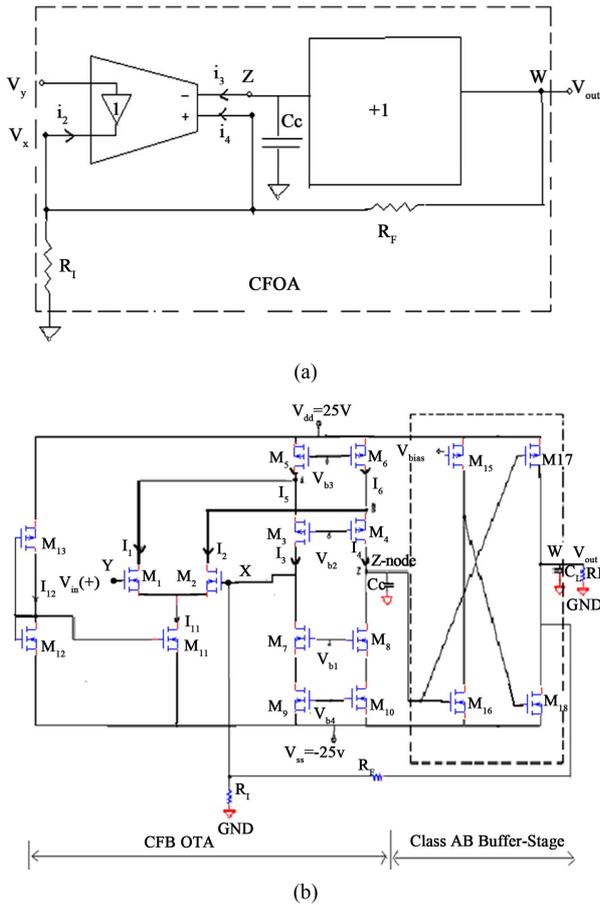


Figure 2. (a) Block diagram of proposed CMOS CFOA; (b) Schematic of proposed CMOS CFOA.

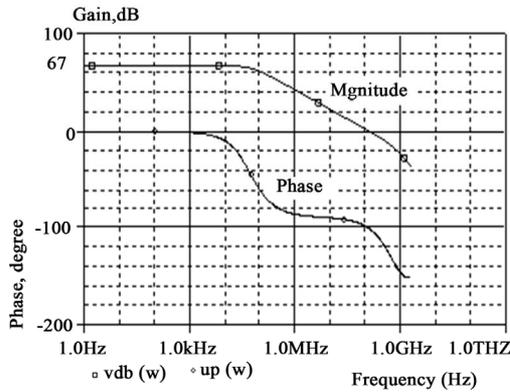


Figure 3. Open-loop frequency response of the proposed CMOS CFOA.

that in **Figure 4**. **Figure 5** indicates that the improvement in closed loop (-3 dB band width) of the proposed CMOS CFOA, since the values of (-3 dB bandwidth) is 104 MHz compared with 36.2 MHz with introduce the closed loop resistors are $R_F = 1$ K Ω and $R_I = 1$ K Ω . The value of voltage gain will increased with decreasing in the (-3 dB) bandwidth due to change the value of R_I and keep the

value of R_F is constant. The slew rate of CMOS CFOA are measured from **Figure 6**. DC characteristics of CMOS CFOA is shown in **Figure 7**, we note that there is a large enhancement in linearity of DC characteristics of the CMOS CFOA due to the symmetry in operation of the fully differential input stage of CFA OTA. Moreover, we note that the value of input offset voltage is -0.2 mV due to the symmetry in input stage (inverting and non inverting inputs) of the proposed CMOS CFOA. **Table 2** shows the effect of varies input resistors R_I value on the feedback loop gain and CMOS CFOA, closed loop voltage gain (A_v), gain bandwidth product (GBW), (-3 dB) bandwidth, phase margin (PM), and total harmonic distortion (HD). Simulation results of proposed CMOS

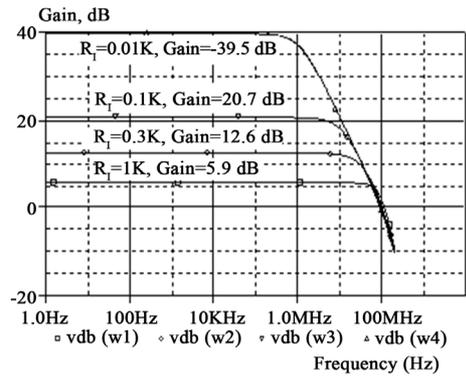


Figure 4. Closed-loop frequency response of the proposed CMOS CFOA with different values of R_I .

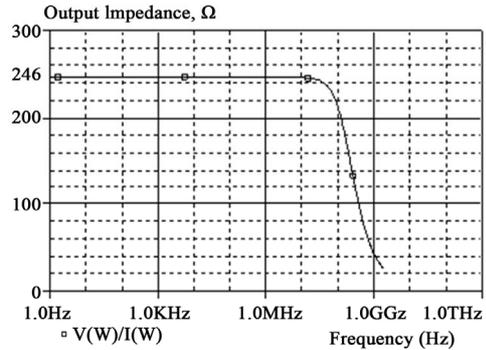


Figure 5. Output impedance of the proposed CMOS CFOA.

Table 2. Performance parameters of proposed CFOA with variation of Feedback resistance R_I .

Feedback resistance (R_I) K Ω	Performance parameters				
	-3 dB B.W MHz	GBW MHz	PM deg.	THD dB	A_v dB
1	79.6	104	49.9°	-67.0	5.9
0.3	32.7	89.2	48.6°	-65.0	12.5
0.1	10.7	81.8	46.0°	-41.7	20.4
0.01	1.0	78.6	45.0°	-41.0	39.1

CFOA confirmed the theoretical concepts in previous sections.

Table 3 Summarizes the comparison between several previous works and the proposed CFOA, we note there are a considerable improvement of performance parameters of proposed CFOA compared with previous works. Specially high frequency parameters, harmonic distortion and input offset voltage.

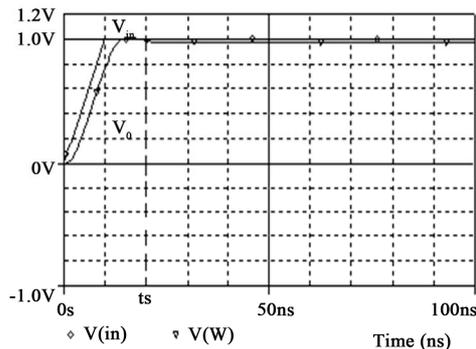


Figure 6. 1V Step response of the CMOS CFOA using (C_L) = 10 PF.

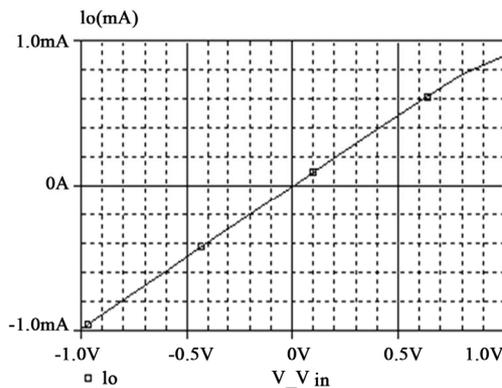


Figure 7. DC Characteristics of the CMOS CFOA with $R_L = 1 \text{ K}\Omega$.

Table 3. Summarize the comparison between several works.

Reference	[1]	[2]	[13]	Proposed CFOA
VDD, -VSS	1.5 V	3.3 V	0.75 V	2.5
Power dissipation	0.45 mW	5.3 mW	0.456 mW	5.5 mW
GBW	120 MHz	58 MHz	120 MHz	104 MHz
Input offset voltage	<20 mV	1.3 mV	<20 mV	0.2 mV
DC gain	-	74 dB	-	67 dB
Input voltage dynamic range	-0.65 V to +0.65 V	-	-0.65 V to +0.65 V	-1 V to +1V
THD	-	-83 dB	-	-67 dB
Technology	0.25 μm	0.35 μm	0.25 μm	0.35 μm

5. Conclusion

A new design technique of the CMOS CFOA with attractive features for high frequency, low offset voltage and low distortion is proposed in this paper. The proposed design based on cross-coupled buffer stage that connected as output stage of the CMOS CFOA. Since this technique operates on logic transition concept which gives the high speed, symmetry operation of the output signal and high current drive capability of proposed CMO CFOA. The high speed operation improved high performance parameters such as gain bandwidth (GBW), (-3 dB) bandwidth, slew rate (SR) and settling time (t_s) with ensure the phase margin (PM) in acceptable value that keep the stability of operation. Moreover, the symmetry of input differential of folded cascode CFA OTA technique decreased the distortion in output signal and improved (DC) characteristics of CMOS CFOA. In addition to that using folded cascode OTA (FC-OTA) as the input stage of CMOS CFOA make the symmetry of inverting and non inverting inputs that reduce input offset voltage. The trans-impedance node (Z) of the CMOS CFOA gained high value due to cascoding transistors of CFA OTA. This feature is very important for design CMOS CFOA with high gain. We can summarize our conclusion by saying that the proposed CMOS CFOA with symmetry of the input stage and symmetry of the output stage will gain CMOS CFOA attractive features for many high frequency, low distortion, low input offset voltage applications such as (A/D) converters, switched capacitor filters, active filters.

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