

Low Phase Noise and Wide Tuning Range VCO Using the MOS Differential Amplifier with Active Load

Cher-Shiung Tsai¹, Kwang-Jow Gan^{2*}, Ming-Shin Lin¹

¹Department of Electronic Engineering, Kun Shan University, Yongkang, Chinese Taipei

²Department of Electrical Engineering, National Chiayi University, Chiayi, Chinese Taipei

Email: gankj@ms52.hinet.net

Received June 18, 2012; revised July 18, 2012; accepted July 25, 2012

ABSTRACT

We demonstrate the design of a novel voltage-controlled oscillator (VCO), which is based on a metal-oxide-semiconductor field-effect transistor (MOS) differential amplifier with active load. This VCO achieves low phase noise and wide tuning range. The phase noise is -120 dBc/Hz at 600 KHz offset from a 1.216 GHz carrier frequency. This value is comparable to that of a LC-based integrated oscillator. The operating frequency can be tuned from 117 MHz to 1.216 GHz with the supply voltage varying from 1.3 V to 3.3 V. Therefore, the tuning range is about 90.38% which is larger than most of the LC and ring oscillator. The VCO circuit, which is constructed using a standard $0.35 \mu\text{m}$ CMOS technology, occupies only $26.25 \times 7.52 \mu\text{m}^2$ die area and dissipated 10.56 mW under a 3.3 V supply voltage.

Keywords: Voltage-Controlled Oscillator (VCO); Differential Amplifier; Phase Noise; Tuning Range

1. Introduction

Wireless communication systems contain low-noise amplifiers, mixers, power amplifiers, and phase-locked loops (PLLs). In particular, the PLL, which provides the function of frequency synthesis, is very important in designing such systems. The voltage-controlled oscillator (VCO) often plays the key element in PLL circuit. Designing VCO for the monolithic integration is always desirable but most challenging. In general, there are two main structures of designing the VCO in monolithic integration. One is the LC-based integrated oscillator and the other is the ring oscillator. The low phase noise, wide tuning range, and low power dissipation and are the most important factors of the basic design of a VCO. The operations of the LC oscillators are excellent in phase-noise performance but their tuning ranges are only about 10% to 20% [1-3]. Besides, they often require extra processes and occupy a large area of chip size due to the existence of inductor and capacitor. However, the ring oscillators have wide tuning range but they are poor in phase-noise performance.

In order to depress the phase noise, the differential pairs (or amplifiers) could be used in designing a VCO [3-5]. In this work, we design a novel VCO, which is designed based on a metal-oxide-semiconductor field-effect transistor (MOS) differential amplifier with active load. Its whole structure is like a ring oscillator. We can

obtain low phase noise and wide tuning range in this VCO. The phase noise is -120 dBc/Hz at 600 KHz offset from a 1.216 GHz carrier frequency. The operating frequency is tuned from 117 MHz to 1.216 GHz with the supply voltage varying from 1.3 V to 3.3 V. Therefore, the tuning range is as high as 90.38%. Wide tuning range is required in VCO for supporting broadband and multi-band RF transceivers. This VCO circuit, which is fabricated using a standard $0.35 \mu\text{m}$ CMOS technology provided by the Taiwan Semiconductor Manufacturing Company (TSMC) foundry, occupies $26.25 \times 7.52 \mu\text{m}^2$ die area and dissipated 10.56 mW under 3.3 V supply.

2. Circuit Design

The VCO demonstrated in this work is shown in **Figure 1**. This circuit is composed of a MOS-based differential amplifier, two standard CMOS inverters, and a buffer. It is an asymmetric structure and is similar to a ring oscillator. The differential amplifier is designed using two PMOS devices as the active load. This differential amplifier can achieve high voltage gain and output resistance. We use a NMOS device to act as a constant current source. Therefore, two NMOS devices (M1 and M2) can not be turned on simultaneously. When the M1 or M2 device is turned on, it is designed to be operated in the saturation state. The parameters of M1 device is designed as the same as those of M2 device. After the operation of this VCO circuit is stable, one of two NMOS devices should be turned on, and the other device should be turned off.

*Corresponding author.

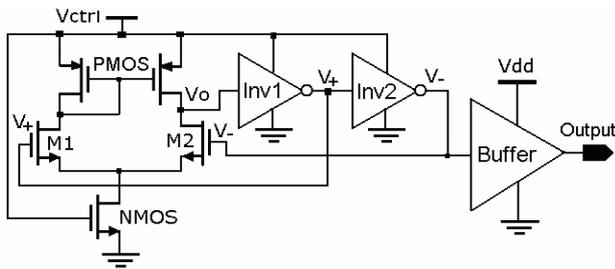


Figure 1. Circuit configuration of our proposed VCO structure.

The possible operation states of the V_+ , V_- and V_o are all listed in **Table 1**. V_+ , V_- are inputs and V_o is output of the differential amplifier with active load. There might be four possible states during the operation of this VCO circuit. The state 1 and state 2 will be only existed in the initial conditions. If the circuit is operated at the state 1 firstly, yet the next state will be changed to state 3 after the propagation of V_o . Then the operation of circuit will be transferred to state 4. Finally, the operation state will be back to state 3 again. As a result, the operation state will be alternately switched between state 3 and state 4. For the other possible condition, if the circuit is operated at the state 2 firstly, yet the following states will be changed to state 4 and state 3 in order. Therefore, the operation state will be located at state 4 and state 3 back and forth. Based on the discussion above, we can obtain the oscillation waveform. The buffer stage is composed of four cascaded CMOS inverters. The functions of the first and second stages are used as a wave-shaping modulator. However, the third and fourth stages are designed to amplify the amplitude of the output waveform and also to isolate the oscillator core from large capacitive load.

This VCO structure is a phase control operation circuit. The oscillation period will be the sum of time delays of the differential amplifier, inverter 1, inverter 2, and the buffer. The supply voltage of the differential amplifier, inverter 1, and inverter 2 is V_{ctrl} . The output oscillation frequency is proportional to the magnitude of the voltage V_{ctrl} . However, the bias V_{dd} for the buffer is fixed at 3.3 V in this design.

3. Measured Results

The VCO is implemented in a 0.35- μm N-well one-poly three-metal CMOS process provided by the TSMC foundry. The chip area is $26.25 \times 7.52 \mu\text{m}^2$. The measured output spectrum is shown in **Figure 2**. The center frequency is 1.216 GHz under a 3.3 V supply voltage, the resolution bandwidth is 100 KHz, and the output power peak is -2.72 dBm . The measured phase noise is shown in **Figure 3**. We can realize that the phase noise is -108.34 dBc/Hz at 100 KHz offset, -120 dBc/Hz at 600

Table 1. Possible operation states of the V_+ , V_- and V_o for the VCO circuit.

	V_+	V_-	V_o
State 1	H	H	L
State 2	L	L	H
State 3	H	L	H
State 4	L	H	L

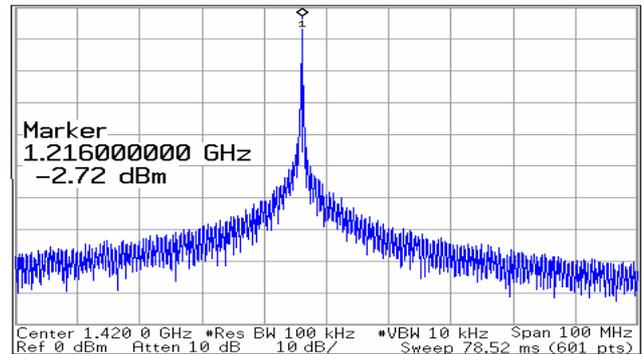


Figure 2. Measured output spectrum of the VCO circuit.

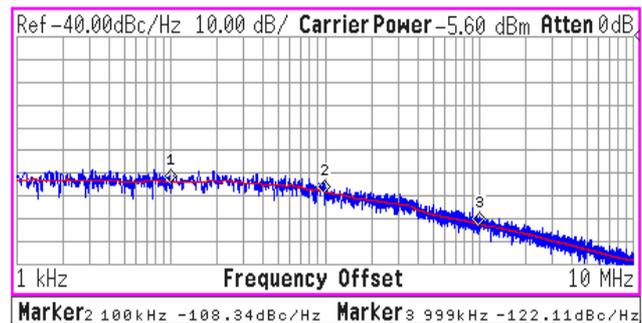


Figure 3. Measured phase noise of the VCO circuit at 1.216 GHz.

KHz offset, and -122.11 dBc/Hz at 1 MHz offset from a 1.216 GHz carrier frequency. Notice that the phase noise at 600 KHz offset is comparable with the LC-based integrated oscillators published in Refs. [1-3].

Figure 4 shows the comparison of the post-layout simulation and measured results of operating frequency with different supply voltages V_{ctrl} . The linearity of two curves is good. The frequency can be tuned from 117 MHz to 1.216 GHz with the supply voltage varying from 1.3 V to 3.3 V. The frequency is ranged from very high frequency (VHF) to ultra high frequency (UHF) bands. As shown, the tuning range is about 90.38%. It is much wider than that of the LC-based integrated oscillators [1-3]. **Figure 5** shows the comparison of the post-layout simulation and measured results of power dissipation with different supply voltages V_{ctrl} . The maximum dissipation power is about 10.56 mW under supply voltage 3.3 V. This value is reasonable in comparison with those

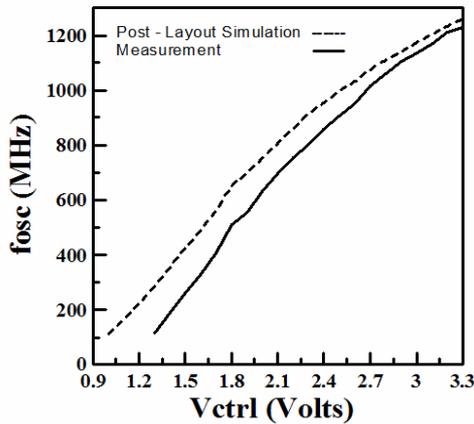


Figure 4. Comparison of the post-layout simulation and measured results of operating frequency with different supply voltages V_{ctrl} .

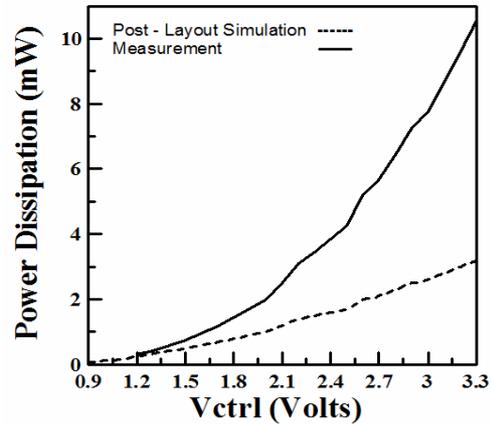


Figure 5. Comparison of the post-layout simulation and measured results of power dissipation with different supply voltages V_{ctrl} .

Table 2. Comparisons of our VCO circuit with the other oscillators.

Design	Process (μm)	Frequency Range (GHz)	Tuning Range (%)	Phase Noise (dBc/Hz @1MHz)	Power Dissipation (mW)	Type
This Work	0.35	0.117 - 1.216	90.4	-120	10.56	Ring
H. Wang, <i>et al.</i> [6]	0.25	1.99 - 2.73	27.10	-102	10	Ring
L. S. de Paula, <i>et al.</i> [7]	0.18	0.39 - 1.41	72.34	-89.79	16	Ring
J. Kim, <i>et al.</i> [8]	0.18	0.924 - 1.85	50.05	-127.1	10.8	LC
C. Shi, <i>et al.</i> [9]	0.18	1.71 - 2.19	21.91	-132	34	LC
G. Huang, <i>et al.</i> [10]	0.18	1.86 - 2.2	15.45	-134	36	LC

shown in Refs. [4,5]. The dissipation power is proportional to the $f \times CL \times V_{dd}^2$. The deviation between the simulated and measured curves might be resulted from the output parasitic loading capacitance.

Compared to the recently published papers [6-10], we have shown the relative VCO characteristics listed in **Table 2**. The phase noise of the circuits shown in Refs. [6-10] has been recalculated to an equivalent offset frequency of 1 MHz by assuming a dependence of 20 dB per decade. As shown, the phase noise is better than the ring oscillator [6,7], and is slightly larger than the complicated LC oscillators [8-10]. But the tuning range of our VCO circuit is the widest. Although the supply voltage of our proposed VCO circuit is 3.3 V, yet the power dissipation is competitive to the ring oscillator in Refs. [6,7] and better than the LC oscillators in Refs. [8-10]. This power dissipation could be decreased, if we implement this VCO circuit using a further scaled-down CMOS technique. Based on the above analysis, our VCO circuit possesses low phase noise, wide tuning range, and low power dissipation.

4. Conclusion

We present a novel VCO circuit, which is mainly con-

structed by a MOS-based differential amplifier with active load. This VCO can achieve low phase noise as the LC-based integrated oscillator and possess wide operating frequency range as the ring oscillator. The phase noise is -120 dBc/Hz at 600 KHz offset from a 1.216 GHz carrier frequency. The operating frequency can be tuned from 117 MHz to 1.216 GHz with the supply voltage varying from 1.3 V to 3.3 V. The tuning range is about 90.38%. This VCO circuit is fabricated using a standard 0.35 μm CMOS technology, occupies $26.25 \times 7.52 \mu\text{m}^2$ die area and dissipated 10.56 mW under 3.3 V supply. A prototype PLL (Phase-Locked Loop) uses the same VCO and will be implemented in the future.

5. Acknowledgements

This work was financially supported by the National Science Council of Taiwan under the contract no. NSC 97-2221-E-168-046. The authors would like to thank the Chip Implementation Center (CIC) of Taiwan for their great assistance in arranging the fabrication of this chip.

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