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Grounded and Floating Inductance Simulation Circuits Using VDTAs

Dinesh Prasad*, D. R. Bhaskar
Department of Electronics and Communication Engineering, Faculty of Engineering and Technology, Jamia Millia Islamia, New Delhi, India
Email: *dprasad@jmi.ac.in, dbhaskar@jmi.ac.in

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ABSTRACT

New electronically-controllable lossless grounded and floating inductance simulation circuits have been proposed employing Voltage Differencing Transconductance Amplifiers (VDTA). The proposed grounded inductance (GI) circuit employs a single VDTA and one grounded capacitor whereas the floating inductance (FI) circuit employs two VDTAs and one grounded capacitor. The workability of the new circuits has been verified using SPICE simulation with TSMC CMOS 0.18 μm process parameters.

Keywords: VDTA; Inductance Simulation; Filters

1. Introduction

Several circuits and techniques for the simulation of grounded and floating inductance employing different active elements such as operational amplifiers, current conveyors, current controlled conveyors, current feedback operational amplifiers, operational mirrored amplifiers, differential voltage current conveyors, current differencing buffered amplifiers, current differencing transconductance amplifiers, operational transconductance amplifiers (OTAs) have been reported in the literature see [1-33] and the references cited therein. Many active elements have been introduced by Biolek, Senani, Biolkova and Kolka in [34], VDTA is one of them. A CMOS realization of VDTA and its filter application have also been reported in [35]. The purpose of this pa- per is, to propose new electronically-controllable VDTA- based lossless GI and FI circuits employing a grounded capacitor. The GI uses only one VDTA along with a grounded capacitor and does not require any matching condition whereas FI employs two VDTAs, a grounded capacitor and requires matching conditions. The worka- bility of the proposed new circuits has been verified us- ing SPICE simulation with TSMC CMOS 0.18 μm proc- ess parameters.

2. The Proposed New Configurations

The symbolic notation of the VDTA is shown in **Figure 1**, where V_P and V_N are input terminals and Z, X^+ and X^- are output terminals. All terminals of VDTA exhibit high impedance values [35]. The VDTA can be described by the following set of equations:

$$\begin{bmatrix} I_Z \\ I_{X^+} \\ I_{X^-} \end{bmatrix} = \begin{bmatrix} g_{m_1} & -g_{m_1} & 0 \\ 0 & 0 & g_{m_2} \\ 0 & 0 & -g_{m_2} \end{bmatrix} \begin{bmatrix} V_{V_P} \\ V_{V_N} \\ V_Z \end{bmatrix} \quad (1)$$

The proposed grounded and floating inductance circuits are shown in **Figures 2** and **3** respectively.

A routine circuit analysis of the circuit shown in **Figure 2** results in the following expression for the input impedance

$$Z_{\text{in}}(s) = \frac{V_{\text{in}}(s)}{I_{\text{in}}(s)} = s\left(\frac{C}{g_{m_1} g_{m_2}}\right) \quad (2)$$

The circuit, thus, simulates a grounded inductance with the inductance value given by

$$L_{eq} = \frac{C}{g_{m_1} g_{m_2}} \quad (3)$$

which is electronically controllable by either g_{m_1} or g_{m_2}.

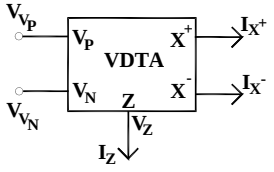

Figure 1. The symbolic notation of VDTA.

*Corresponding author.

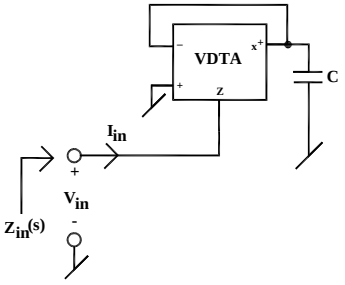

Figure 2. Proposed grounded inductance simulation configuration.

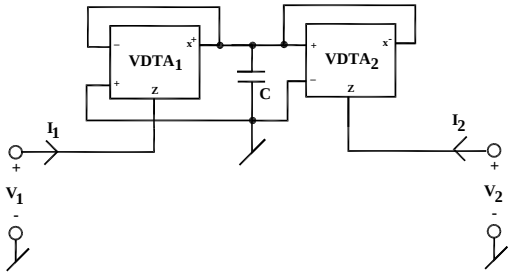

Figure 3. Proposed floating inductance simulation configuration.

On the other hand, analysis of the new FI circuit shown in **Figure 3** yields $\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{g_{m_1} g_{m_2}}{sC} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$, with $g_{m_1} = g_{m_3}$ and

$$g_{m_2} = g_{m_4} \tag{4}$$

which proves that the circuit simulates a floating lossless electronically-controllable inductance with the inductance value given by

$$L_{eq} = \frac{C}{g_{m_1} g_{m_2}} \tag{5}$$

3. Non-Ideal Analysis and Sensitivity Performance

Considering the various VDTA non-ideal parasitics *i.e.*, the finite X-terminal parasitic impedance consisting of a resistance R_X in parallel with capacitance C_X and the parasitic impedance at the Z-terminal consisting of a resistance R_Z in parallel with capacitance C_Z.

The non-ideal input impedance for the circuit shown in **Figure 2** is given by

$$Z_{in}(s) = \frac{\left\{ s(C+C_x) + \frac{1}{R_x} \right\}}{\left\{ s^2 C_z (C+C_x) + s\left\{ \frac{(C+C_x)}{R_z} + \frac{C_z}{R_x} \right\} + \frac{1}{R_x R_Z} + g_{m_1} g_{m_2} \right\}} \tag{6}$$

From Equation (6) a non-ideal equivalent circuit of the grounded inductor is derivable which is shown in **Figure 4**.

Where $L_{GI} = \frac{(C+C_x) R_x R_z}{\left(1 + g_{m_1} g_{m_2} R_x R_z\right)}$, $R' = \frac{(C+C_x) R_x R_z}{R_x (C+C_x) + R_z C_z}$, $C' = \frac{(C+C_x) R_x + C_z R_z}{R_z}$, $R'' = \frac{R_z}{\left(1 + g_{m_1} g_{m_2} R_x R_z\right)}$ and $D = R_x R_z (C+C_x)$

From the above, the sensitivities of L_{GI} with respect to various active and passive elements are found to be

$$S_C^{L_{GI}} = \frac{C}{(C+C_x)},\ S_{C_x}^{L_{GI}} = \frac{C_x}{(C+C_x)},\ S_{R_x}^{L_{GI}} = \frac{1}{\left(1 + g_{m_1} g_{m_2} R_x R_z\right)} = S_{R_z}^{L_{GI}},\ S_{g_{m1}}^{L_{GI}} = -\frac{g_{m_1} g_{m_2} R_x R_z}{\left(1 + g_{m_1} g_{m_2} R_x R_z\right)} = S_{gm2}^{L_{GI}} \tag{7}$$

Similarly, for the circuit shown in **Figure 3**, the input-output current and voltage relationships are given by:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{g_{m_1} g_{m_2}}{\left\{ s(C+2C_x) + \frac{2}{R_x} \right\}} \begin{bmatrix} 1 + \left\{ s(C+2C_x) + \frac{2}{R_x} \right\}\left(sC_z + \frac{1}{R_z} \right) & -1 \\ -1 & 1 + \left\{ s(C+2C_x) + \frac{2}{R_x} \right\}\left(sC_z + \frac{1}{R_z} \right) \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

with $g_{m_1} = g_{m_3}$ and $g_{m_2} = g_{m_4}$ (8)

The non-ideal equivalent circuit of floating inductor of **Figure 3** is derivable from Equation (8) and is shown in **Figure 5**.

where $L_{FI} = \frac{(C+2C_x)}{g_{m_1} g_{m_2}}$ and $R = \frac{2}{R_x g_{m_1} g_{m_2}}$

The various sensitivities of L_{FI} with respect to active and passive elements are:

$$S_C^{L_{FI}} = \frac{C}{(C+2C_x)},\ S_{C_x}^{L_{FI}} = \frac{C_x}{(C+2C_x)},$$

$$S_{g_{m1}}^{L_{FI}} = -1,\ S_{g_{m2}}^{L_{FI}} = -1 \tag{9}$$

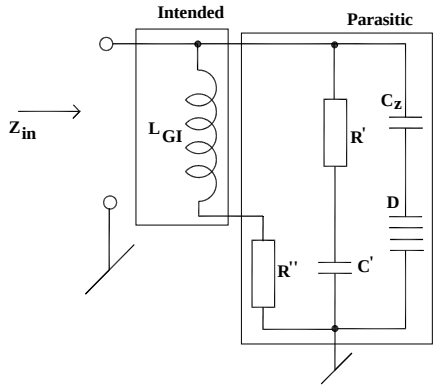

Figure 4. Non-ideal equivalent circuit of Figure 2.

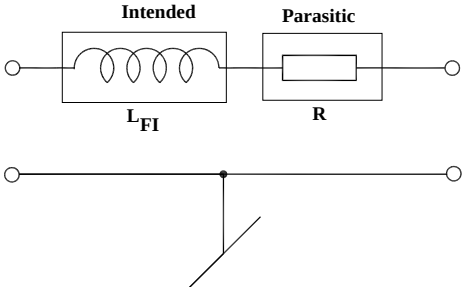

Figure 5. Non-ideal equivalent circuit of Figure 3.

Taking $g_{m1} = g_{m2} = 631.702$ μA/V, $C_z = C_Z = 0$, $R_x = R_z = \infty$ and C = 0.01nF, these sensitivities are found to be (1, 0, 0, 0, 1, 1) and (1, 0, –1, –1) for Equations (7) and (9) respectively. Thus, all the passive and active sensitivities of both grounded and floating inductance circuits are low.

4. Simulation Results of the New Proposed Grounded/Floating Inductance Configurations

The workability of the proposed simulated inductors has been verified by realizing a band pass filter (BPF) as shown in **Figures 6** and **7**.

The transfer function realized by this configuration is given by

$$\frac{V_0}{V_{in}} = \frac{s\left(\frac{1}{R_1C_1}\right)}{s^2 + s\left(\frac{1}{R_1C_1}\right) + \left(\frac{g_{m_1}g_{m_2}}{C_1C_2}\right)} \qquad (10)$$

from where it is seen that bandwidth and centre frequency both are independently tunable, the former by R_1 and the latter by any of the transconductances g_{m1}, g_{m2} and C_2.

The transfer function realized by the configuration shown in **Figure 7** is given by

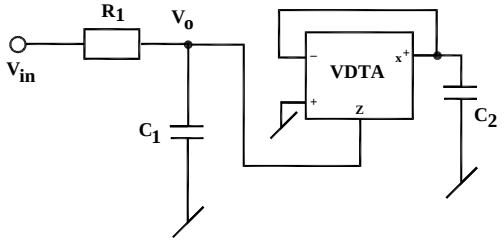

Figure 6. Band pass filter realized by the new grounded simulated inductor.

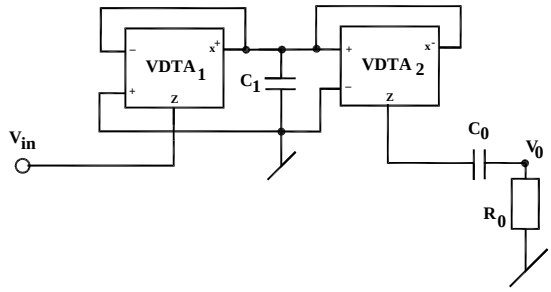

Figure 7. Band pass filter realized by the new floating simulated inductor of Figure 3.

$$\frac{V_0}{V_{in}} = \frac{s\left(\frac{R_0 g_{m_1} g_{m_2}}{C_1}\right)}{s^2 + s\left(\frac{R_0 g_{m_1} g_{m_2}}{C_1}\right) + \frac{g_{m_1} g_{m_2}}{C_0 C_1}} \quad \text{with} \quad g_{m_1} = g_{m_3}$$

$$\text{and} \qquad g_{m_2} = g_{m_4} \qquad (11)$$

In this case, bandwidth is tunable by R_0 whereas centre frequency can be tuned by C_0.

Performance of the new simulated inductors was verified by SPICE simulations. CMOS-based VDTA from [35] was used to determine the frequency responses of the grounded and floating simulated inductors. The following values were used for grounded as well as floating inductor: $C = 0.01$ nF, $g_{m1} = g_{m2} = 631.7$ μA/V. From the frequency response of the simulated grounded inductor (**Figure 8**) it has been observed that the inductance value remains constant upto 10 MHz. Similarly, from the frequency response of the simulated floating inductor (**Figure 9**) the inductance value also remains constant up to 10 MHz.

To verify the theoretical analysis of the application circuits shown in **Figures 6** and **7**, these configurations have also been simulated using CMOS VDTAs. The component values used were for **Figure 6**: $C_1 = 5$ pF, $C_2 = 0.01$ nF, $R_1 = 1.58$ kΩ and for **Figure 7**: $C_0 = 0.01$ nF, $C_1 = 5$ pF, $R_0 = 1.58$ kΩ. The VDTAs were biased with ±0.9 volts D.C. power supplies with $I_{B1} = I_{B2} = I_{B3} = I_{B4} = 150$ μA. **Figures 10** and **11** show the simulated filter responses of the BP filters. A comparison of the other

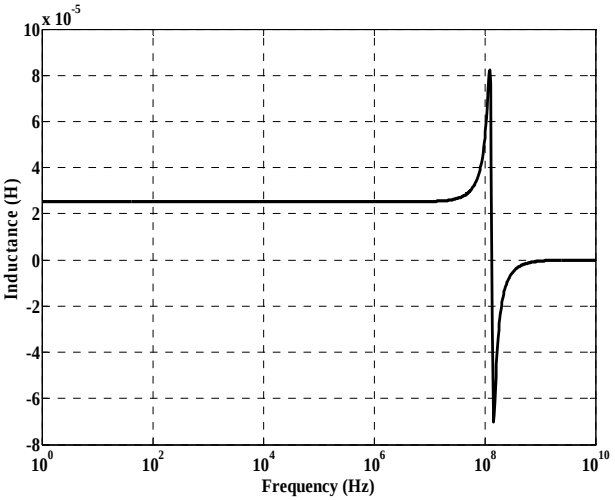

Figure 8. Frequency response of the simulated grounded inductor.

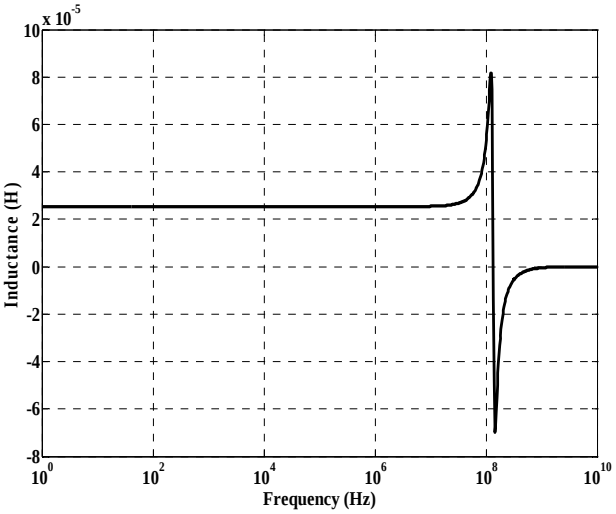

Figure 9. Frequency response of the simulated floating inductor.

previously known grounded and floating inductance simulators has been presented in **Table 1**.

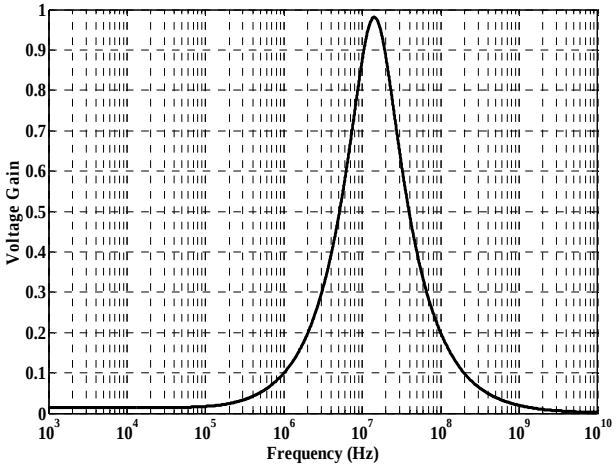

Figure 10. Frequency response of BPF using the proposed simulated GI.

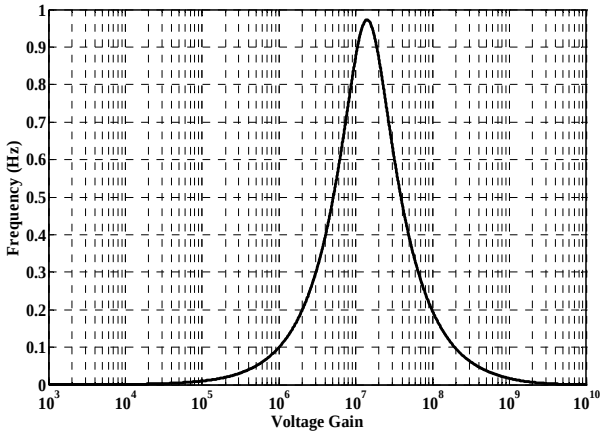

Figure 11. Frequency response of BPF using the proposed simulated FI.

Table 1. Comparison with other previously known grounded and floating simulators.

Reference	Inductance type[+]	Number of active devices	Number of resistors	Number of capacitors	Required Matching condition	Electronic Tunable Inductance
[4]	F	3	3	1	YES	NO
[7]	G	2	0	1	NO	YES
[10]	F	3	0	1	YES	YES
	F	4	4	1	YES	NO
[11]	F	4	3	1	YES	NO
[12]	F	4	2	1	NO	NO
[14]	G	2	2	1	NO	NO
[15]	F	3	2	1	NO	NO
[16]	F	3	2	1	NO	NO
[17]	F	4	2	1	NO	NO
[18]	F	2	2	1	NO	NO
[22]	F	3	0	1	YES	YES

Continued

[23]	F	3/4	4	1	YES	YES
[24]	G	1	2	1	YES	NO
[25]	F	3	0	1	YES	YES
[26]	F	4/3	3	1	NO	NO
[27]	G	2	0	1	NO	YES
[28]	G	3	3	1	NO	NO
[29]	G	3	4	1	NO	NO
[30]	F	3	4	1	NO	NO
	G	2	0	1	NO	YES
[32]	F	3	0	1	YES	YES
	G	2	0	1	NO	YES
[33]	F	3	0	1	YES	YES
	F	2	3	2	YES	NO
Proposed	G	1	0	1	NO	YES
	F	2	0	1	YES	YES

G = Grounded, F = Floating.

The above results, thus, confirm the validity of the applications of the proposed grounded and floating simulated inductance circuits.

5. Conclusion

New electronically-controllable circuits of lossless grounded and floating inductance have been proposed employing VDTAs. The proposed grounded inductance circuit employs only one VDTA and one grounded capacitor. On the other hand, the floating inductance configuration uses two VDTAs and one grounded capacitor, requires realization conditions for floatation. A comparison of the other previously known grounded and floating inductance simulators has been presented in **Table 1**. The SPICE simulation results have confirmed the workability of the new proposed circuits.

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