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High-Performance CMOS Current Mirrors: Application to Linear Voltage-to-Current Converter Used for Two-Stage Operational Amplifier

Radwene Laajimi, Mohamed Masmoudi
Department of Electrical Engineering Electronics, Micro-Technology and Communication (EMC) Research Group Sfax (ENIS), University of Sfax, Sfax, Tunisia
Email: radwene_fac@hotmail.fr

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ABSTRACT

This paper presents two schemes of high performance CMOS current mirror, one of them is used for operational transconductance amplifier (OTA) in analog VLSI systems. The linearity, output impedance, bandwidth and accuracy are the most parameters to determine the performance of the current mirror. Here a comparison of two architectures based on same architecture of the amplifier is presented. This comparison includes: linearity, output impedance, bandwidth and accuracy. These two circuits are validated with simulation in technology AMS 0.35 µm. An operational amplifier based on the adapted current mirror is proposed. Its frequency analysis with large bandwidth is validated with the same technology.

Keywords: Analog Circuits; Current Source; Current Mirror; Low Voltage; Operational Transconductance Amplifier

1. Introduction

In the last few years, the demand for analog circuits which can operate at low voltage is an established fact and does not need any further justification. In particular structures of current mirrors which have increased rapidly and become one of the most interesting areas of research [1]. Many configurations of current mirror are discussed and used for many applications. Especially cascode current mirror which is one of the main building blocks of analog and mixed-signal integrated circuits. For low voltage design circuit and high speed application, the important parameters to determine high performance current mirror are [2-4]:

- Low input and output voltage.
- Low input impedance.
- High output impedance.
- Minimum error of copying accuracy and settling time.

The four transistors circuit shown in **Figure 1(a)** is a simple cascode current mirror and it is characterized by moderately low input and output voltages.

Equation (1) of input voltage is:

$$V_{\text{in}} = 2V_{\text{DSAT}} + 2V_T \tag{1}$$

Equation (2) of output voltage is:

$$V_{\text{out}} = 2V_{\text{DSAT}} + V_T \tag{2}$$

(V_{DSAT} and V_T denote is the minimum drain-source saturation voltage and the transistor's threshold voltage.)

This circuit has higher output impedance than the simple current mirror and moderately high input impedance.

Equation (3) of input impedance is:

$$Z_{\text{in}} = \frac{1}{gm_{11}} + \frac{1}{gm_{12}} \tag{3}$$

Equation (4) of output impedance is:

$$Z_{\text{out}} = \frac{gm_9}{go_9 \cdot go_{10}} \tag{4}$$

(where *gm* and *go* are the small-signal transconductance gain and the conductance of the MOS transistor, respectively.)

A simple variation of this circuit is shown in **Figure 1(b)** [5]. In this scheme the variable voltage V_{ar} with resistance R1 are added. They are injected between the drain of transistor M12 and the source of transistor M11. The drain source voltage of the mirror transistor M12 is forced to a constant value by means of transistor M11, current I_{in} and variable voltage V_{ar}. Thus, on one hand, a reduction of the input impedance by the gain of M11. On the other hand, it reduces the input voltage requirements. In this case, the input voltage can be set to its minimum value by proper selection of the variable voltage Var. Hence, this scheme achieves low input impedance with low input voltage requirements but with some limitation due to the difference between the current in M11 and M9. This difference causes a mismatch in the drain source

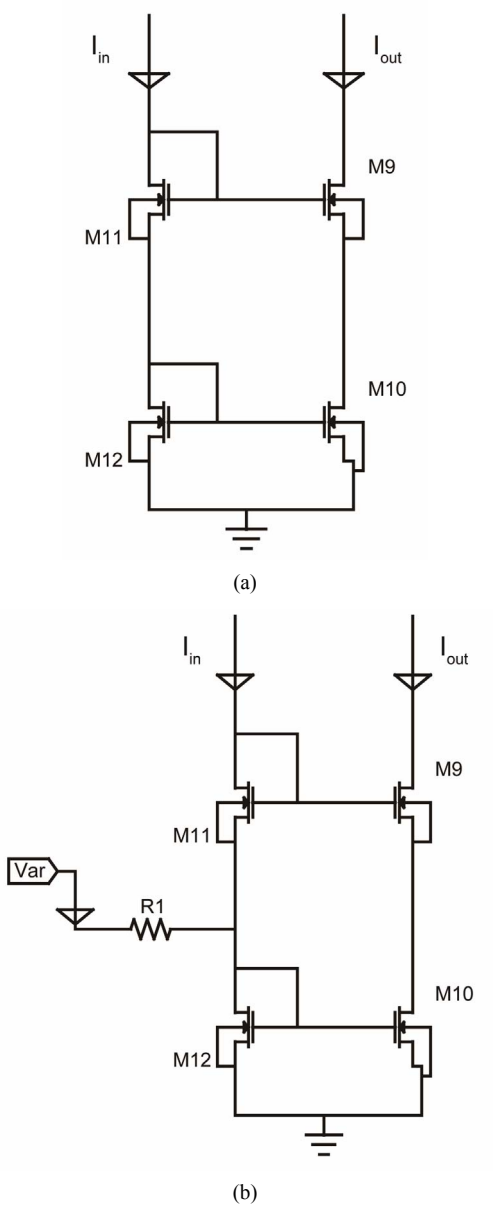

Figure 1. Current mirror configuration. (a) Simple cascode current mirror; (b) Cascode current mirror with regulated voltage.

voltage of M10 and M12 and results in a loss of accuracy, so degraded linearity (due to channel length modulation).

To overcome this limitation, we are proposing two novels structures of current mirror which offers both the low compliance voltage and a minimum error of copying accuracy. The two proposed approaches are based on using a differential amplifier to compare the drain voltages of the input and output mirror transistors, to force the equality between these voltages, thereby improving the accuracy of the current copy, and improving linearity.

The paper is organized as follows. The second section presents the amplifiers structures used for voltage to current (V-I) converter. In the third section, the design of proposed version 1 of V-I converter is presented with simulations results. The proposed version 2 of V-I converter is presented in section four. Section 5 presents an application of V-I converter in two-stage operational amplifier. Conclusion is drawn in the last section.

2. Amplifier Structures

In order to achieve high current copy accuracy, it is necessary to use an amplifier between the mirror's input and output transistors.

The amplifier architectures are: simple differential amplifier [6] and amplifier proposed by [5]. As shown in **Figure 2(a)**, this structure is formed by the input differential pair (MP1 and MP2) and the active charge (MN1 and MN2). The **Figure 2(b)** shows a differential amplifier with two MOS transistors (MN1 and MN2) in which MN1 is operated in the weak version region (source gate voltage of MN1 equal to zero). This version can operate either in the linear region or in the saturation region for achieving low voltage and low consumption.

Moreover, the amplifier, which has many transistors, causes the increase of the power dissipation and the chip area. The advantages of the scheme proposed by [7] are low voltage operation, small chip area, high output resistance and no bias current. For this reason we use this structure in our two versions of voltage to current converter which are more described in the following paragraph.

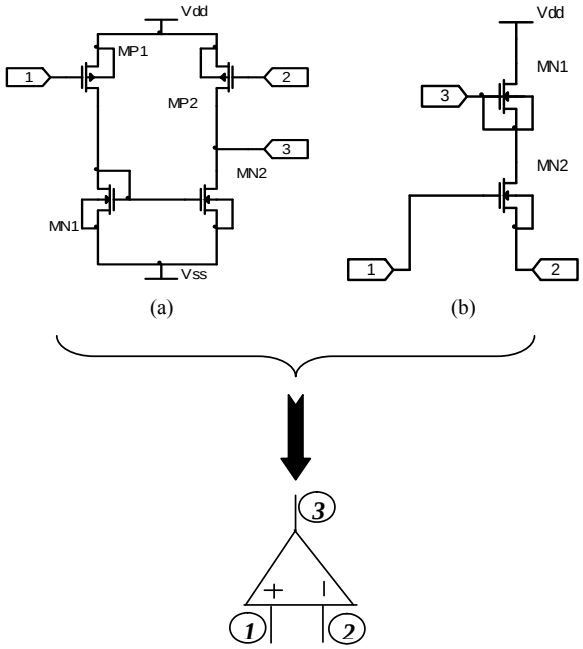

Figure 2. Amplifier configuration. (a) Simple differential amplifier structure [6]; (b) Two-transistor apmlifier structure [7].

3. Proposed Version 1 of Voltage to Current Converter

3.1. Description

According to **Figure 3** the version 1 of V-I converter is composed of three blocks: polarisation, correction and output load.

The polarisation block is formed of four transistors (MP1, MP2, MP3, MP4) with variable input voltage V_{in} and input resistance R_{in}. The correction block is composed of three transistors (M1, M2, MC2). It characterized by minimum error of copying accuracy due to the equality of drain source voltage between M1 and M2. This equality thanks to an amplifier between the mirror's input and output transistors M1 and M2 and causes high accuracy and good linearity. High output impedance is obtained by the output current of amplifier and passes to the gate of transistor MC2. The output load block is a simply resistance (R_{out}).

This scheme offers a comparison between drain source voltage of M1 and M2 by using a differential amplifier to provide higher accuracy of the current copy. The input injection current signal I_{in} is replaced by another source formed by variable input voltage V_{in} with resistance R_{in}. On the one hand, we obtain a reduction of the input impedance which given by this relation:

Equation (5) of input impedance is:

$$Z_{in} = \frac{1}{gm_1 \,.\, A_{olinp}} \tag{5}$$

Equation (6) presents moderate output impedance

$$Z_{out} = ro_2 \cdot A_{olout} = ro_2 \cdot Av_{MC2} \cdot Av_{omp} \tag{6}$$

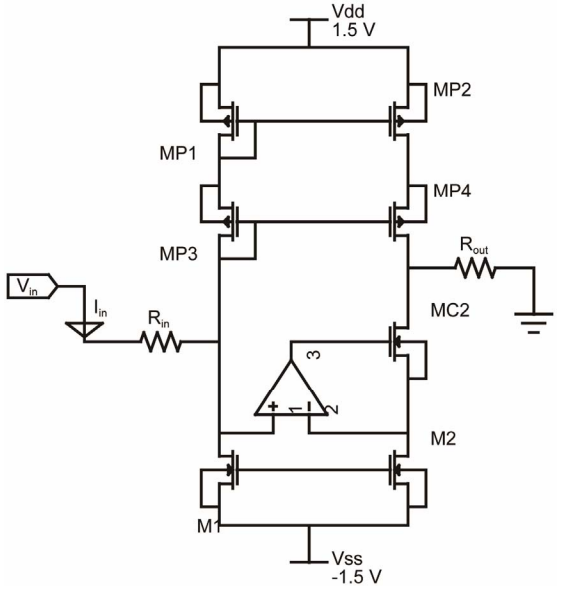

Figure 3. Proposed version 1 of voltage to current converter.

where *gm* and *ro* are the small-signal transconductance gain and the output resistance of the MOS transistors. In this case we assume that the amplifier have an input open-loop gain A_{olinp} and output open-loop gain A_{olout} ($A_{olout} = Av_{MC2} \cdot Av_{omp}$). Av_{MC2} and Av_{omp} denote the voltage gain of the transistor MC2 and amplifier gain respectively.

On the other hand, the drain source voltage of the mirror transistor M1 achieves a small constant value thanks to current source I_{in} and variable voltage source V_{in}. Drain source voltage can be decreasing to a minimum value, by selection of V_{in} and consequently a very low input voltage of the circuit.

3.2. Simulations Results

Different schemes are simulated using Tspice based on BSIM3V3 transistor model for the technology AMS 0.35 µm at ±1.5 V power supply voltage.

Tspice simulations are carried for an input voltage V_{in} varied from −1.1 V to 0 V, **Figure 4** shows the DC characteristic for the V-I converter for different values of resistance (R_{out} = 100 Ω, R_{out} = 1 KΩ, R_{out} = 5 KΩ) in which the full input voltage swing capability is evident with truly linearity.

As shown in **Figure 5**, from DC output characteristics simulations, the output resistance presents a moderate value of 0.18 MΩ.

The **Figure 6** shows the AC characteristic of the proposed V-I converter. For a resistance of 100 Ω, we achieved a common gain bandwidth (GBW) equal to 750 MHz for different values of resistance (R_{out} = 100 Ω, R_{out} = 1 KΩ, R_{out} = 5 KΩ) and variable gain (*Av*) from 53 dB to 80.2 dB at minimum resistance (R_{out} = 100 Ω).

According to **Figure 7**, the deviation of the DC output current from the ideal characteristic for different values of resistance R_{out}. The large error is reached for the lowest input voltage V_{in} of −1.1 V. On the other hand the variation of V_{in} between −0.9 V to 0 V provide a small current error under 0.1% for different values of resistance (R_{out} = 100 Ω, R_{out} = 1 KΩ, R_{out} = 5 KΩ). Moreover for the maximum current error of 0.5%, V_{in} varied from −1.1 V to −0.95 V in particular for output resistance R_{out} = 5 KΩ.

4. Proposed Version 2 of Voltage to Current Converter

4.1. Description

The version 2 of V-I converter is presented in **Figure 8**. It is like the structure of version 1 shown in **Figure 3** and composed of three blocks: polarisation, correction and output load. The main difference is in the correction block. In which there are three transistors (M1, M2, MC2)

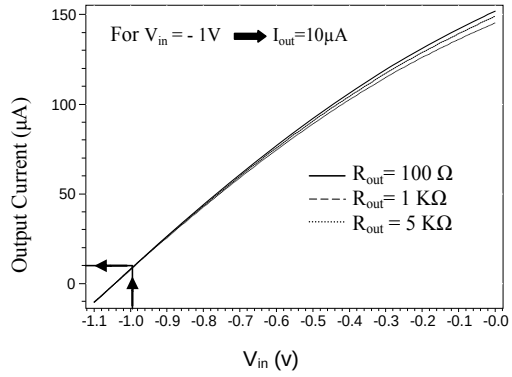

Figure 4. DC characteristics of V-I converter for different values of resistance R_{out}.

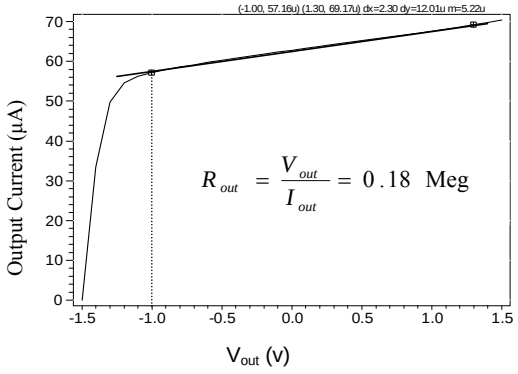

Figure 5. Output current vs output voltage variation of proposed V-I converter.

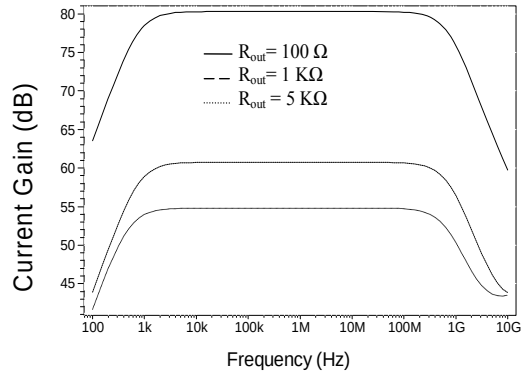

Figure 6. Frequency response of proposed V-I converter.

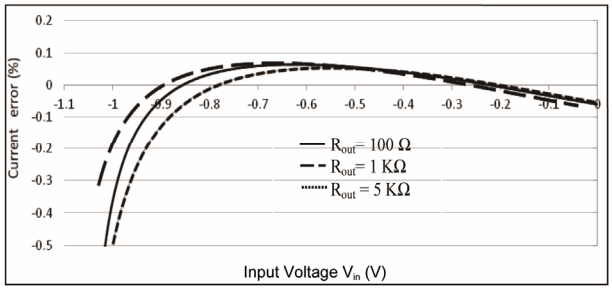

Figure 7. Current error of V-I converter.

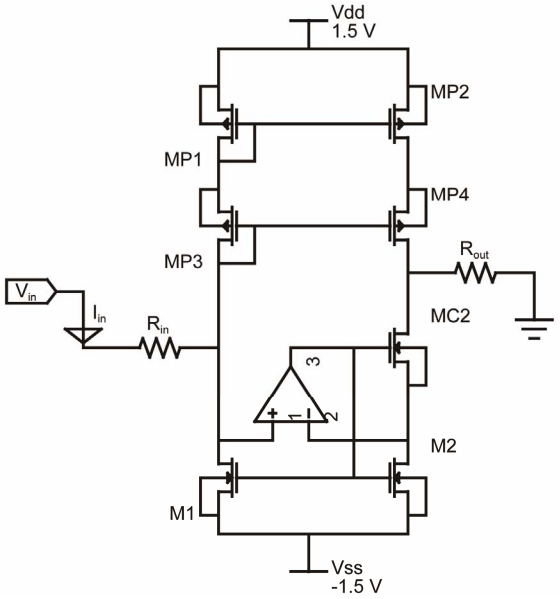

Figure 8. Proposed version 2 of voltage to current converter.

with an amplifier between M1 and M2 in order to minimise error of copying accuracy.

In this case of structure an approach is used to increase the output impedance without sacrificing the equality between input and output of drain source voltage (M1 and M2), consists in integrating a connection between the gate of transistor MC2 and the gate of transistor M2. We achieved very high output impedance due to the output current of amplifier. This current is passed through each gate of transistors MC2 and M2. Equation (8) shows the value of output impedance which is:

$$Z_{out} = ro_2 \cdot A_{olout} = ro_2 \cdot Av_{MC2} \cdot Av_{M2} \cdot Av_{omp} \quad (8)$$

ro_2 denote the output resistance of the MOS transistor M2. The amplifier has an output open-loop gain A_{olout}. Equation (9) give this relation:

$$A_{olout} = Av_{MC2} \cdot Av_{M2} \cdot Av_{omp} \quad (9)$$

We assume that Av_{MC2}, Av_{M2} and Av_{omp} denote the voltage gain of the transistor MC2, M2 and amplifier gain respectively.

4.2. Simulations Results

From Tspice simulations, an input voltage V_{in} varied from −1 V to 0 V, the DC characteristic for the V-I converter for different values of resistance (R_{out} = 100 Ω, R_{out} = 1 KΩ, R_{out} = 5 KΩ) is shown in **Figure 9**. We find that the linearity is evident for each value of resistance.

To confirm the high output resistance given by the proposed version 2 of V-I converter, **Figure 10** shows the DC output characteristics simulations. The value of the output resistance in this case is equal to 0.34 MΩ.

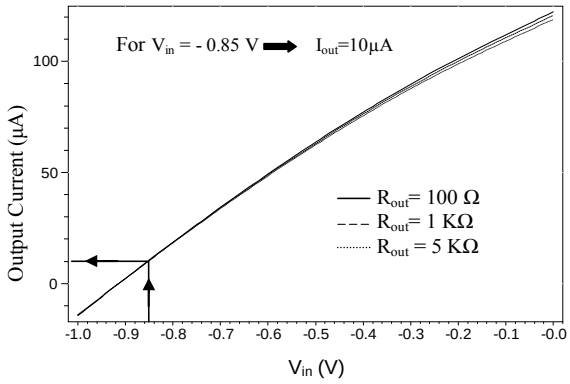

Figure 9. DC characteristics of V-I converter for different values of resistance R_{out}.

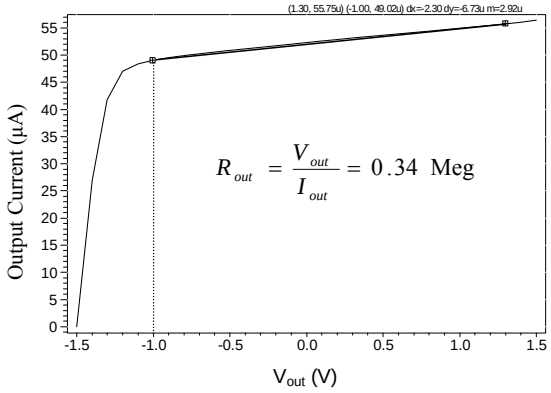

Figure 10. Output current vs output voltage variation of proposed V-I converter.

From AC characteristic, we note an improvement of the gain (*Av*). Its maximum value is 73 dB but it is 80.2 dB for the proposed version 1 of V-I converter. The bandwidth responses for different values of resistance are presented in **Figure 11**.

From **Figure 12**, we present a current error of V-I converter for different values of resistance R_{out}. On the one hand, the variation of V_{in} from −0.9 V to 0 V give the same characteristic of error for different values of resistance (R_{out} = 100 Ω, R_{out} = 1 KΩ, R_{out} = 5 KΩ). On the other hand for the maximum current error of 0.35%, V_{in} is lower than −0.95 V.

5. Application of V-I Converter in Two-Stage Operational Amplifier

Voltage to current V-I converter becomes the most interesting element of interface measurement in the field of mixed signal systems [8].

The most important parameters to determine high performance of current V-I converters are:

- High linear range.
- Large bandwidth and gain.

Because the large bandwidth and gain of the proposed version 1 of V-I converter, it is possible to use this approach for Operational amplifier [9,10]. The **Figure 13** shows a practical implementation of the two-stage Operational amplifier.

The simulated output frequency response of our application is shown in **Figure 14**. The bode diagram gives an open loop gain of 60 dB with a large GBW of 82 MHz, a 97 KHz of cut-off frequency and a phase margin of 62°. We note that the input current passes through M8 using for polarisation is equal to 10 µA and this corresponds to an input voltage V_{in} of −1 V.

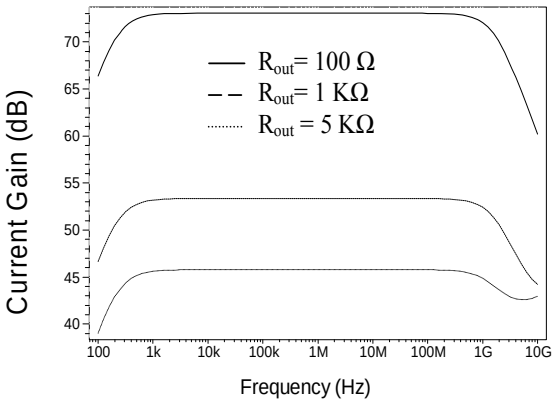

Figure 11. Frequency response of proposed V-I converter

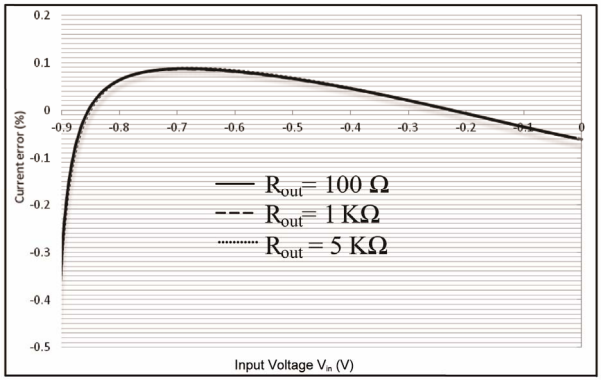

Figure 12. Current error of V-I converter.

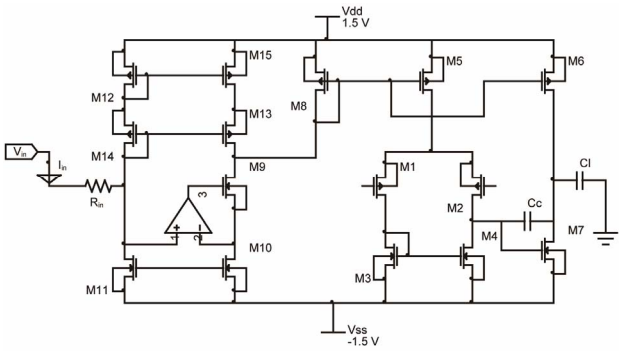

Figure 13. Proposed two-stage operational amplifier with proposed version 1 of V-I converter.

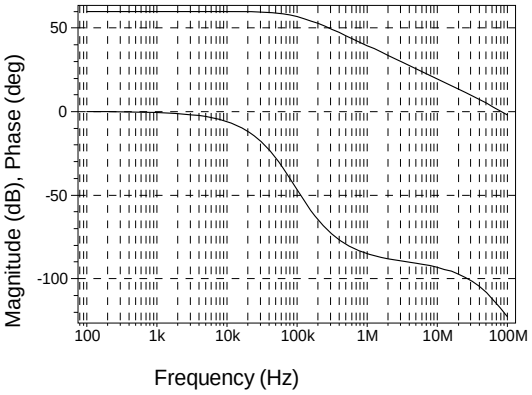

Figure 14. Frequency response of proposed V-I converter.

6. Conclusion

Current mirror play an important role in analog circuits used for V-I converter. This work presents two novels design of V-I converter. The version 1 of V-I converter is implemented in Two-Stage Operational Amplifier. However the version 2 gives high output impedance. The use of version 1 due to its large bandwidth of 750 MHz and gain of 80.2 dB. Simulations results of application of V-I converter in two-stage operational amplifier indicated that phase margin is 62˚ to ensure a good stability, gain of 60 dB for ±1.5 V, and GBW of 82 MHz.

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