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On-Chip Inductor Technique for Improving LNA Performance Operating at 15 GHz

El-Sayed A. M. Hasaneen, Nagwa Okely
Electrical Engineering Department, El-Minia University, El-Minia, Egypt
Email: hasaneen@netzero.net

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ABSTRACT

This paper presents a technique for low noise figure reduction of low-noise amplifier (LNA). The proposed LNA is designed in a source degeneration technique that offers lower noise figure. The resistance of the on-chip inductor is reduced by using multilayer that significantly reduces the thermal noise due to spiral inductor. Also, using spiral inductor as a gate inductor reduces the effect of the input parasitic capacitance on the noise figure and provides a good matching at the input and output of the LNA. The results of the LNA using multilayer on-chip inductor compared will off-chip inductor have been illustrated. It shows that the proposed technique reduces significantly the noise figure and improves the matching. The proposed LNA is designed in 0.13 μm process with 1.3 V supply voltage and simulated using Advanced Design System (ADS) software. The simulation results show that the LNA is unconditionally stable and provides a forward gain of 11.087 dB at operating frequency of 15 GHz with 1.784 dB noise figure and input and output impedance matching of –17.93 dB, and –10.04 dB.

Keywords: Low Noise Amplifier; On-Chip Inductor; Noise Figure; Cascade Amplifier; Scattering Matrix

1. Introduction

The communication market has been growing very fast during the last decade especially for mobile communication systems. The low noise amplifier is one of the most essential building blocks in the communication circuits. It can be found in the almost of the commercial and military receivers. The first stage followed the antenna, LNA, is the most critical stage because its noise figure dominates the overall communication systems. The main function of the LNA is to amplify the incoming signal while adding the minimum possible noise and also provides impedance matching. Additional requirement to the LNA is the low power consumption, which is especially important in portable communications systems [1]. Various techniques to improve the LNA performances were proposed [2-5].

In this paper, we propose a new technique for improving LNA performance. The proposed multilayer on-chip spiral inductor technique significantly decreases the value of inductor series resistance that reduces the contribution of the spectral noise current due inductor series resistance and provides a good matching at the LNA input and output. It also reduces the effect of the parasitic capacitance at the input of the LNA which considers one of the biggest problems in the LNA design. In our design, we use inductive source degeneration technique [5]. Source degeneration technique provides no additional noise generation since the real part of the input impedance does not correspond to a physical resistor that offers lower noise figure than the common-gate LNA. Although the distributed amplifiers [6] normally provide wide bandwidth characteristics but it tends to consume a large dc current due to the distribution of multiple amplifying stages, which make them unsuitable for low-power applications. The resistive shunt-feedback-based amplifiers [7] provide good wideband matching and flat gain, but they tend to suffer from poor noise figure (NF) and large power dissipation. It makes the inductive source degeneration technique the best topology for LNA with high gain, low noise figure, good matching and good stability.

This paper is organized as follows. Section 2 describes the proposed LNA circuit and analysis. Section 3 presents modeling of spiral inductor and Section 4 describes the noise analysis. The stability of the LNA is described in Section 5. Results and discussions are illustrated in Section 6 and followed by a conclusion in Section 7.

2. LNA Circuit Description and Analysis

Figure 1(a) shows the schematic circuit diagram of the proposed CMOS LNA with cascoded topology. An inductive source degeneration technique is used to provide

no additional noise generation. The cascode topology reduces the influence of the miller capacitance effect which strongly limits the frequency performance and gives a rise to a very poor reverse isolation [8]. It is also used to decouple miller effect from the gain of the circuit and to simplify the design matching network to the antenna. Because LNA directly interfaces with the antenna, a 50 Ω impedance matching is usually required at its input and it is very important to avoid reflections over the transmission line feeding LNA. So, additional tuning components are usually used to match it to the source impedance. The circuit shown in **Figure 1(a)** has purely capacitive input impedance. In order to create a resistive input, a source generation inductor L_S is connected to the source of the input transistor M_1 to provide an effective resistive input without contributing additional noise. The gate inductor L_g is used for input impedance matching which is required to transform upwards the equivalent impedance looking into the gate of M_1 and also it is used to optimize the noise figure.

Figure 1(b) shows the small-signal equivalent circuit for the input transistor M_1 and the overall LNA circuit. The capacitance C_{gs} represents the gate-source capacitance of the input transistor M_1, g_m is the MOS transconductance, and R_s is the source resistance, typically 50 Ω.

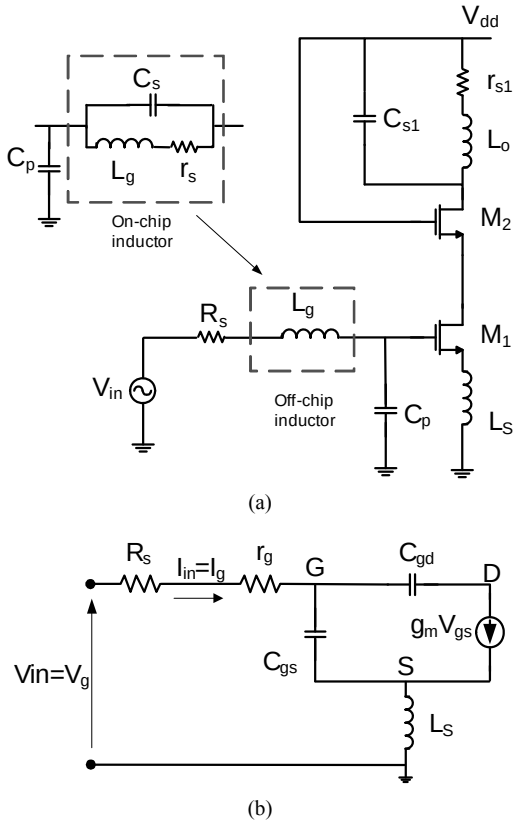

Figure 1. (a) Schematic circuit diagram of the proposed CMOS LNA; (b) Small-signal equivalent circuit.

The input impedance can be expressed as:

$$Z_{\text{in}} = \frac{V_g}{I_g} = \frac{V_{\text{in}}}{I_{\text{in}}} = \frac{V_{\text{in}}}{j\varpi C_{gs} V_{gs}} \tag{1}$$

where

$$\begin{aligned} V_{\text{in}} = {} & r_g \left(j\varpi C_{gs} V_{gs} \right) + j\varpi L_g \left(j\varpi C_{gs} V_{gs} \right) + V_{gs} \\ & + j\varpi L_s \left(g_m V_{gs} + j\varpi C_{gs} V_{gs} \right) \end{aligned} \tag{2}$$

Substituting (2) into (1) gives:

$$Z_{\text{in}} = r_g + \frac{g_m L_s}{C_{gs}} + j\varpi \left[\left(L_s + L_g \right) + \frac{1}{\left(j\varpi \right)^2 C_{gs}} \right] \tag{3}$$

The real part of Z_{in} is given by:

$$R_e \left(Z_{\text{in}} \right) = r_g + \frac{g_m L_s}{C_{gs}}$$

where r_g is the gate resistance of MOS transistor. Neglecting the gate resistance, the real part of the input impedance can be expressed as:

$$R_e \left(Z_{\text{in}} \right) = \frac{g_m L_s}{C_{gs}} \tag{4}$$

For matching purpose, the real part of the input impedance should be equal to the source resistance. It is given by:

$$R_s = \frac{g_m L_s}{C_{gs}} = \varpi_T L_s \tag{5}$$

where ϖ_T is the unity-current gain angular frequency of the MOS transistor and can be approximated as [8]:

$$\varpi_T = \frac{g_m}{C_{gs} + C_{gd}} = \frac{g_m}{C_{gs}\sqrt{1 + \dfrac{C_{gd}}{C_{gs}}}} \cong \frac{g_m}{C_{gs}} = \frac{3}{2}\frac{\alpha \mu V_{ov}}{L^2} \tag{6}$$

The effective transconductance of the matched device of the LNA is defined as the ratio of the input transistor output current to the input voltage and given by:

$$G_m = \frac{I_d}{V_{in}} \tag{7}$$

In this case, $I_d = g_m \ V_{gs}$ & $V_{in} = V_{gs} / Q_{in}$, where $Q_{in} = 1/(\omega RC)$ is the quality factor of the input RLC tank which formed from the input matching network and it is given by:

$$Q_{\text{in}} = \frac{1}{\varpi \cdot R_s \cdot C_{gs}} = \frac{1}{\varpi \cdot g_m \cdot L_s} \tag{8}$$

and

$$\varpi = \frac{1}{\sqrt{C_{gs}\left(L_s + L_g \right)}} \tag{9}$$

Substituting (8) into (7), the input stage transconductance will be:

$$G_m = \frac{1}{\varpi \cdot L_s} \tag{10}$$

The LNA input stage transconductance given by (10) is independent on the actual input device transconductance g_m which considered a merit for LNA circuit.

At output, the output inductance (L_o) of the on-chip inductor is used to resonate with the cascode output capacitance at the resonance frequency. The disadvantage of the on-chip inductor is the series resistance and overlap capacitance between the turns of spiral and the cross-under layer. The series resistance of the spiral decreases the inductor quality factor which has a significant effect on the quality factor of the output tank. In this work, the series resistance is decreased significantly by using multilayer technique as we will discuss in next the sections and the overlap capacitance is used as the output capacitance for LNA circuit. So, on-chip spiral inductor becomes preferable compared to off-chip inductor.

At the resonance frequency, the voltage gain of the LNA shown in **Figure 1(a)** can be expressed as:

$$A_v = G_m \times Z_l(\varpi) \tag{11}$$

and

$$\begin{aligned} Z_l(\varpi) &= \left(Q_{ind} \times (\varpi L_o)\right) // R_{ot} // R_l \\ &= \left(\frac{(\varpi L_o)^2}{r_{s1}}\right) // R_{ot} // R_l \end{aligned} \tag{12}$$

where R_{ot} is the output resistance of the cascode architecture and R_l is the load resistance. Q_{ind} (ωL_o) is the output inductor parallel resistance. The output resistance is given by:

$$R_{ot} = g_{m2} \times r_{o1} \times r_{o2}$$

where g_{m2}, r_{o1} and r_{o2} are the transconductance of cascode transistor, and output resistance of input and cascode transistors, respectively.

If the load resistance value is small compared with the output resistance of the cascode and parallel resistance of the output inductor, the overall output resistance will be:

$$Z_l(\varpi) \equiv R_l$$

and

$$A_v = G_m \times R_l = \frac{R_l}{\varpi \times L_s} \tag{13}$$

The voltage gain of the low noise amplifier should be set to maximize the dynamic range of the total receiver. It can be accomplished if the next blocks are very linear but the noise will be increased and vice versa [8].

3. Modeling of Spiral Inductor

A lumped circuit model of on-chip spiral inductor grown on Si substrate is shown in **Figure 2** [9-11]. L_S and r_S are the series inductance and resistance of the spiral respectively. C_S is the overlap capacitance between the turns of spiral and the cross-under layer. C_{OX} is the oxide capacitance between the spiral and the substrate. R_{Si} and C_{Si} are the parameters modeling substrate losses and capacitive effects, respectively. The inductance of a spiral is a complex function of its geometry and includes both self and mutual inductances. The expressions for on-chip spiral inductor parameters are given by [9]:

$$\begin{aligned} L_s = \frac{\mu l}{2\pi}\Bigg\{ &\ln\frac{l}{2N(w+t)} + 0.5 + \frac{4N(w+t)}{3l} \quad -0.47N \\ &+ (N-1)\Bigg[\ln\left(\sqrt{1+\left(1/4Nd^+\right)^2} + \frac{l}{4Nd^+}\right) \\ &- \sqrt{1+\left(4Nd^+/l\right)^2} + \frac{4Nd^+}{l}\Bigg]\Bigg\} \end{aligned} \tag{14}$$

$$r_s(\omega) = \frac{l}{w \cdot \sigma \cdot \delta(\omega) \cdot \left(1 - e^{\frac{t}{\delta}}\right)} \tag{15}$$

$$C_{OX} = l \cdot w \frac{\varepsilon_{ox}}{t_{OX}} \tag{16}$$

$$C_s = N \cdot C_{OV} = N \cdot w^2 \cdot \frac{\varepsilon_{ox}}{d} \tag{17}$$

$$R_{Si} = \frac{2}{l \cdot w \cdot G_{\text{sub}}} \tag{18}$$

$$C_{Si} = \frac{l \cdot w \cdot C_{\text{sub}}}{2} \tag{19}$$

where l is the wire length, w is the width of the metal conductor, and t is the thickness of the metal conductor. The substrate parasitic capacitances and resistances cause

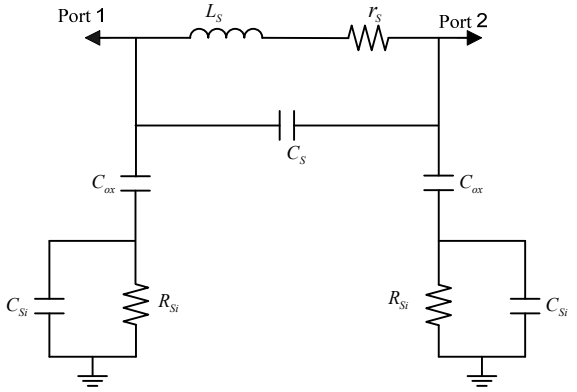

Figure 2. Lumped model of spiral inductor.

high losses in the circuit that present several challenges for implementing monolithic gigahertz circuitry. The placement of a patterned ground shield (PGS) beneath the spiral inductor eliminates the substrate parasites that improve the inductor performance [12]. A patterned ground shield is used in our calculations and simulations in this paper.

4. Noise Analysis

The noise figure of LNA at operation frequency ω can be estimated by analyzing the circuit shown in **Figure 3**. Five noise sources contribute the noise at the output of the low noise amplifier. The MOS transistor M_1 contributes by two of them. The noise sources are as follows:

1) the thermal noise of the channel current ($i_{n,d}$). It has a power spectral density of:

$$\frac{\overline{i_{n,d}^2}}{\Delta F} = 4K \cdot T \cdot \gamma \cdot g_{dso} \tag{20}$$

where K is the Boltzman constant, T is the absolute temperature, γ is the bias dependent constant, and g_{dso} is the drain-source conductance at $V_{ds} = 0$ and it is defined as:

$$g_{dso} = \frac{g_m}{\alpha}$$

where α equals 1 for long channel and 0.85 for short channel transistors.

2) The gate induced current noise ($i_{n,g}$): It has a power spectral density of:

$$\frac{\overline{i_{n,g}^2}}{\Delta F} = 4KT\delta g_g \tag{21}$$

and

$$\delta g_g = \frac{\varpi^2 C_{gs}^2}{5g_{dso}} = \frac{\alpha \varpi^2 C_{gs}^2}{5g_m}$$

Subsituting δg_g in (21) gives:

$$\frac{\overline{i_{n,g}^2}}{\Delta F} = 4KT\frac{\delta\alpha}{5g_m}\varpi^2 C_{gs}^2 = \frac{4KT\delta\alpha g_m}{5}\left(\frac{\varpi}{\varpi_T}\right)^2 \tag{22}$$

The gate current noise is related to the drain current noise and actually it is partially correlated to it with a correlation coefficient C given by:

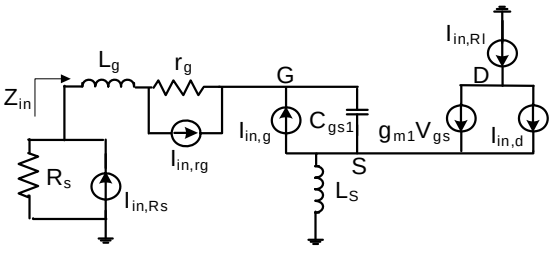

Figure 3. Circuit model for input stage noise analysis.

$$C = \frac{\overline{i_{n,g} i_{n,d}^*}}{\sqrt{i_{n,g}^2 i_{n,d}^2}} \tag{23}$$

where $C = j0.395$ for short channel transistors, and the power spectral density of the gate induced current noise source can be expressed as:

$$\frac{\overline{i_{n,g}^2}}{\Delta F} = \frac{\overline{i_{n,gc}^2}}{\Delta F} + \frac{\overline{i_{n,gu}^2}}{\Delta F}$$

or

$$\begin{aligned}\frac{\overline{i_{n,g}^2}}{\Delta F} &= \frac{4KT\delta\alpha g_m}{5}\left(\frac{\varpi}{\varpi_T}\right)^2 \left|C^2\right| \\ &+ \frac{4KT\delta\alpha g_m}{5}\left(\frac{\varpi}{\varpi_T}\right)^2 \left(1-\left|C^2\right|\right)\end{aligned} \tag{24}$$

The first term $i_{n,gc}$ is the correlated term and the second term $i_{n,gu}$ is the uncorrelated term.

3) The distributed gate resistance of CMOS transistor: It is also added noise to the output of the low noise amplifier and has a power spectral density equal to:

$$\frac{\overline{i_{n,rg}^2}}{\Delta F} = 4KTG_m^2 r_g = 4KT\frac{r_g}{\left(\varpi_T L_s\right)^2} \tag{25}$$

where r_g is distributed gate resistance given by:

$$r_g = 1/5g_m$$

where g_m is the input transistor transconductance.

4) The thermal noise due to source resistance: It has a power spectral density of:

$$\frac{\overline{i_{n,Rs}^2}}{\Delta F} = 4KTG_m^2 R_s \tag{26}$$

5) Thermal noise of the output resistance: The low noise amplifier utilizes an LC resonator circuit at the drain of the output transistor to adjust the output of the LNA at a desired resonance frequency ω. The losses of the LC resonant circuit result from output inductor series resistance R_d. The noise contribution of the series resistance in the LNA in the form of output noise current has a spectral density of:

$$\frac{\overline{i_{n,Rd}^2}}{\Delta F} = \frac{4KT}{R_d} \tag{27}$$

In this paper, using multilayer on-chip spiral inductor technique significantly decreases the value of the inductor series resistance that reduces the contribution of the spectral noise current due to inductor series resistance. Cascode transistor M_2 has a minor influence on the noise behavior of the LNA and its contribution to the total noise is disregarded in the analysis. Finally, the noise factor F is the ratio between the total output noise power

and the noise power due to the source resistance and it is give by:

$$F = 1 + \frac{r_g}{R_s} + \frac{\delta\alpha}{5} g_m R_s \left(\frac{\varpi}{\varpi_T}\right)^2 \left[|C|^2 \left(\frac{\varpi}{\varpi_T}\right)^2 + \left(1 - |C|^2\right)\left(\frac{\varpi}{\varpi_T}\right)^2 \right] + \frac{\gamma}{\alpha} g_m R_s \left(\frac{\varpi}{\varpi_T}\right)^2 + \frac{4R_s}{R_d}\left(\frac{\varpi}{\varpi_T}\right)^2 \quad (28)$$

The above equation describes the noise figure for low noise amplifier without taking the parasitic capacitance C_P effect into consideration. The parasitic capacitance C_P is the total parallel parasitic capacitance due to the ESD protection diodes, QFN package parasitic and bonding pad structure. The value of C_P is a fabrication dependency. If we include the parasitic capacitance effect on the noise figure, the noise factor will be:

$$F = 1 + \frac{r_g}{R_s} + \frac{\delta\alpha}{5} g_m R_s \left(\frac{\varpi\left(C_{gs} + C_p\right)}{g_m}\right)^2 \left[|C|^2 \left(\frac{\varpi}{\varpi_T}\right)^2 + \left(1 - |C|^2\right)\left(\frac{\varpi}{\varpi_T}\right)^2 \right] + \frac{\gamma}{\alpha} g_m R_s \left(\frac{\varpi}{\varpi_T}\right)^2 + \frac{4R_s}{R_d}\left(\frac{\varpi}{\varpi_T}\right)^2 \quad (29)$$

From the above equation, the noise figure of the LNA directly depends on the parallel parasitic capacitance C_P. With off-chip inductor, the value of C_P is very high because the parasitic capacitance dominates the input capacitance of the LNA which considers one of the biggest problems in the LNA design. Therefore, it is difficult to reduce the total noise figure. Our solution for this problem is to use on-chip spiral inductor as a gate inductor. In this case, the parasitic capacitance becomes non-dominat. So, any value for parasitic capacitance, high or low, do not highly effect on the noise figure and LNA gain. It also gives a good matching at input and output of the LNA without using any other matching components. Therefore, we can design a stable LNA circuit that gives the desired performance without taking into consideration C_P and other LNA complemented packaging.

There are many efforts for decreasing the effect of parasitic capacitance in noise figure as follow:

The first one considers a specific value for parasitic capacitance C_p and takes the parasitic capacitance as a part of the circuit and builds the design upon this idea [13] as follow:

$$\mathrm{Re}\left(Z_{in}\right) = R_s = \frac{g_m L_s C_{gs}}{\left(C_P + C_{gs}\right)^2} \quad (30)$$

From the above equation, increasing C_P increases the value of source inductor L_S and lowers the value of gate inductor L_g.

The second effort considers a specific value for C_P and uses matching network at the input [14] and the value of the matching capacitor is defined from:

$$\mathrm{Re}\left(Z_{in}\right) = R_s = \frac{1}{\left(\varpi * C_m\right)^2}\left(\frac{C_p + C_{gs}}{C_{gs}}\right)^2 \frac{1}{R_s} \quad (31)$$

and

$$L_g = \frac{C_p + C_{gs} + C_m}{C_m\left(C_p + C_{gs}\right)\varpi^2} \quad (32)$$

where C_m is the matching capacitor placed before gate inductor, C_p is parasitic capacitance, and ϖ is the resonance frequency.

5. LNA Stability

The stability of an amplifier is a very important factor which must not be susceptible to unwanted oscillation. The stability factor of an amplifier is a frequency dependent. The amplifier may be stable at its design frequency and unstable at other frequencies. It is highly recommended that the amplifier circuit is made unconditionally stable at all frequencies to ensure that it does not produce unwanted oscillations. For unconditionally stable, the input and output stable circuits should not be clipped the outer edge of the Smith chart. The stability of a two-port network can be determined from its *S*-parameters and the load and source impedances. The stability is determined by using Rollets factors K and Δ, where K and Δ in terms of *S*-parameters at frequency of operation is determined as follow [15]:

$$K = \frac{1 - S_{11}^2 - S_{22}^2 + \Delta^2}{2\left|S_{12}S_{21}\right|} \quad (33)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (34)$$

6. Results and Discussions

Cascode low noise amplifier with source degeneration technique shown in **Figure 1(a)** has been designed in 0.13 μm CMOS technology and simulated using ADS software. The value of the source resistance R_S = 50 Ω and the input transistor M_1 has W/L ratio of 44.73 μm/ 0.13 μm. It is biased at 1 mA and have a gate-source capacitance of 60 fF. The LNA is optimized at 15 GHz by the proper selection of the on-chip inductor parameters. The inductor has 5-levels, 4.75-turns, and squirrel shape that provides 1.08 nH inductance and its nonidealities series resistance of 2.5 Ω, overlap capacitance of 0.8 fF and the oxide capacitance between the spiral and the substrate of 21 fF with 2 μm width and 1 μm spacing between turns. It is designed to have a very small overlap capacitance and a series resistance to reduce the total LNA noise figure. The effect of the capacitance due to the ESD protection diodes, QFN package parasitic and bonding pad structure is taken in consideration during the

design of the LNA circuit. The cascade transistor M_2 is designed to have the same dimensions to decrease the power consumption at output. The output inductor L_o used to resonate with the output cascade capacitance and provide matching with the coupling capacitors C_1 and C_2 at the operating frequency f_o.

In our design, we use on-chip spiral inductor at the output and we include the inductor nonidealities to be part of the circuit. The inductor overlap capacitance is considered a part of the output capacitance and the inductor series resistance a part of the cascade output resistance. The value of L_o used in our simulation is 0.415 nH at an operating frequency of 15 GHz.

Table 1 gives the simulated results of the LNA performance using on-chip spiral inductor compared with off-chip inductor at different values of a parallel parasitic capacitance C_p. From the simulated results, with off-chip inductor, the noise figure (NF) highly increases with increasing C_P. Also, the power gain (A_p), input and output matching decrease to reach no matching when the parasitic capacitance is higher than the gate-source capacitance of input transistor M_1. Since, the parasitic value is undetermined and depends on the fabrication, the off-chip inductor is not effective in LNA design. The LNA with on-chip inductor has a higher power gain (A_p), higher voltage gain (A_v) compared with LNA with off-chip inductor. It also has lower noise figure and better input and output matching compared with LNA with off-chip inductor.

Table 2 gives the simulated results of LNA with different layers of on-chip inductor (N = 1, 3 and 5) with a parasitic capacitance of 120 fF. Increasing the number of the metal layers (N) decreases the inductor resistance, increases the power gain, improves the matching and reduces the noise figure. **Figures 4** and **5** show the variation of the LNA noise figure with the frequency for different layers of the on-chip inductor (N = 1, 3 and 5) at two different values of the parasitic capacitance C_p (C_p = 0 and 120 fF). As illustrated in the figures, increasing the number of the on-chip inductor layers reduces the LNA noise figure due to decrease the inductor resistance. **Figures 6-8** show the simulated LNA gain, input and output matching and noise figure using input matching capacitor and 5-layer on-chip spiral inductor. The results indicate that the maximum gain occurs at 15 GHz. The value of the power gain (A_P), input and output impedances matching (S_{11} and S_{22}), and noise figure are 11.087 dB, –17.93 dB, –10.04 dB, and 1.784 dB, respectively.

Figure 9 shows the stability factor K as a function of frequency. It is clear that K is greater than unity which means the system is stable. **Figures 10** and **11** show the LNA input and output stability circuits. The results illustrate that the LNA is unconditionally stable because the input and output circles locate inside the Smith Chart.

Table 1. Comparison between the simulated results of LNA performance with on-chip spiral and off-chip inductor.

Case	C_P fF	A_P (S_{21}) (dB)	A_V (dB)	S_{11} (dB)	S_{22} (dB)	S_{12} (dB)	NF_{min} (dB)	NF (dB)
Results with On-Chip Spiral Inductor								
1	60	11.119	5.09	–20.5	–10.0	–22.2	1.3	1.554
1	90	11.121	5.1	–20.7	–10.2	–22.5	1.3	1.658
3	120	11.087	5.067	–17.9	–10.4	–22.5	1.3	1.784
4	200	10.83	4.8	–11.4	–11.1	–22.8	1.3	2.218
Results with Off-Chip Inductor								
1	60	8.647	2.626	–3.54	–6.78	–24.5	1.229	1.7
2	90	7.064	1.044	–2.13	–6.11	–26.1	1.229	2.487
3	120	5.572	0.449	–1.39	–5.75	–27.57	1.229	3.474
4	200	2.272	–3.75	–0.6	–5.39	–30.9	1.229	6.241

Table 2. Simulated LNA performance with different layers of on-chip inductor.

N	r_S (Ω)	A_P (S_{21}) (dB)	A_V (dB)	S_{11} (dB)	S_{22} (dB)	S_{12} (dB)	NF_{min} (dB)	NF (dB)
1	12.6	10.01	3.986	–15.546	–9.656	–23.6	1.807	2.656
3	4.2	10.896	4.875	–17.908	–10.26	–22.7	1.401	1.942
5	2.5	11.087	5.067	–17.931	–10.4	–22.5	1.301	1.784

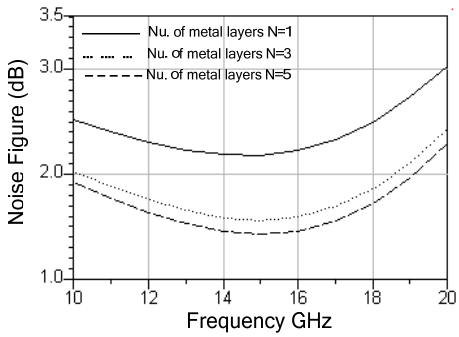

Figure 4. LNA noise figure versus frequency with different layers of on-chip inductor (N = 1, 2, and 3) for C_P = 0.

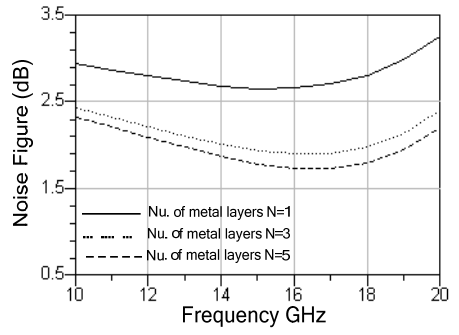

Figure 5. LNA noise figure versus frequency with different layers of on-chip inductor (N = 1, 3, and 5) for C_P = 120 pF.

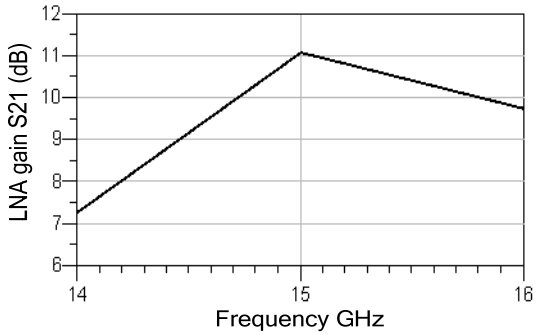

Figure 6. Simulated LNA output gain.

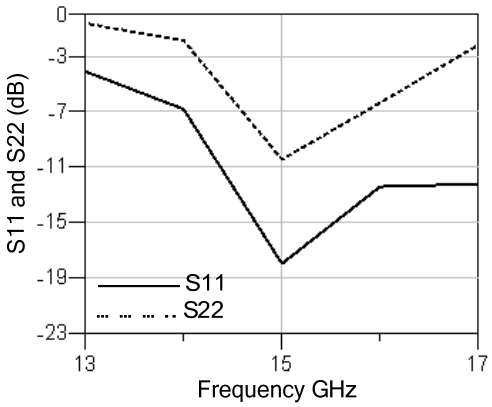

Figure 7. Simulated LNA input and output matching.

Figure 8. Simulated LNA noise figure.

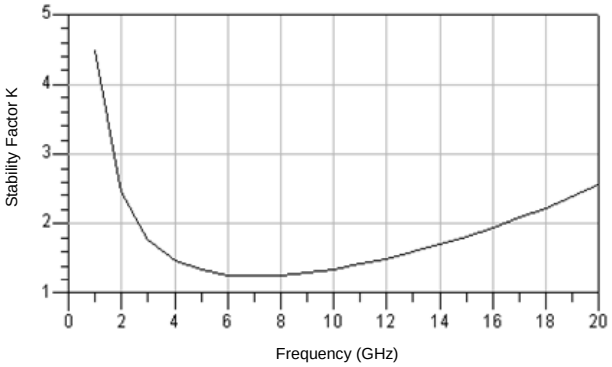

Figure 9. LNA Circuit Stability Factor *K* versus frequency.

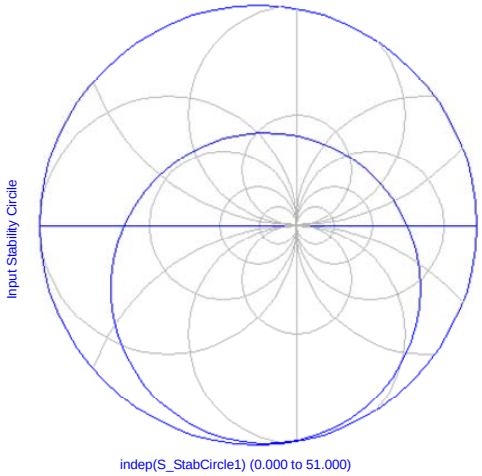

Figure 10. LNA input stability circle.

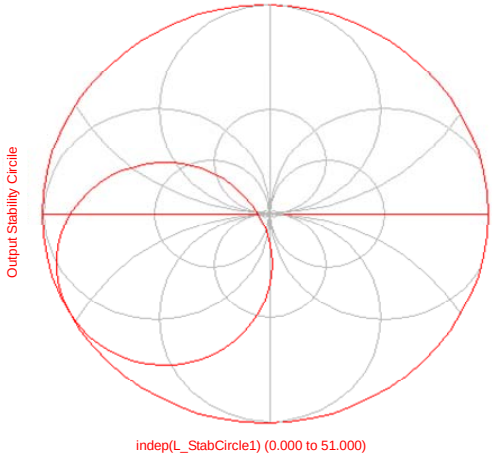

Figure 11. LNA output stability circle.

7. Conclusion

In this paper, a low noise amplifier has been designed using multilayer on-chip inductor to improve the LNA performance. Our results show that the suggested technique improves the noise figure and gives a better matching at the input and output of the LNA. Also, it gives a good power gain. Increasing the on-chip inductor metal layers reduces the spiral resistance and improves the noise figure. The results of our technique are compared with the results of the off-chip inductor technique that show our technique gives a better LNA performance.

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