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New Integrators and Differentiators Using a MMCC

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ABSTRACT

Using the new building block Multiplication-Mode Current Conveyor (MMCC), some inverting/non-inverting type integrator and differentiator designs are presented, wherein the time constant (τ) is tuned electronically. The MMCC is implemented by a readily available chip-level configuration using a multiplier (ICL 8013) and a current feedback amplifier (AD-844 IC) CFA. Detailed analysis, taking into account the device non-idealities, had been carried out that indicates slight deviations affecting the values of the nominal time constant but the design is practically insensitive to the port mismatch errors (ε). Satisfactory response on wave conversion, for signal frequencies up to 600 kHz had been verified with both hardware circuit test and PSPICE macromodel simulation.

Keywords: Voltage-Controlled Oscillator; Multiplication Mode Current Conveyor (MMCC); Current Feedback Opamp (CFA); Quadrature Oscillator

1. Introduction

Recently a new active building block named as the MMCC [1] is introduced; the element is quite attractive for analog signal conditioning and wave processing applications. Here we present the realization of some simple integrator and differentiator based on the MMCC wherein the time constant (τ) may be tuned electronically by a d.c. control voltage (V_c). The integrators/differentiators find numerous applications in signal processing and filter design [2,3].

The MMCC block here is implemented employing the readily available IC-chips, viz., the ICL-8013 multiplier [4] and a AD-844 CFA [5-7]. Electronic τ-tuning is done by varying V_c of the multiplier and by changing the polarity of V_c, an inverting or non-inverting response may be obtained.

The ICL-8013 device is a four-quadrant analog multiplier whose output is proportional to the electronic product of two input voltage signals with a transmission constant k·volt^{-1} [4]. The high accuracy (±1%), relatively wide bandwidth (B = 1 MHz) ad improved versatility make it quite suitable for analog signal conditioning and wave processing applications.

The quality factor (Q) of the circuits is shown to be practically active-insensitive relative to the device port errors (ε) of the multiplier and CFA elements. At relatively higher frequencies, the shunt-RC trans-impedance components across the z-node of the CFA device cause some phase deviations which alter the Q-values slightly; these effects had also been examined. The proposed designs have been tested in time-domain for wave conversion applications up to a signal frequency of 600 KHz and satisfactory response are verified by both hardware test and PSPICE simulation. The Q-value indicates a measure of the idealness of the phase properties of integrator/differentiator in frequency domain. The device non-idealities produce very insignificant effects on these phase properties; hence active-insensitive.

2. Analysis

The MMCC block and its proposed device implementation are shown in **Figures 1(a)** and **(b)**; the nodal equations [1] are $V_x = kV_{y1}V_{y2}$, $I_z = I_x$ and $I_{y1} = 0 = I_{y2}$. In the proposed configuration, the control voltage V_c is used at terminal y_2 with k as the multiplication constant in volt^{-1} wherein the nominal input stimulus V_i is applied to terminal y_1. We could devise either polarity MMCC by changing the sign of (V_c) so as to obtain both inverting/non-inverting functions. The CFA nodal relations are $I_z = aI_x$, $V_x = bV_y$, $V_0 = \delta V_z$ and $I_y = 0$; We thus have design convenience with this implementation that provides an additional voltage source output V_0, which is not usually available with the conventional current conveyor [8] along with the current source output (I_z). The CFA port tracking ratios are postulated in the literature [3,9] in terms of finite but small errors $(|\varepsilon| \ll 1)$ as $a = 1-\varepsilon_i$, $b = 1-\varepsilon_y$ and $\delta = 1-\varepsilon_0$; the error vanish $(\varepsilon = 0)$ for an ideal element,

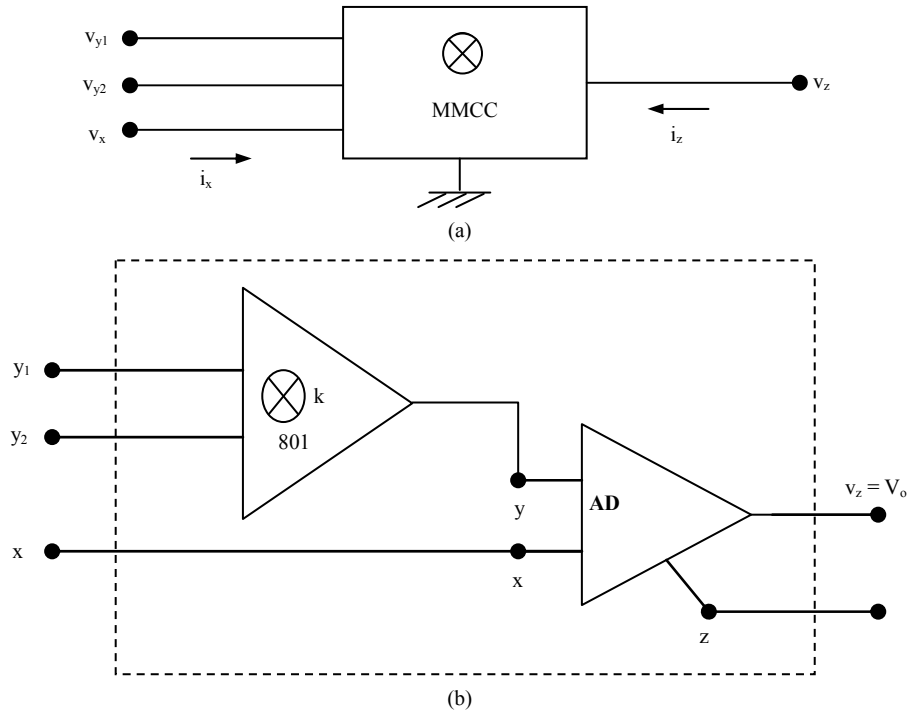

Figure 1. The MMCC building block (a) MMCC with nodal relations; (b) MMCC implementation with commercially available chips.

hence we get in **Figure 1(b)**.

$$V_y = kV_{y1}V_c \tag{1}$$

$$V_x = V_y;\ \ I_z = I_x \tag{2}$$

and

$$V_0 = V_z \tag{3}$$

with $\pm V_c$ one gets a $\pm$MMCC.

The proposed integrator/differentiator are obtained after realizing a ratio type (Z_2/Z_1) function as shown in **Figures 2(a)** and **(b)** after incorporating the RC-components in the building block appropriately so that we could implement design within the single MMCC configuration; analysis by Equations (1) to (3) yields in **Figure 2**.

$$G(s) = V_0/V_i = \pm\ kV_c\, Z_2/Z_1 \tag{4}$$

where $V_{y1} = V_i$ is used as input signal and $V_{y2} = V_c$ is control voltage and $Z_{1,2}$ are passive one-port RC impedances. For **Figure 2(a)** the transfer is non-inverting with positive sign and for **Figure 2(b)** it is inverting. We select $Z_2 = 1/sC$ and $Z_1 = R$, for an ideal integrator so that

$$G_i(s) = \pm 1/s\tau_i;\ \ \tau_i = RC/kV_c \tag{5}$$

Interchanging the components we get the ideal differentiator

$$G_d(s) = \pm s\tau_d;\ \ \tau_d = kV_cRC \tag{6}$$

Thus for a given RC product, $\tau_{i,d}$ are electronically tunable by V_c.

3. Effect of Non-Ideality

The design imperfections of the proposed circuits may be examined in terms of two types device non-idealities, viz., first with respect to parasitic time constant components appearing in shunt at the current source output node-z (r_zC_z) of the AD-844 current amplifier. Effect of these transimpedance components becomes dominant at relatively higher frequency operation of the integrator/differentiator while the parasitic capacitance (C_Z) affects the quality factor (Q) due to its excess phase. Analyses show that some upper and lower bounds in the operating frequency ranges of the integrator/differentiator are introduced by the parasitic components, albeit this effect could be minimized with suitable design. The second non-ideality is with respect to the finite device port mismatch errors $(\varepsilon \neq 0)$ which slightly alters the values of the nominal time constant $(\tau_{i,d})$. As per datasheet [5] $r_z \approx 5$ MΩ and 3 pF $\leq C_z \leq$ 6 pF. In the proposed designs we selected $R \ll r_z$ and usually $C_z \ll C$. Also we expressed $k \approx (1-\varepsilon_m)$ volt^{-1} so that we can essentially write $kV_c = (1-\varepsilon_m)$ for sensitivity calculation. First we derive the nonideal effects owing to the shunt transimpedance components. The transfer functions for **Figure 2(a)** then modify to

$$G_i'(s) = 1/(s\tau_i' + \lambda) \tag{7}$$

and $$G'_d(s) = s\tau'_d/(s\tau_z + p + 1) \quad (8)$$

where $$\tau'_i = (1+n)\tau_i \quad (9)$$

$$p = R/r_z \ll 1;\ \ n = C_z/C \ll 1;\ \ \lambda = p/kV_c;\ \ \tau_z = RC_z \quad (10)$$

Table 1 shows the details of the proposed realizations and the corresponding effects of non-ideality due to the device transimpedance components for both **Figures 2(a)** and **(b)**; here ω_c is the lower bound corner frequency of integrator and ω_z is the upper bound cut-off frequency of differentiator. Above ω_c corner frequency the integrator becomes practically ideal, and below ω_z cut-off frequency the differentiator becomes practically ideal. For example if $r_z \approx 5\ \Omega$, $C \approx 15$ pF, $C_z \approx 5.5$ pF and $R \approx 3$ KΩ, one gets $f_c \approx 2$ kHz and $f_z \approx 10$ MHz.

The port mismatch errors modify the nominal values given by

$$\tau_i = RC/kV_c(ab\delta),\ \ f_c \approx kV_c\, RC/(a\delta) \quad (11)$$

which yields the active sensitivity figures as

$$\tau_i,\ \ \tau_d,\ \ S \approx -\varepsilon/(1-\varepsilon_T) \ll 1;\ \ S \approx \varepsilon/(1-\varepsilon_t) \ll 1$$

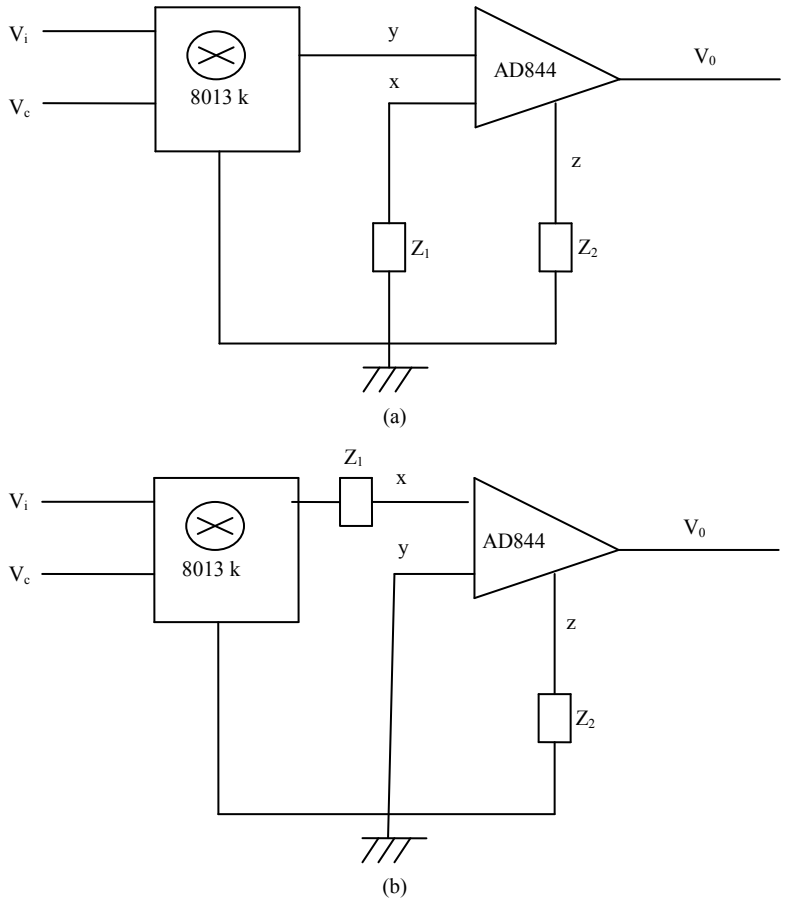

Figure 2. Integrator/differentiator design (a) Non-inverting ratio function realization $V_0/V_1 = kV_cZ_2/Z_1$; (b) Inverting ration function realization.

Table 1. Effects of transimpedance non-ideality for Figures 2(a) and (b).

Function	Component Selection	Ideal Transfer	Non-Ideal Transfer	Quality Factor (Q)
Integrator	$Z_1 = R$ $Z_2 = 1/sC$	$G_i = \pm 1/s\tau_i$ $\tau_i = RC/kV_c$	$G'_i = \pm 1/(s\tau'_i + \lambda)$	$Q_i \approx \omega/\omega_c$, $\omega_c = 1/r_zC$, $Q_i \gg 1$ for $\omega \gg \omega_c$
Differentiator	$Z_1 = 1/sC$ $Z_2 = R$	$G_d = \pm s\tau_d$ $\tau_d = kV_cRC$	$G'_d = \pm s\tau_d/(s\tau_z + p + 1)$, $\tau_z = C_zR$	$Q_d \approx \omega_z/\omega$, $\omega_z = (1+p)/\tau_z$, $Q_d \gg 1$ for $\omega \ll \omega_z$

Transfer G has (+) sign for **Figure 2(a)** and (–) sign for **(b)**.

Table 2. Summary on performance of some recent oscillators.

Ref.	Electronic tunability	Quadrature property	f_o (KHz) tuning range reported	S_f	THD (%)
[11]	No	Yes	20	$\approx 2n(1-\varepsilon)=2n$	2.50
[12]	Yes	No	145	NI	NI
[13]	No	Yes	986	NI	NI
[14]	No	Yes	15.8	NI	2.47
[15]	Yes	No	73	$2\sqrt{n}/(1-n)$	1.52 - 1.88
Proposed	Yes	Yes	600	$n\sqrt{(1-\varepsilon_T)} \approx n \equiv r_z/R \gg 1$ (assuming equal-value resistors)	1.11

NI: Not indicated.

where $\varepsilon_T \approx \varepsilon_i + \varepsilon_v + \varepsilon_0 + \varepsilon_m$ and $\varepsilon_t \approx \varepsilon_i + \varepsilon_0 + \varepsilon_m$. It may be shown similarly that the active-Q sensitivities are also extremely low.

4. Quadrature Linear VCO Design

We next present the design of a MMCC based Dual Integrator Loop (DIL) sinusoid oscillator (involving one non-inverting and the other inverting type). The feature of four quadrant operation of the multiplier device is utilized here for realizing the opposite polarity ideal integrators by using a bipolar d.c. control voltage ($\pm V_c$). A linear f_o-tuning law in a range of 40 KHz $\le f_o \le$ 600 KHz with satisfactory quadrature signal generation had been measured both by PSPICE macromodel simulation [9] and with hardware circuit implementation. The oscillation frequency is $f_o = kV_c/2\pi\sqrt{(\tau_{i1}\tau_{i2})}$ where τ_{i1} and τ_{i2} denote time constants of the two MMCC-based integrators in loop. The frequency stability factor (S_f) of a sinusoid oscillator is defined as $S_f = (\Delta\theta/\Delta u)\big|_{u=1}$ where $u = f/f_o$ and θ is the loop phase shift. We evaluated the value of S_f after assuming finite trans-admittance parameters, given by $S_f = (2r_{zp})\sqrt{(1-\varepsilon_T)/R_1R_2}$ where r_{zp} is the shunt equivalent $\{1/r_{zp} = (1/r_{z1}) + (1/r_{z2})\}$ of the r_z components for the two integrator stages. The stability is quite satisfactory $S_f \gg 1$ since $r_{z1,2} \gg R_{1,2}$. Here both capacitors are grounded [10] and the parasitic capacitances C_z have an additive effect $(C + C_z)$; but since value of C is chosen such that $(C \gg C_z)$ the resulting deviation would be insignificant, or alternatively, the effect of C_z may be pre-absorbed in value of C.

Analysis on the effects of device port mismatch errors (ε) indicate that f_o is practically active insensitive and the effects of the shunt parasitic components of the CFA-device are negligible. The frequency stability (S_f) factor of the proposed oscillator is quite high $(S_f \gg 1)$ at low values of measured THD (≈1.1%). Integrators/differentiators are useful as filters, phase compensators and delay measuring blocks; double integrator loops are useful as quadrature signal generators which had been proposed here with linear electronic tuning properties.

5. Experimental Results

The proposed circuits were tested for wave conversion application by both hardware test and PSPICE simulation. Some simulation results for square wave to triangular wave conversion by integrator and vice versa for the differentiator are shown in **Figure 3** with inverting/non-inverting polarity. The multiplier constant is set to k = 0.5/volt and the passive components are suitably chosen for the measurement in a frequency range of 50 KHz ≤ f ≤ 600 KHz. Both PSPICE simulation and hardware circuit tests were carried out using AD-844 CFAS Op-amp and ICL 8013 multiplier device; additionally AD-534 multiplier element had also been used to verify the results.

With hardware circuit test, however, a deviation of 2% - 5% in the response had been observed; this may be due to the inter-lead stray capacitance between the chip terminal and the breadboard pin. With sinusoid excitation, the desired phase shift of ±π/2 had been verified and a phase error of less than 1˚ had been measured at 900 KHz; expected 6 db/octave attenuation for the integrator and accentuation for the difference in magnitude response had also been measured. It may be mentioned that that the operating range of the circuits concomitant to the bandwidth (=1 MHz) of the ICL-8013 device; embedding the HA 2557 multiplier device [4] with bandwidth equal to 130 MHz is expected to yield an extended frequency range. The error analysis has been carried out here following the model of non-idealities and their subsequent effects on the nominal design as per the relevant recent literature survey cited in **Table 2** [11-15].

6. Conclusion

Some new inverting/non-inverting voltage tunable inte-

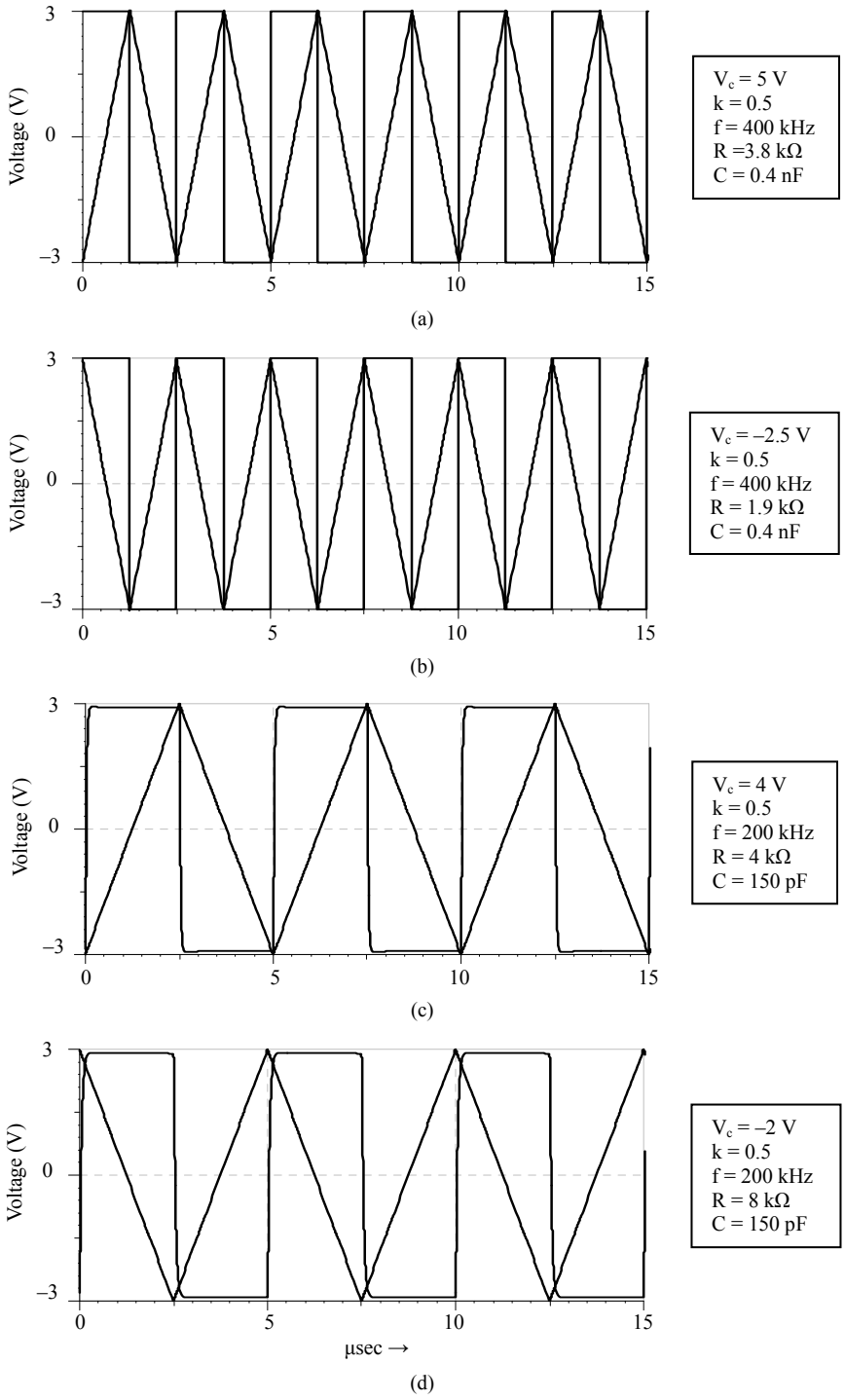

Figure 3. Response of integrator/differentiator, (a) Integrator; (b) Integrator; (c) Differentiator; (d) Differentiator.

grator and differentiator realizations are presented using the recent MMCC device. The chip level design implementation is done by the readily available elements, viz., the ICL-8013 or AD-534 four-quadrant multiplier and the AD-844 CFA unity-gain current amplifier. The quality factor (Q) of the circuits is practically active—insensitive. Satisfactory response had been measured in a range of 50 kHz ≤ f ≤ 600 kHz with suitable design. Measured phase error is less than 1˚ at 900 kHz. Application to wave conversion had been verified for both the integrator and differentiator function while electronic tuning of $\tau_{i,d}$ with respect to control voltage is obtained satisfactorily. Subsequently a double-integrator loop sine wave quadrature oscillator had been designed and its

electronic tuning property is tested in a range of 40 KHz $\leq f_o \leq$ 600 KHz. Experimental results are shown in **Figure 4**. The MMCC is a recently proposed active building block; its application to the design of such integrator/differentiator and linear quadrature VCO had not yet been reported. The VCO is a useful element for PLL or FM discriminator design. The authors are now carrying out further work to extend the functionality of the VCO so as to implement a digitally programmable oscillator wherein a digital code (e.g. BCD word), after being con-

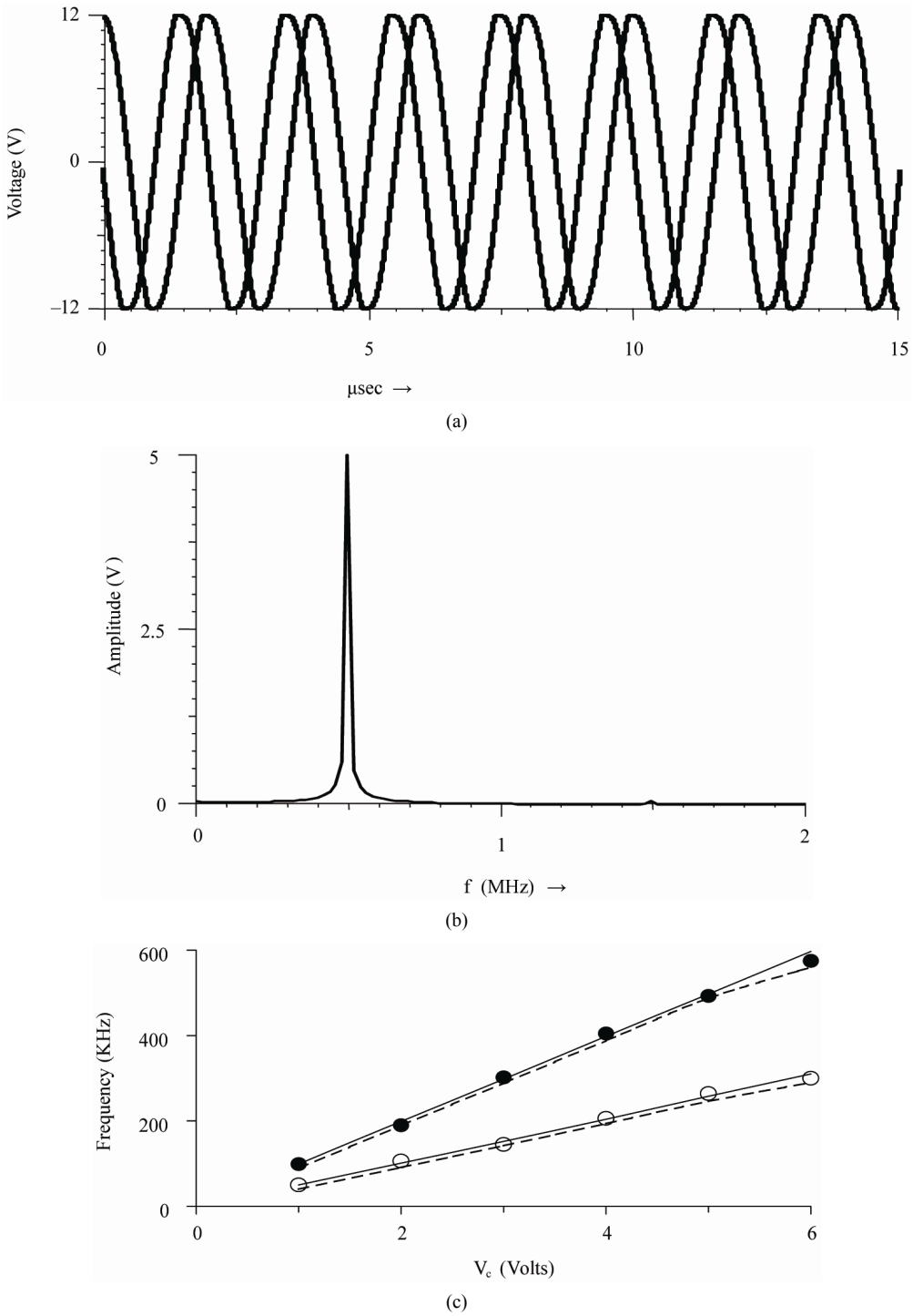

Figure 4. Response of dual-integrator loop quadrature oscillator: (a) Simulated response at f_o = 500 KHz with k = 0.1/volt and V_c = 5 V.d.c.; (b) Spectrum of the generated signal; (c) Linear tuning characteristics with C = 160 pF:R = 1 KΩ (●); R = 2 KΩ (○) (dotted line by hardware test).

verted by a D to A Converter (DAC), would be able to tune and generate a sequence of frequencies leading to FSK/PSK type modulation signal.

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