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Power Conversion Enhancement of CdS/CdTe Solar Cell Interconnected with Tunnel Diode

Wagah F. Mohammed, Omar Daoud, Munther Al-Tikriti
Communications and Electronics Department, Faculty of Engineering, Philadelphia University, Amman, Jordan
Email: {wagahfaljubori, oamr1462004}@yahoo.com, munther_baker44@yahoo.co.uk

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ABSTRACT

One of the most promising solar cell devices is cadmium telluride (CdTe) based. These cells however, have their own problems of stability and degradation in efficiency. Measurements show that CdS/CdTe solar cell has high series resistance which degrades the performance of solar cell energy conversion. Both active layers (CdS and CdTe) had been fabricated by thermal evaporation and tested individually. It was found that CdS window layer of 300 nm have the lowest series resistance with maximum light absorption. While 5 - 7 μm CdTe absorber layer absorbed more than 90% of the incident light with minimum series resistance. A complete CdS/CdTe solar cell was fabricated and tested. It was found that deposited cell without heat treatment shows that the short circuit current increment decreases as the light intensity increases. This type of deposited cell has low conversion efficiency. The energy conversion efficiency was improved by heat treatment, depositing heavily doped layer at the back of the cell and minimizing the contact resistivity by depositing material with resistivity less than 1 $m\Omega \cdot cm^2$. All these modifications were not enough because the back contact is non-ohmic. Tunnel diode of CdTe (p++)/CdS (n++) was deposited in the back of the cell. The energy conversion efficiency was improved by more than 7%.

Keywords: CdS/CdTe; Solar Cells; Energy Conversion; Efficiency

1. Introduction

Silicon-based solar cells are currently the most successful commercial photovoltaic product. The PV market, dominated by crystalline silicon, has grown on average more than twenty percent per year but faces the problem of profitability as it must compete with traditional sources and methods of energy conversion. To become competitive, PV materials are needed as they are much less expensive than single crystal silicon and are compatible with large scale manufacturing. Thin film materials and manufacturing processes are an obvious choice for lowering the cost. Thin film solar cells based on polycrystalline Cadmium Telluride (CdTe) reached record efficiencies of 16.5% [1] for laboratory scale device and of 10.9% for terrestrial module [2]. Since the record efficiency of such type solar cells is considerably lower than the theoretical limit of 28% - 30% [3], the performance of the modules can be improved, through new advances in fundamental material science and engineering, and device processing. CdTe is one of the most suitable materials for photovoltaic applications. CdTe has a direct band gap material ($E_g \approx 1.5$ eV at room temperature) with a high absorption coefficient (above 10^5 cm^{-1} at the wavelength of 700 nm). Few microns thick layer of CdTe absorbs more than 90% of the incident light with the photon energy higher than the band gap. The maximum theoretical efficiency corresponding to such band gap is about 27%. The small thickness required for an absorbing layer makes the cost of material for the solar cells relatively low. To date, CdTe has been deposited successfully by a variety of techniques [4].

CaCadmium sulfide (CdS) belonging to the II-VI group is one of the promising materials for optoelectronic devices. CdS has been the subject of intensive research because of its intermediate band gap ($E_g \approx 2.42$ eV) making the material suitable as window material for a heterojunction solar cell [5], high absorption coefficient, reasonable conversion efficiency, stability and low cost [6]. Knowledge of the optical properties of CdS films is very important in the field of optoelectronic devices like photo-detectors and solar cells. A broad variety of deposition techniques can be used to fabricate CdS films with desirable optical properties [7]. Although CdTe can be doped both p-type and n-type CdTe: homojunction cells have not shown very high efficiency. Due to high absorption coefficient and small diffusion length, the junction must be formed close to the surface, which reduces the carrier lifetime through surface recombination. The In-doped CdTe (p) thin film is of high bulk resistivity

which largely affects its photovoltaic properties particularly the short circuit current [8]. It was noted that, the deteriorative effect of the high bulk resistivity increases by increasing the light intensity, which in turn limits the benefit of using light concentrators that improve the short circuit current.

Heterojunctions which consist of CdTe as one of the junction sides had been under investigation for many years [9]. The electrical properties of post-deposition annealed and as-deposited In-doped CdTe thin films were studied in details [10]. It was observed that the CdTe film was of modified Poole-Frenkel conduction mechanism and the resistivity of the film could be lowered by more than one order of magnitude due to indium doping. Also, considerable amount of work had been paid to develop the CdS/CdTe solar cells over the last twenty years [11]. Also the electrical, photoelectrical, and structural properties of CdS/CdTe heterostruture were studied [12]. Deposition of thin polycrystalline CdTe layers on the top of the CdS layer for solar cells has been successfully performed by using various methods. Considerably higher efficiencies were obtained by using n-CdS/p-CdTe heterojunctions. The CdS layer serves as a window layer and helps to reduce the interface recombination. Without special doping the CdS film has significantly higher carrier concentration ($\approx 10^{16}$ - 10^{17} cm^{-3}) than the CdTe adjacent to the interface ($\approx 10^{14}$ - 10^{15} cm^{-3}). As a result the built-in potential is applied mostly to the CdTe absorber layer, providing effective separation of the photo generated carriers. High efficiency solar cells of efficiencies up to 12.5% were developed with a CdTe low temperature (<450˚C) process [13]. Efficient solar cell performance requires minimizing the forward recombination current and maximizing the light generated current. Collection losses can be minimized in thin film of high absorption and short diffusion length. Voltage dependent photocurrent collection losses in CdTe films were observed [14]. The voltage dependence of photocurrent of CdTe/CdS solar cells was characterized by separating the forward current from the photocurrent. Recently, preparation and performance of CdS/CdTe tandem solar cells is introduced [15,16]. Thinner layers at the top and thicker ones at the bottom managed to increase the open circuit voltage and improve the spectral response.

2. Laboratory Preparations and Solar Cell Structure

Cadmium Sulphide/Cadmium telluride (CdS/CdTe) solar cell is composed of four main layers deposited on a glass substrate. A transparent conducting oxide deposited directly on top of the glass to form the front contact. The second layer is the window layer, which is usually n-type semiconductor. CdS, with band gap of 2.4 eV at room temperature, is the most suitable material for CdTe-based solar cells. The work of [17-19] showed that without special doping, the CdS films have significantly higher carrier concentration than the CdTe. The third layer is the absorber layer of CdTe, which is usually from 5 - 10 μm thick film. The deposition parameters, optical and electrical properties of active layers will be discussed deeply later. Finally, the fourth step in the solar cell fabrication is the application of the back electrical contact to the CdTe layer. 2 μm Aluminum is used as metal back contact. It was recognized that this step is critical for CdS/CdTe solar cell performance due to low stability and resulted in a high contact resistance. In order to minimize this resistance (ρ_C < 1 mΩ·cm) tunnel diode is proposed to be connected in series with the solar cell [20]. These problems will be the main issues in this work and they will be addressed later.

Fabrication of CdS films of thickness up to 800 nm was carried out on a glass substrate using Balzer vacuum thermal evaporation system. The substrate temperature, vacuum pressure, deposition rate, film thickness and annealing temperature have been measured by the system. CdS film was evaporated at optimum evaporation parameters [18], under 10^{-6} mbar vacuum. The substrate temperature was 300˚C and the deposition rate is 2˚ A/sec. Thickness of the layer and annealing temperature are varied to obtain maximum grain size at minimum thickness with very low resistivity. Few samples of CdTe thin film were prepared by thermal evaporation and deposited on glass substrate to be examined individually. A comprehensive study of CdTe layer in CdS/CdTe solar cell had been conducted [21], and the main parameters of CdTe material that affect the module efficiency had been discussed. Among these parameters are the lifetime, diffusion length, drift length of minority carriers and thickness of CdTe absorber layer. In this research; it is found that 7 μm of CdTe thickness deposited with 8˚ A/sec. rate of deposition on substrate with 100˚C temperature is optimum for maximum absorption of radiation and produces large enough grain size [10]. The annealing temperature is varied for optimum optical and electrical properties of the film.

3. Optical and Electrical Properties of the Solar Cell Layers

Transmission and absorption coefficient spectrum have been carried out for each individual layer at different annealing temperature. **Figures 1** and **2** shows the transmission and absorption coefficients of CdS and CdTe layers respectively. CdS film exhibited high degree of transmittance in the infrared region and showed sharp falling of the absorption edge towards lower wavelength. The absorption edge is lowered as the annealing tem-

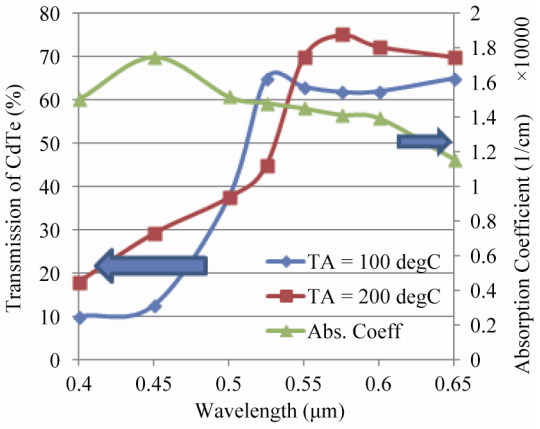


Figure 1. Transmittance and absorption coefficients of CdS layer at different annealing temperatures.

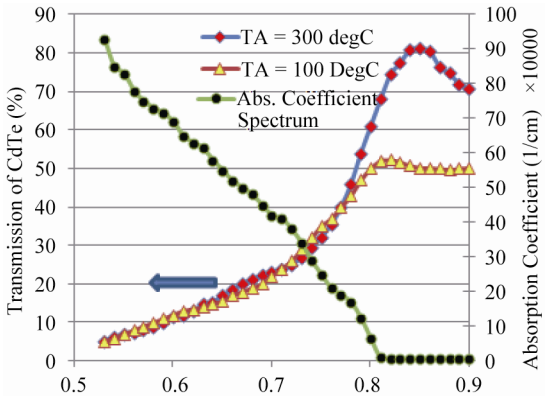


Figure 2. Transmittance and absorption coefficients of CdTe layer at different annealing temperatures.

perature of the film increased. It was found that small changes in the thickness of CdS had a greater influence on transmission. It must, however, be emphasized that more reduction of CdS will increase the resistivity of the layer which will deteriorate the electrical properties of the layer. Thicker CdTe layer is used in order that all light is absorbed in this layer. CdTe film exhibits transmittance at short wavelength ($\lambda \approx 500$ nm). The transmittance becomes more pronounced at wavelength higher than 800 nm. The absorption edge shifted toward lower wavelength at high annealing temperature (250˚C).

Figures 3 and **4** show that the variation of resistivity and photo generated current of CdS and CdTe layers with wavelength at different annealing temperatures. It is clear that CdS sample annealed at 250˚C gave minimum resistivity and of course maximum photo generated current. This is because that the absorption coefficient for this sample is very high which is inversely proportional to resistivity. The material becomes more n-type due to excessive Cadmium under layer and enhanced diffusion at grain boundaries or impurities incorporated in the deposit [7].

4. The Effect of Series Resistance

Figure 5(a) represents a schematic representation of the CdS/CdTe solar cell heterostructure. The layers succession and thicknesses are the one used in the present work. An electronic solar cell model can be considered, as shown in **Figure 5(b)**, taking into account the effect of the series resistance (R_s) and shunt resistance (R_{sh}). The solar cell current source generates a light current (I_{PH}) which is directly proportional to the solar illumination. The two resistors (R_{sh}) and (R_s) represent the losses incurred in the solar cell. The series resistor (R_s) caused by the ohmic losses in the surface of the solar cell. The par-

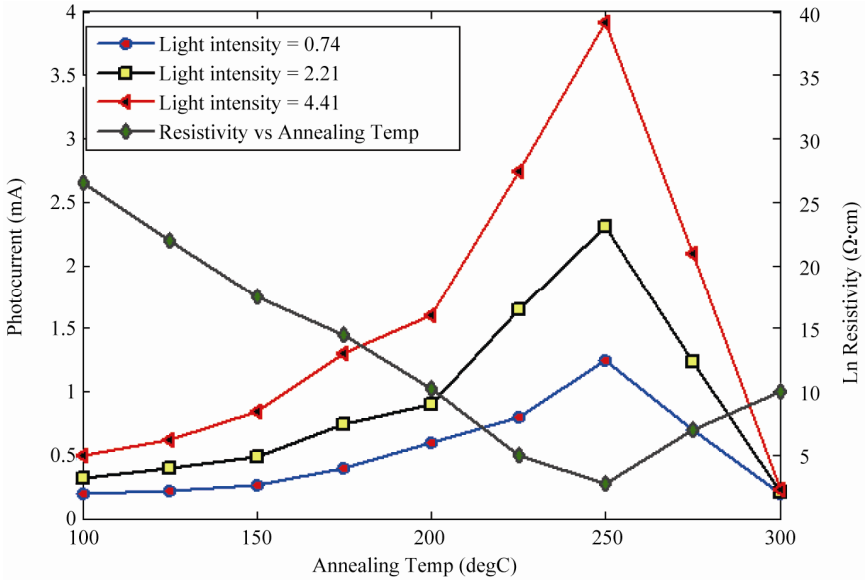


Figure 3. Variation of resistivity and photo generated current with annealing temperature for CdS layer.

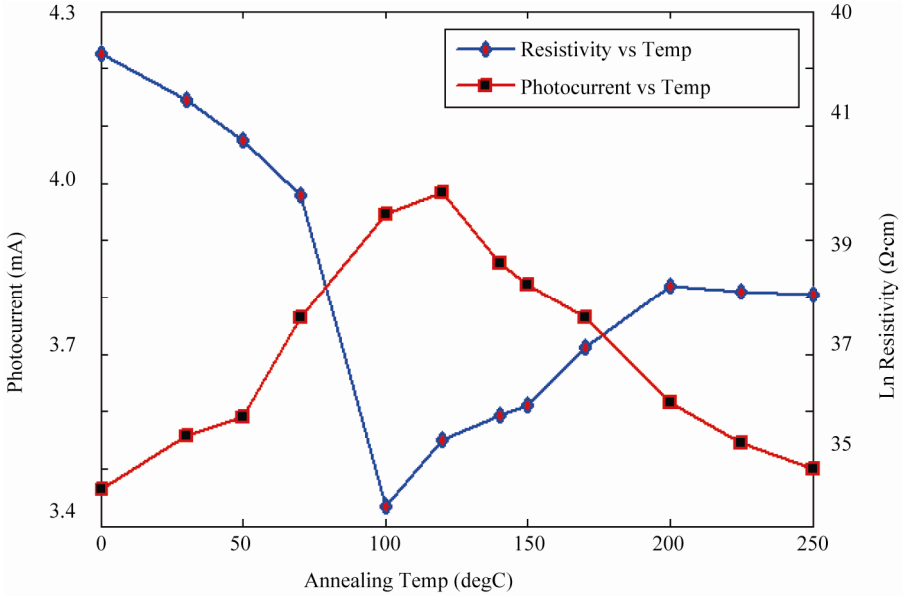
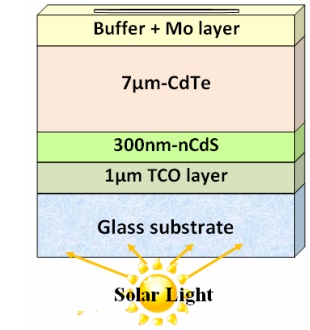
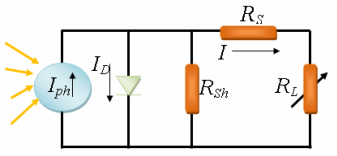


Figure 4. Variation of resistivity and photo generated current with annealing temperature for CdTe layer.



(a)



(b)

Figure 5. (a) Schematic representation of the CdS/CdTe solar cell heterostructure; (b) Electronic solar cell model.

allel shunt resistor (R_{sh}) denotes the losses due to leakage current in the solar cell.

Taking into account the effect of the series resistance (R_s) and shunt resistance (R_{sh}), the current supplied to the load (I) can be expressed as:

$$I = I_{ph} - I_o\left(e^{\left(\frac{V}{nV_T}\right)} - 1\right) - \left(\frac{V + IR_s}{R_{sh}}\right) \qquad (1)$$

where I_{ph} is the photo generated current, I_o is the saturation current, V is the applied voltage, n is the identity factor and V_T is thermal voltage which is equal to 26 mV at room temperature. The saturation current is measured to be equal to 2 µA. The series resistance is determined as [22].

$$R_{oc} = \left.\frac{dV}{dj_{sc}}\right|_{V=V_{oc}} = R_s\left[1 + \frac{R_o}{R_s} + \frac{R_o}{R_{sh}}\right]\left[1 + \frac{R_o}{R_{sh}}\right]^{-1} \qquad (2)$$

where R_{oc} is the open circuit series resistance and $R_o = [nkT/q \cdot J_{sc}]$. Usually for CdTe based cells, $J_{sc} \approx 20$ mA/cm^2 and n = 2 [8], hence $R_o \approx 2.5$ Ω at room temperature. R_{sh} is usually of order of few several hundred Ohms which means $R_o/R_{sh} \ll 1$ leads to an approximate relation: $R_s \approx R_{oc} - R_o$. Hence the calculated range of series resistance is 5 - 10 Ω. I-V characteristics of CdS/CdTe show that the device has high series resistance [8]. The real value of measured series resistance is higher than the calculated one due to the parasitic resistance connected in series to the main cell. **Figure 6** shows the variation of the short circuit current with the light intensity measured practically. It can be seen that the short circuit current

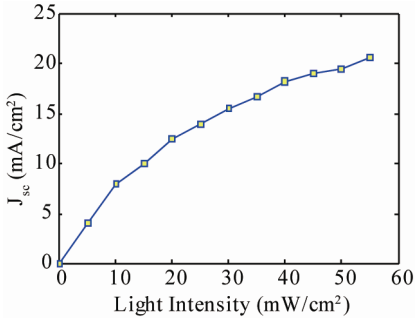


Figure 6. Variation of short circuit current density with light intensity.

varies rapidly at low intensity (<5 mW) while it saturates at high intensity. It can be suggested that this degradation in the cell performance at high light intensities is due to the high series resistance.

The solar cell model given by Equation (1) is simulated using MATLAB. The photo generated current density is measured using the following equation [8]:

$$J_{ph} = q\int F(\lambda)\left[1-R(\lambda)\right]\left[1-e^{-\alpha d}\right]\eta(\lambda)\cdot\partial\lambda \qquad (3)$$

q is the electron charge, F is the number of incident photons with energies greater than the band energy in $[cm^{-2}\cdot s^{-1}]$, R is the reflection coefficient, α is the absorption coefficient (cm^{-1}), d is the cell thickness which is nearly equal to CdTe, and η is the collection efficiency which varies from 0 - 1. The limits of integration are from 0.48 - 0.87 μm; out of this range the absorption process can be ignored. The reflection coefficient varies from 0.7 - 0.9 for the wavelength mentioned above. The absorption coefficient can be deduced from **Figure 2**, which is approximately equals to 1.3×10^7 cm^{-1}. **Figure 7** shows that the simulation result and practical measurements of short circuit current versus photo generated current at different values of series resistance with shunt resistance is 10 KΩ. The results given in **Figure 8** were calculated at high light intensity (high photo generated currents) which in turn means high short circuit current.

Mathematical manipulation of Equation (1) at short circuit current condition when the voltage across the load resistance becomes zero yields:

$$\frac{dI_{sc}}{dI_{ph}} = \left[\left(\frac{I_o R_s}{nV_T}\right)e^{\left(\frac{I_{sc}R_s}{nV_T}\right)}\right]^{-1} \qquad (4)$$

It can be seen that the slope varies inversely with R_s that means the variation of I_{sc} will be less as the I_{ph} increases due to the high effect of R_s. That is evidently shown in **Figure 7**, when R_s becomes zero the slope $\left(dI_{sc}/dI_{ph}\right)$ will be equal to one; that means the change in the short circuit current equals to the change in photo generated current. The deterioration effect of the high series resistance increases by increasing the light intensity. This will limit the benefit of using light concentrators and improve the short circuit current. Many researches have been carried out to reduce the effect of series resistance. Post-deposition heat treatment with $CdCl_2$ to activate CdTe (p) would probably reduce the series resistance and possibly improve ohmic contact performance [23]. Another improvement of CdS/CdTe solar cell can be achieved in the fill-factor. The improvement is achieved by depositing a thin heavily doped p-type semiconductor with a high work function at the back of CdTe layer [24]. Small valence band (<0.2 eV) would be formed between CdTe layer and metal leads to a low or zero potential barrier at the interface and hence an easy hole transport between the two layers. **Figure 8** shows the improvement in quantum efficiency at different annealing temperatures (curves 1 & 2) and depositing thin layer of Te (curve 3) compared with theoretically calculated (curve 4).

More improvements have been made by varying the thickness of CdTe layer. Considering the information of the drift and diffusion components of the photocurrent will lead to the calculation of the short circuit current. Calculation of short circuit current gives an expression of quantum efficiency spectra [21]. In order to reach the total change collection at CdTe layer, the thickness should

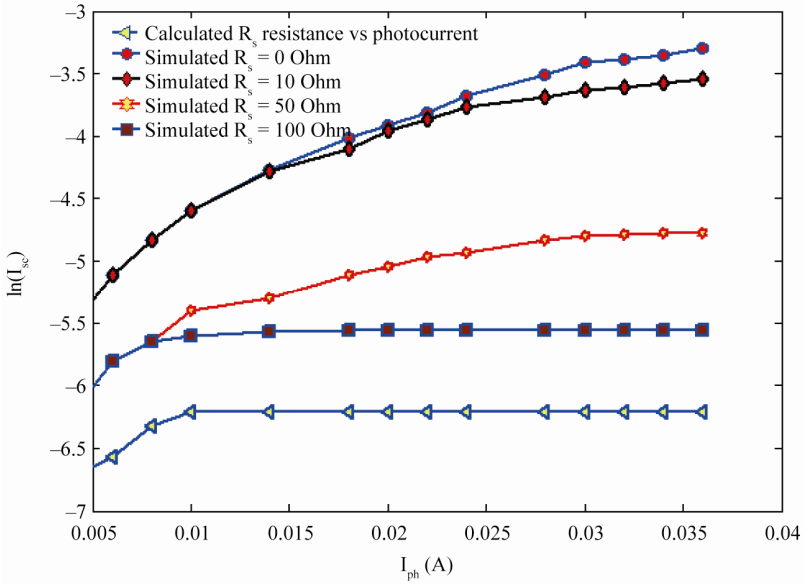


Figure 7. Simulated and calculated short circuit current versus photo current at different values of series resistance.

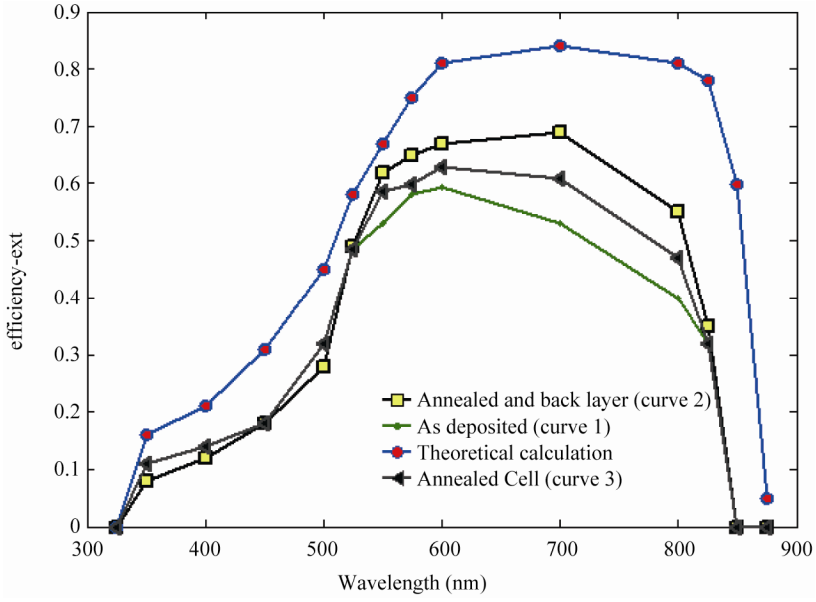


Figure 8. Improvement the quantum efficiency of the solar cell: (1) As deposited; (2) Annealed; (3) With deposited layer and (4) Theoretical calculated.

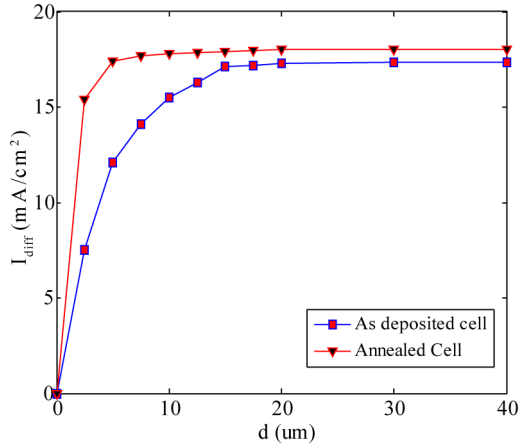


Figure 9. Variation of quantum efficiency of CdS/CdTe solar cell for different values of CdTe thickness: (1) As deposited cell; (2) Annealed cell.

be 50 μm or more [25]. Layer thickness can be reduced by shortening electron life time and hence electron diffusion length. **Figure 9** shows the variation of quantum efficiency of the annealed CdS/CdTe cell for different values of CdTe layer thickness. More than 83% efficiency has been detected at 10 μm thickness with the highest efficiency in the gradual transition between 500 nm and 800 nm (the characteristics of the intermixing between CdTe and CdS layer). High quantum efficiency at the thinner CdTe layer achieved due to the increasing of absorption coefficient. As soon as the photon energy exceeds the band gap of CdTe, the absorption coefficient becomes higher than 10^4 cm^{-1} *i.e.* the effective penetration depth becomes less than 10^{-4} cm (1 nm). This is the reason behind the choice of a few microns (5 - 10 μm) thickness of the CdTe layers. It is evident that the resistance between the CdTe layer and metal back contact is non-ohmic [10]. Actually, there are two diode circuits; the first one is the CdS/CdTe junction (main diode) and the second one is the back contact Schottky diode, which they are connected opposite to each other. Thus, distribution of the applied voltage between the two diodes changes in favor of Schottky diode when applying forward bias voltage to the cell. There is a decrease in the resistance of the main diode and increase that of the Schottky diode.

The above discussions means that the value of the series resistance depends on the voltage applied and current flowing through the cell. According to Schottky theory, the formation of an ohmic contact between a p-type semiconductor and metal results in a high contact resistance due to high potential barrier. Creating a highly doped p++ layer at the surface of CdTe can reduce the effects of the back contact potential barrier. Thinner potential barrier (lower the depletion layer width) produces tunneling or thermally assisted tunneling carrier transport mechanism. The individual sub cell of multi-junction solar cell is interconnected via interband tunnel diode [20]. They feature both low electrical resistivity and high optical transmittance. Reliable simulations of the tunnel diode behavior are still a challenge for solar cell application. Theoretical and experimental measurements of current voltage (I-V) characteristics of tunnel diodes and solar cells had been studied [26]. It is concluded that as the short circuit current of the cell is lower than the maximum tunneling current, the tunnel diode is operated

in the state with lower voltage drop. Hence, the tunnel diode acts like an almost ohmic resistor and will not reduce the maximum power output of the solar cell. If the short circuit current of the cell exceeds the maximum tunneling current, the tunnel diode works in the region where thermal current dominated and high voltage drop occurs over the tunnel diode. I-V curve of the solar cell will be sheared to lower voltages. The test structure consisting of CdS/CdTe solar cell with underlying tunnel diode can be regarded as a series of two diodes connected back-to-back as shown in the left side of **Figure 10**. The tunnel diode is formed by high doping thin layer of CdTe to produce p++ ($5 \times 10^{19}/cm^3$), then depositing another highly doped CdS to produce n++ ($3 \times 10^{19}/cm^3$). The tunnel diode is designed to be able to have a peak current may exceeds values of 50 mA/cm^2. Measured I-V characteristics of a CdS/CdTe solar cell with CdTe (p++) CdS (n++) tunnel diode is shown in the right side of **Figure 10**.

Circled line marks the measurement at low light concentration (<50 mW/cm^2), causing the short circuit current of the cell to be lower than the maximum tunneling current. The short circuit current is increased as long as the photo generated current is increased. Consequently the maximum power output with the solar cell is increased. Dashed line in **Figure 10** marks the measurements at higher light concentration (>50 mW/cm^2) causing the short circuit current to exceed the maximum tunneling current. When critical illumination is reached, the cell current exceeds the tunneling current of the tunnel diode and voltage dip appears in the I-V characteristics.

5. Conclusion

CdTe based solar cell is a leading technology in thin film energy conversion efficiency. Their energy conversion efficiency is degraded by the high series resistance of the cell. The resistance is a combination of contact resistances, semiconductor resistance and non-ohmic ones of the back contact. The contact resistance and semiconductor resistances can be modified by annealing, fabrication parameter and using materials of low resistivity at the contacts. The non-ohmic contact can be modified by connecting tunnel diode at the back of the cell. The only limitation to this approach is that the short circuit current of the cell should not exceed the maximum tunneling current of the tunnel diode. More research and study about this point is needed. AC measurements in wide range of frequencies should be carried out to measure impedances of both diodes and then more adequate physical model can be suggested.

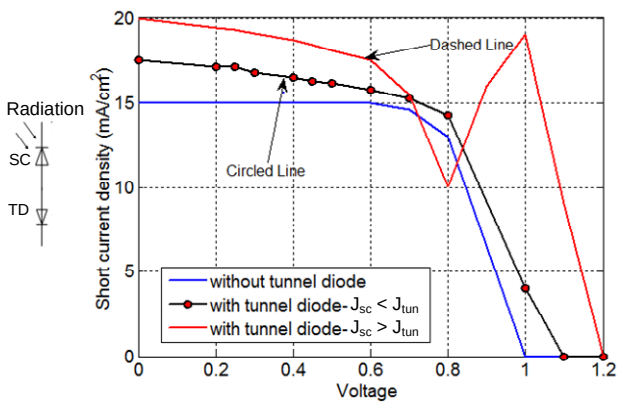


Figure 10. I-V characteristics of a CdS/CdTe solar cell. (a) Without tunnel diode; (b) With tunnel diode and $J_{sc} > J_{tun}$; (c) With tunnel diode and $J_{sc} < J_{tun}$.

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