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A New Current-Controlled-Power Technique for Small Signal Applications

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ABSTRACT

In this paper, a new current-controlled-power technique for small signal applications is presented. The proposed technique needs no passive devices (a resistor and a capacitor) but the well-known SCR technique needs, thus the proposed technique is very suitable for an IC process. An example application as a new current-controlled-power CMOS full-wave rectifier is also given. The example application is simulated by using the SPICE program. Simulation results show that the proposed technique can work well; the controlled-current from 0 μA to 5.5 μA produces the peak area amplitude from 100 mV to 0 mV to the load.

Keywords: Current-Controlled-Power; Full-Wave Rectifier; Analog Signal Processing

1. Introduction

As is well known, it is hard to find the device that operates as a silicon-controlled rectifier (SCR) [1] for controlling the power in small signal applications. In this paper, the author presents a new current-controlled-technique for small signal applications. The proposed technique yields the advantages:

- The proposed technique needs no a capacitor and a resistor but the well-known SCR technique needs; therefore, without passive devices, the proposed technique uses a much smaller chip area in the IC process [2].
- The proposed technique works with a small signal but the SCR technique cannot work because of the threshold voltage of the SCR [1].
- The proposed technique can also work with a large signal by driving a power bipolar transistor.
- The proposed technique with current-controlled is very suitable for an automatic control system by the current feedback. Whereas the SCR technique uses the RC time constant for clipping time [1], it is hard for the automatic control system.

The example application as a new current-controlled-power CMOS full-wave rectifier is also presented. It provides the advantages as follows.

- The new full-wave rectifier works both full-wave rectification and current-controlled-power operation. But the previous proposed full-wave rectifiers cannot control the output power.
- The new rectifier uses all MOSs with typical structure thus it is very suitable for IC processes [3].
- The new rectifier, its core operates in balanced mode resulting in a low noise output [4].
- Using the new rectifier, one can independently control the positive part and the negative part of the input signal, this yields more precision control.

2. Proposed Current-Controlled-Power Technique

The proposed technique is shown in **Figure 1(a)** and its signals are shown in **Figure 1(b)**. The operation is as follows. I_{CL1} is fed to shift down the input differential current signal (I_{in+}). It will decrease the amplitude and area of the positive signal and will increase those of the negative signal. The bias source (V_b) is the voltage or current, for turning-on the current mirror (MN1 and MN2) all the time for very small signal operation. The V_b must be the minimum voltage or current to make the minimum offset at the output (I_{out}). The I_{out} is the positive signal rectified by the current mirror. Because the input signal is shifted down, one must compensate this for (I_{in-}) by feeding I_{CL2} for balancing the input signal.

Note the proposed technique that the output is a horizontal clipped signal but the well-known SCR technique the output is a vertical clipped signal. The proposed technique with all active devices is better than the SCR technique with the resistor and capacitor devices in view of IC fabrication. Additionally, the proposed technique with current-controlled is very suitable for automatic control system by a current feedback. Whereas the SCR

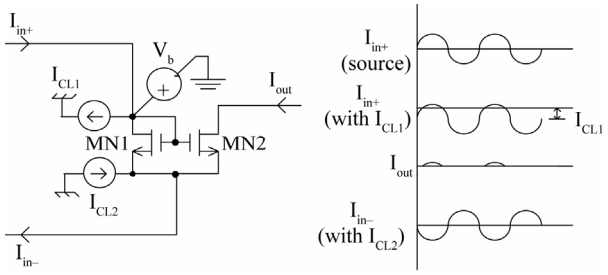

Figure 1. Proposed technique: (a) circuit and (b) operation.

technique uses the RC time constant for clipping time, it is hard for automatic control system. Moreover, the proposed technique can be used in high power applications; it can drive the high current bipolar transistor.

3. Application Example as a New Current-Controlled-Power Full-Wave Rectifier

The circuit in **Figure 2** operates as a full-wave rectifier where $I_{CL+1} = I_{CL+2} = I_{CL-1} = I_{CL-2} = 0$. Its operation is as follows. The constant current source I_C is mirrored by MI1 and MI3 to the drain of M3 (I_{D3}); and is mirrored by MI1, MI2, MI4 and MI5 to the drain of M1 (I_{D1}). The W/L ratios of MI1 to MI5 are equal, making $I_{D1} = I_{D3}$. Moreover, using matched MOS transistors M1 to M4 [5], the input voltage is thus followed to a MOS resistor (R_A) [6], the resistance of which is given by

$$R = \frac{1}{2KV_{DT}} \tag{1}$$

where MA1 and MA2 have the same characteristics; $K = \mu C_{ox}W/L$, μ is the carrier mobility, C_{ox} is the gate capacitance per unit area, W and L are the channel width and length respectively; $V_{DT} = V_{DD} - V_T = -(V_{SS} + V_T)$, $V_{DD} = -V_{SS}$, V_T is the threshold voltage.

Equation (1) is valid when both MA1 and MA2 maintain in the saturation region, which is true if

$$|V_A| \le V_{DT} \tag{2}$$

This input voltage creates the current I_{in} flowing through R_A.

$$I_{\text{in}} = V_{\text{in}} 2KV_{DT} \tag{3}$$

In **Figure 2**, I_{in} is mirrored by M5, M6, M9, and M10 as I_1; and is mirrored by M5, M7, M9, and M11 as $I_4 = -I_1$. Furthermore, I_{in} is mirrored by M5, M8, M9, M12, M13, M14, M16, and M17 as I_2; and is mirrored by M5, M8, M9, M12, M13, M15, M16, and M18 as I_3. One assumes that the gain of all current mirrors is unity, thus

$$\left.\begin{aligned} I_1 &= I_2 \\ I_3 &= I_4 \end{aligned}\right\} \tag{4}$$

When the input voltage is positive, the current mirror (M19 and M20) turns on and the current mirror (M21 and M22) turns off. Inversely, when the input voltage is negative, the current mirror (M19 and M20) turns off and the current mirror (M21 and M22) turns on, resulting in

$$\left.\begin{aligned} V_{\text{in}} > 0;\ I_1 = I_2 = I_{\text{in}};\ I_3 = I_4 = 0 \\ V_{\text{in}} < 0;\ I_1 = I_2 = 0;\ I_3 = I_4 = I_{\text{in}} \end{aligned}\right\} \tag{5}$$

The drain currents of M20 and M22 are finally mirrored by M23 and M24 and then are converted to the voltage by R_B. Using $R_A = R_B$ by setting MA1 = MA2 = MB1 = MB2, the relation between input and output voltages (full-wave rectification) can be written as

$$\left.\begin{aligned} V_{\text{in}} > 0;\ V_{\text{out}} &= V_{\text{in}} \\ V_{\text{in}} < 0;\ V_{\text{out}} &= -V_{\text{in}} \end{aligned}\right\} \tag{6}$$

The bias sources (V_{b1} and V_{b2}) in **Figure 1** may be the voltage or current source. This bias source makes the MOSs in core 1 and core 2 (M19, M20, M21, and M22) turning-on all the time, to reduce the error at zero-crossing of the full-wave output signal.

Three main errors of the operation of the proposed rectifier can be considered. Assume that the error of W/L ratios of MOS transistors is ignored since it is very small in the present technology.

The first error is for transferring an input voltage to node A [5] because the currents I_{D1} and I_{D3} are slid resulting from the error of simple current mirrors (MI1 to MI5). This error can be minimized by using the better current mirrors (cascode or Wilson type); however, it requires higher supply voltage [7].

The second error is for mirroring the input current from R_A to core 1 and core 2. And the last error is the error of core 1 and core 2. The second and the last errors can be reduced by using the better current mirrors as mentioned above.

The best way for setting three above errors to minimize, is compensation. The compensation can be done by adjusting the gain of core 1 and core 2 through the W/L ratios (of M20 for positive input and of M22 for negative input). In addition, adjusting the resistant of R_B through W/L ratios of MB1 and MB2 is also compensation.

M2 and M4 must be in the saturation mode as M1 and M3; this yields the input operation range,

$$\left.\begin{aligned} V_{\text{in(min)}} &= \frac{V_{SS} + |V_{eff4}| + |V_{eff9}| + |V_{TP}| + |V_{TN}|}{\alpha} \\ V_{\text{in(max)}} &= \frac{V_{DD} - |V_{eff2}| - |V_{eff5}| - |V_{TN}| - |V_{TP}|}{\alpha} \end{aligned}\right\} \tag{7}$$

where $V_{eff} = V_{GS} - V_T = \sqrt{\dfrac{2I_D}{\mu C_{OX}(W/L)}}$ [7], and α is the

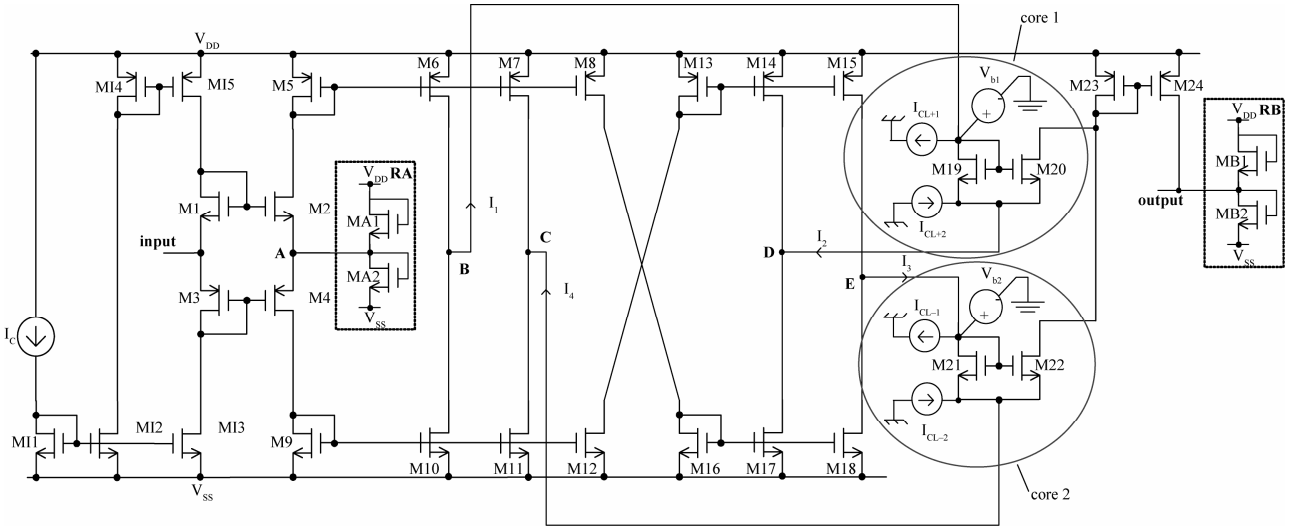

Figure 2. Application example as a new current-controlled-power full-wave rectifier.

voltage gain between input and node *A*, ideally it must be unity.

In the same way, M6, M7, M8, M10, M11, M12, M14, M15, M17, and M18 have to be in the saturation mode. If these MOSs have the same parameters, one can write the operation range of signals at nodes *B*, *C*, *D*, and *E* as

$$\left.\begin{aligned} V_{B,C,D,E(\min)} &= V_{SS} + \left|V_{effN}\right| + \left|V_{TN}\right| \\ V_{B,C,D,E(\max)} &= V_{DD} - \left|V_{effP}\right| - \left|V_{TP}\right| \end{aligned}\right\} \quad (8)$$

Using the same characteristics M5 to M18, considering Equations (2), (7), and (8), the operation range of the proposed full-wave rectifier is considered as (7).

Note that two signals of core 1 at nodes *B* and *D*, two signals are 180 degrees out-of-phase; hence, some in-phase outside noise around the core will be cancelled, as well-known. It is also for core 2. This indicates that the proposed rectifier operates in a balanced mode, canceling some outside noise around the core.

As mentioned above, if we feed the control current ($I_{CL+1} = I_{CL+2}$), we can control the peak area of the positive input signal (see **Figure 1(b)**). Moreover, by feeding $I_{CL-1} = I_{CL-2}$, we also can control the peak area of the negative input signal. It is evident that we can independently control the positive part and the negative part of the input signal, this yields more precision control.

At this point, we can see that one application example of the new current-controlled-power technique is the new full-wave rectifier. The new rectifier can be realized by using all MOS transistors with typical structure. It is very suitable for the process of IC fabrication. Furthermore, not only full-wave rectification but also current-controlled-power operation, the proposed rectifier can work. The previous proposed rectifiers cannot operate this current-controlled-power function. Additionally, the balanced mode operation of the core gains a lower noise output.

4. Results

To verify the theoretical design, the application example as a new current-controlled-power full-wave rectifier was simulated by using parameters extracted from its layout (including parasitic capacitance) in a 0.5 μm AMI MOS transistor technology, through a level-49 model.

The supply voltage is ±1.2 V. For full-wave rectifier simulation, I_C is 20 μA, $V_{b1} = V_{b2}$ are the current sources of 5 μA, $I_{CL+1} = I_{CL+2} = I_{CL-1} = I_{CL-2}$ are 0 μA. The W/L ratios of MA1 = MA2 = 1.5 μm/1.5 μm, MB1 = MB2 = 1.5 μm/3.9 μm, and other MOSs = 20 μm/0.6 μm, were chosen.

Figure 3 shows the output of the proposed full-wave rectifier with a sine wave input signal (100 mV_{peak}, 100 kHz). The amplitude error of the output signal is almost zero because of compensation by using $R_B > R_A$, by adjusting their *W*/*L* ratios as mentioned in Section 3. Also, the gain compensation can be done through the *W*/*L* ratios of M20, M22, and M24. The author tried to decrease the amplitude of the input signal; one found that the proposed rectifier can rectify a minimum voltage of 350 μV_{peak}. Changing frequency was done, the maximum operation frequency of the proposed rectifier was 30 MHz (–3 dB point).

For current-controlled-power operation, the author set $I_{CL+1} = I_{CL+2} = I_{CL-1} = I_{CL-2}$ following to the left column of **Table 1**, the right column shows the rectified output peak area amplitude. According to the theory, it was (namely, more $I_{CL+1} = I_{CL+2} = I_{CL-1} = I_{CL-2}$, more shifted-down signal, less output peak area amplitude).

As mentioned in Section 3 that we can independently control the positive part and the negative part of the input signal, this yields more precision control. We will show

it here. The rectifier output can be divided to two parts for controlling (*A*. the positive input part and *B*. the negative input part shifted the phase by 180 degrees, by rectifier). *A* is controlled by $I_{CL+1} = I_{CL+2}$ and *B* is controlled by $I_{CL-1} = I_{CL-2}$. **Figure 4** shows the full-wave rectified output with $I_{CL+1} = I_{CL+2} = 1$ μA and $I_{CL-1} = I_{CL-2} = 3.5$ μA (changing the frequency to 1 MHz). It also shows that we can independently control the positive part and the negative part of the input signal, giving more precision control. Moreover, the proposed current-controlled- power full-wave rectifier is very suitable for an automatic control system by the current feedback. Whereas the SCR technique uses the RC time constant for clipping time, it is hard for the automatic control system.

Absolutely, not only full-wave rectification but also current-controlled-power operation, the proposed rectifier can work. The previous proposed rectifiers cannot operate this current-controlled-power function.

5. Conclusions

In this paper, the author has reported a new current-controlled-power technique that can be useful in analog small signal processing. The proposed technique needs no passive devices; it is very suitable for the IC process. The proposed technique can also work with a large signal by driving a power bipolar transistor. The proposed technique is very suitable for an automatic control system by the current feedback.

An application example as a new current-controlled-power full-wave rectifier has also been proposed. The new full-wave rectifier works both full-wave rectification

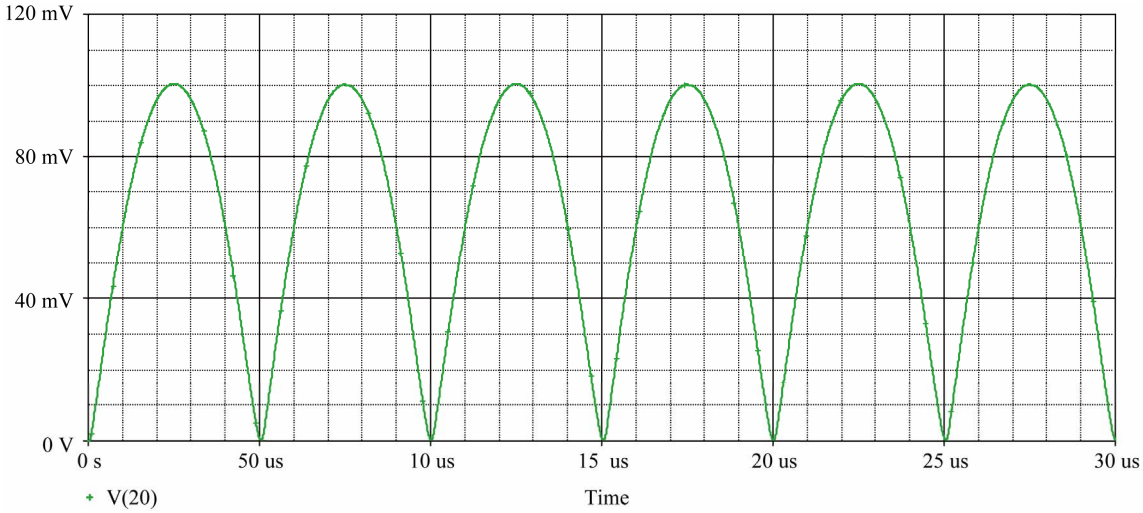

Figure 3. Output of the proposed current-controlled-power full-wave rectifier ($I_{CL+1} = I_{CL+2} = I_{CL-1} = I_{CL-2} = 0$) with an input sine wave of 100 mV_{peak}, 100 kHz.

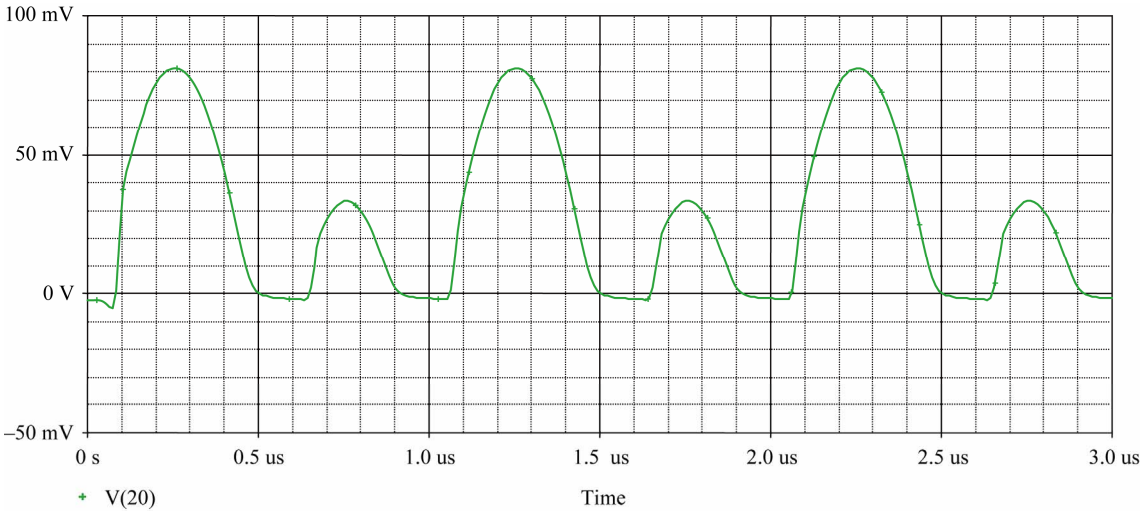

Figure 4. Output of the proposed current-controlled-power full-wave rectifier with an input sine wave, 100 mV_{peak}, 1 MHz, ($I_{CL+1} = I_{CL+2} = 1$ μA and $I_{CL-1} = I_{CL-2} = 3.5$ μA).

Table 1. Relation between the controlled current and the output.

$I_{CL+1} = I_{CL+2} = I_{CL-1} = I_{CL-2}$ (μA)	Output peak area amplitude (mV)
0	100
0.5	91
1	81.7
1.5	72.3
2	62.8
2.5	53.1
3	43.3
3.5	33.4
4	23.4
4.5	13.5
5	1.9
5.5	0

and current-controlled-power operation. The new rectifier uses all MOSs with typical structure thus it is very suitable for the IC process. The new rectifier, its core operates in balanced mode resulting in a low noise output. Using the new rectifier, one can independently control the positive part and the negative part of the input signal, this yields more precision control.

It should be noted on the use of the new rectifier that it is suitable for a high impedance load. If the low impedance load is applied, it needs a voltage buffer at the output.

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