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Design and Analysis of a Power Efficient Linearly Tunable Cross-Coupled Transconductor Having Separate Bias Control

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ABSTRACT

A common current source, generally used to bias cross-coupled differential amplifiers in a transconductor, controls third harmonic distortion (HD_3) poorly. Separate current sources are shown to provide better control on HD_3. In this paper, a detailed design and analysis is presented for a transconductor made using this biasing technique. The transconductor, in addition, is made to offer high G_m, low power dissipation and is designed for linearly tunable G_m with current mode load as one of the applications. The circuit exhibits HD_3 of less than –43.7 dB, high current efficiency of 1.18 V^{-1} and G_m of 390 μS at 1 $V_{p\text{-}p}$ @ 50 MHz. UMC 0.18 μm CMOS process technology is used for simulation at supply voltage of 1.8 V.

Keywords: Analog Electronics; Low Power Analog CMOS Circuit; Operational Transconductance Amplifier (OTA); Multiple-Output OTA (MOTA); MOS Transconductors; Linearly Tunable G_m; Current Efficiency; Linearization Techniques; Harmonic Distortion Analysis

1. Introduction

Transconductors interface a current mode circuit to a voltage signal, making it a fundamental element of analog circuits [1-4]. Performance of a transconductor deteriorates due to higher total harmonic distortion (THD), more so at high signal level. Several techniques are devoted to improve THD of transconductors [5-20]. Sánchez-Sinencio and J. Silva-Martínez [4] have classified these as input signal attenuation [5-7], cancellation of nonlinear terms [7-12], and source degeneration [7, 11-19]. Besides these, adaptive biasing [16,19] and mobility compensation [20] techniques are also reported to improve THD.

One of the important building blocks in many analog circuits is a tunable linear transconductor [9,13,15,17, 21-25], which may be used for tuning center frequency and Q-factor of filters. Moreover it helps to compensate fabrication tolerances and environment parameters, especially temperature.

A method of tuning transconductance, G_m is to control the bias current (I_{Bias}) applied to the differential amplifier. But G_m is proportional to the square root of I_{Bias} due to which the allowable input signal swing is limited to small value [1]. In [17], the allowable input swing for a constant value of I_{Bias} is made independent of variation in G_m by using current mirrors with source degeneration.

Another tuning method uses source degeneration resistance (R). In this method due to degeneration, THD improves but at the cost of transconductance. Further, the condition of improvement, ($1/G_m < R$) [1] occupies large area and add noise if passive resistance is used. In [13], tunability has been achieved using active resistance. But G_m adjustment in this tuning method affects the bandwidth, which has been compensated in [15] by employing a separate source follower biased with constant current source.

Linearly adjustable G_m is realized using control voltage at inputs of one of the cross-coupled differential amplifier [8,9]. In both the papers authors have used identical transistors in the cross-coupled amplifiers to obtain linear tuning of G_m at supply voltage 5 V or higher. Different bias strategies are given in [25] to achieve tunability for ultra low range transconductance.

A low voltage transconductor on 0.18 μm technology is given by us in [23] in which bias currents of cross-coupled differential amplifiers and aspect ratio of their

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transistors are adjusted to cancel third harmonic distortion. Shift level biasing is used in the cross-coupled differential amplifier to obtain tunability. The circuit is designed for resistive load, not suitable for current mode signal processing.

The topology cited in [23] is analyzed in detail in this paper. In addition diode mode MOSFETs are used as load for current mode signal processing in place of active resistance. A triode mode tail transistor is used in MA for better linear tuning instead of constant current source. Design steps in detail with algorithm are given for low HD_3, high linearly tunable G_m and high frequency of operation at low voltage. Efforts have also been made to maintain low power operation and high current efficiency. The circuit is developed for 1 V_{p-p} input signal for frequency range upto 50 MHz.

The paper is organized as follows. In Section 2, block diagram, circuit design alongwith its algorithm and analysis of the proposed circuit are given. In Section 3, simulation results are discussed and finally conclusions are drawn in Section 4.

2. Design and Analysis of Tunable Transconductor

2.1. Block Diagram of Tunable Transconductor

The proposed transconductor is designed using main differential amplifier (MA) biased using tail transistors in triode mode, compensatory differential amplifier (CA) biased using separate constant current source for minimizing HD_3 and level shifters (LS) are used for tunability. Separate controls of the two bias currents of MA and CA provide flexibility, improvement in HD_3 and better tuning in comparison to others [8,9]. Block diagram of the proposed transconductor is shown in **Figure 1** and the complete circuit diagram is furnished in **Figure 2**.

The square law model of MOSFETs is used in this work for design and analysis. Design steps are given below:

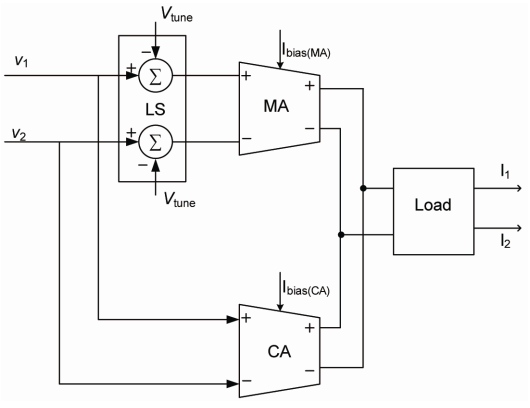

Figure 1. Functional block diagram of the trnsconductor.

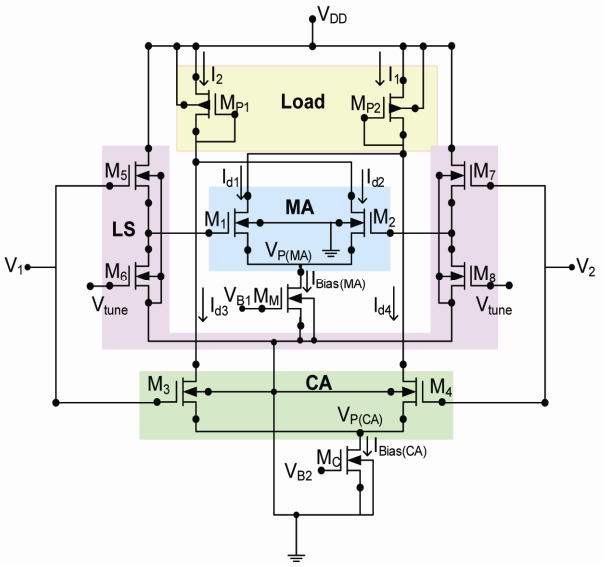

Figure 2. Circuit diagram of the transconductor.

2.1.1. Design of MA

Upper limit and lower limit of biasing current ($I_{Bias(\mathrm{MA})}$) for MA are given as follows [3]:

$$I_{Bias(\mathrm{MA})_{(\max)}} \ll P_{Diss}/V_{DD} \tag{1}$$

$$I_{Bias(\mathrm{MA})_{(\min)}} \geq \left(2*\omega_{3\mathrm{dB}}*C_l\right)/\left(\lambda_n+\lambda_p\right) \tag{2}$$

where P_{Diss} is the specified total power consumption, C_l is the load capacitor, $\omega_{3\mathrm{dB}}$ is the 3 dB frequency, λ_n and λ_p are the channel length coefficients of NMOS and PMOS transistors respectively. MA is designed using NMOS transistors and load using PMOS transistors.

Transconductance, $G_{m(\mathrm{MA})}$ of MA and input swing, V_{swing} are given in [1,3] and are reproduced in Equation (3) and Equation (4).

$$G_{m(\mathrm{MA})} = \sqrt{\mu_n C_{ox}\left(W/L\right)_{\mathrm{MA}} I_{Bias(\mathrm{MA})}} \tag{3}$$

$$V_{\mathrm{swing}} = \sqrt{\left(2I_{Bias(\mathrm{MA})}\right)/\left\{\mu_n C_{ox}\left(W/L\right)_{\mathrm{MA}}\right\}} \tag{4}$$

From Equation (3) $G_{m(\mathrm{MA})}$ is the function of $I_{Bias(\mathrm{MA})}$ and $\left(W/L\right)_{\mathrm{MA}}$. To keep high $G_{m(\mathrm{MA})}$, higher values of $I_{Bias(\mathrm{MA})}$ are not used as it would lead to loss of power. The second option is to increase the aspect ratio but that may deteriorate HD_3 for specified input swing {Equation (4)}.

The second option is preferred wherein, for better HD_3, the method of non-linear terms cancellation with the help of compensatory amplifier is used but at the cost of area occupied by it. However, the use of CA (**Figure 2**) reduces overall transconductance. To maintain transconductance G_m of the OTA at the desired level, $G_{m(\mathrm{MA})}$ is adjusted {Equation (7)}. For high current efficiency (*i.e.* G_m/I_{DD}), $I_{Bias(\mathrm{MA})}$ is selected slightly greater than

$I_{Bias(\mathrm{MA})_{\min}}$ and aspect ratio $(W/L)_{\mathrm{MA}}$ is determined from Equation (3) for the modified value of $G_{m(\mathrm{MA})}$. In addition, $I_{Bias(\mathrm{MA})}$ is allowed to vary independently of CA as a function of tuning voltage by operating tail transistor of MA in triode mode.

2.1.2. Design of CA

The ratio "*p*" of bias currents of MA and CA are adjusted [11,12] in accordance with Equation (5):

$$p = q^3 \tag{5}$$

where $p = I_{Bias(\mathrm{MA})} / I_{Bias(\mathrm{CA})}$ and $q = (W_{\mathrm{MA}}/L_{\mathrm{MA}})/(W_{\mathrm{CA}}/L_{\mathrm{CA}})$. A lower value of "*q*" not only increases power dissipation (due to high bias current of CA), but also lowers the overall transconductance, thereby, decreasing the current efficiency. On the other hand, due to higher values of "*q*" the harmonics will not be suppressed effectively. Moreover, it is difficult to bias the CA transistor in saturation region in the specified low voltage operation due to skewed overdrive voltages of the MA and CA. In the proposed circuit choosing a moderate "*q*" as 2 and equal channel length of MA and CA gives:

$$W_{\mathrm{MA}}/W_{\mathrm{CA}} = 2 \tag{6}$$

and $I_{Bias(\mathrm{MA})}/I_{Bias(\mathrm{CA})} = 8$. This ratio of bias currents is adjusted for the centre value of the tuning voltage range at which specified G_m is expected to occur.

Overall transconductance G_m due to cross-coupling of MA and CA is the difference of $G_{m(\mathrm{MA})}$ and $G_{m(\mathrm{CA})}$, hence $G_{m(\mathrm{MA})}$ is selected to get the specified G_m in accordance of Equation (7).

$$G_{m(\mathrm{MA})} = \left\{q^2/\left(q^2-1\right)\right\} G_m \tag{7}$$

2.1.3. Design of Load

The PMOS transistors, M_{p1} and M_{p2} are selected in diode mode as load. It is possible to easily convert the proposed transconductor to Multiple-output OTA suitable for current mode signal processing by incorporating three current mirrors. The aspect ratio of load transistors is computed using the Equation (8), where in Equation (8) $V_{CM_{\max}}$ is the maximum common mode input voltage at MA, V_{thn} and V_{thp} are the threshold voltages of NMOS and PMOS transistors respectively.

$$(\mathrm{W/L})_{load} = \frac{\left(I_{Bias_{(\mathrm{MA})}} + I_{Bias_{(\mathrm{CA})}}\right)}{\left\{\mu_p C_{ox} * \left(V_{DD} - V_{CM_{\max}} - V_{thn} - V_{thp}\right)^2\right\}} \tag{8}$$

2.1.4. Design of LS

Linearly tunable G_m is obtained by modulating common mode voltage with V_{tune} in two level shifters. The transistors (M_5 and M_6) of a level shifter of LS are selected to have same aspect ratio to maintain same V_{tune} across gate to source in both the transistors. They are biased in saturation region by following the conditions given in Equation (9) and Equation (10).

$$V_1(\text{or } V_2) < V_{DD} + V_{thn} \tag{9}$$

$$V_{thn} < V_{tune} < \left\{V_1(\text{or } V_2) + V_{thn}\right\}/2 \tag{10}$$

where $V_1 = \left(V_{DC} + \frac{v_{id}}{2}\right)$ and $V_2 = \left(V_{DC} - \frac{v_{id}}{2}\right)$ are the signal inputs applied at the gates of M_5 and M_7 of level shifters, respectively. Same input V_1 and V_2 are applied to the gate of M_3 and M_4 of CA. As per the Equation (10) higher values of V_1 (or V_2) give better tuning range, accordingly, V_{DC} is selected slightly less than to V_{DD}. Further, MA remains in saturation if and only if condition given in Equation (11) is satisfied.

$$V_{tune} \le V_1(or\, V_2) - V_{thn} - V_{P_{(\mathrm{MA})}} \tag{11}$$

where $V_{P_{(MA)}}$ is the drain to source voltage of tail transistor of MA Thus, the limits on V_{tune} are obtained as in Equation (12). Transistors of other level shifter of LS are also made identical on the same ground.

$$V_{thn} < V_{tune} \le \min\left[\left\{V_1(\text{or } V_2) + V_{thn}\right\}/2,\; V_1(\text{or } V_2) - V_{thn} - V_{P_{(\mathrm{MA})}}\right] \tag{12}$$

2.1.5. Design of Tail Transistor of MA

As the bias current supplied to MA by its tail transistor is a function of tuning voltage, it is operated in triode mode. It needs $V_B > V_{P_{(MA)}} + V_{thn}$, where V_{B1} is gate voltage of tail transistor of MA. The aspect ratio of tail transistor of MA is derived for the mentioned operating mode and is given in Equation (13):

$$(W/L)_{T_{(\mathrm{MA})}} = I_{Bias(\mathrm{MA})} \Big/ \left\{(\mu_n C_{ox})(V_{B1} - V_{thn}) V_{P_{(\mathrm{MA})}}\right\} \tag{13}$$

2.1.6. Design of Tail Transistor of CA

Tail transistor of CA is chosen as constant current source independent of $I_{Bias(MA)}$ by biasing the transistor in saturation. The aspect ratio of it is given in Equation (14):

$$(W/L)_{T_{(\mathrm{CA})}} = \frac{2I_{Bias_{(\mathrm{CA})}}}{(\mu_n C_{ox})(V_{B2} - V_{thn})^2} \tag{14}$$

where V_{B2} is gate voltage of tail transistor of CA.

2.2. Algorithm for Designing the Proposed Transconductor

The algorithm to design proposed transconductor is summarized as below:

Step 1	Compute $I_{Bias(\mathrm{MA})_{(\max)}}$	/* from specified P_{Diss}; refer Equation (1)*/
Step 2	Compute $I_{Bias(\mathrm{MA})_{(\max)}}$	/* from specified ω_{3dB}; refer Equation (2)*/
Step 3	Select $I_{Bias(\mathrm{MA})} \geq I_{Bias(\mathrm{MA})_{(\max)}}$	/* to increase current efficiency*/
Step 4	Compute $G_{m(\mathrm{MA})}$	/* for specified G_m ; refer Equation (7)*/
Step 5	Compute $(W/L)_{\mathrm{MA}}$	/* using Equation (3)*/
Step 6	Calculate $(W/L)_{\mathrm{CA}}$	/* using Equation (6)*/
Step 7	Select diode mode MOSFET load	/* for current mode signal processing*/
Step 8	Compute $(W/L)_{load}$	/* using Equation (8)*/
Step 9	Compute $(W/L)_{LS}$	/*minimum size transistors*/
Step 10	Design tail transistor of MA	/*refer (13)*/
Step 11	Design tail transistor of CA	/*refer (14)*/
	END	

2.3. Analysis of the Circuit

The analysis of the circuit is given below:

In **Figure 2**, applying the square law to the transistors of MA and CA, which are biased in saturation region, the currents, I_1 and I_2 through load transistors of the cross-coupled amplifiers (MA-CA) are given by:

$$I_1 = I_{d1} + I_{d4} = \beta_{\mathrm{MA}}\left(V_1 - V_{tune} - V_{P_{(\mathrm{MA})}} - V_{thn}\right)^2 + \beta_{\mathrm{CA}}\left(V_2 - V_{P_{(CA)}} - V_{thn}\right)^2 \quad (15)$$

$$I_1 = I_{d2} + I_{d3} = \beta_{\mathrm{MA}}\left(V_2 - V_{tune} - V_{P_{(\mathrm{MA})}} - V_{thn}\right)^2 + \beta_{\mathrm{CA}}\left(V_1 - V_{P_{(CA)}} - V_{thn}\right)^2 \quad (16)$$

where $\beta = (1/2)\mu C_{ox}(W/L)$ is the transconductance parameter. $V_{P_{(\mathrm{MA})}}$ and $V_{P_{(\mathrm{CA})}}$ are the drain to source voltage across tail transistor of MA and CA respectively.

The differential output current, i_o is given by

$$i_0 = I_1 - I_2 = 2(v_{id})\left[\left\{(\beta_{\mathrm{MA}} - \beta_{\mathrm{CA}})(V_{DC} - V_P - V_{thn})\right\} - \beta_{\mathrm{MA}} V_{tune}\right] \quad (17)$$

where $V_{P_{(\mathrm{MA})}} \cong V_{P_{(\mathrm{CA})}} = V_P$ is assumed.

Since "q" is taken as 2 to minimize HD_3:

$$\beta_{\mathrm{MA}} = 2\beta_{\mathrm{CA}} \quad (18)$$

Combining Equation (17) and Equation (18), one gets:

$$i_0 = (v_{id})\left\{\beta_{\mathrm{MA}}(V_{DC} - V_P - V_{thn}) - 2\beta_{\mathrm{MA}} V_{tune}\right\} \quad (19)$$

From Equation (19) the transconductance G_m is calculated as,

$$G_m = \frac{\partial i_0}{\partial v_{id}} = \beta_{\mathrm{MA}}(V_{DC} - V_P - V_{thn}) - 2\beta_{\mathrm{MA}} V_{tune} \quad (20)$$

Equation (20) shows linear behaviour of G_m with V_{tune}, as first part, $\beta_{\mathrm{MA}}(V_{DC} - V_P - V_{thn})$ on the right hand side of the equation is almost constant. Thus from Equation (20) the tuning range is obtained and is given in Equation (21).

$$G_{m_{range}} = \left|2\beta_{MA} V_{tune}\right| \quad (21)$$

3. Simulation Results and Discussions

The proposed transconductor is simulated in Cadence VIRTUOSO environment using UMC 0.18 µm CMOS process technology. The transconductor is operated at 1.8 V and 27° Celsius. Bias currents $I_{Bias_{(\mathrm{MA})}}$ and $I_{Bias_{(\mathrm{CA})}}$ are kept at 200 µA and 25 µA, respectively to maintain $I_{Bias_{(\mathrm{MA})}} / I_{Bias_{(\mathrm{CA})}} = 8$. Channel length is taken as 0.9 µm which is five times the minimum as specified by the technology for all the MOSFETs of the transconductor to minimize channel length modulation effect [26]. The differential signal input voltage of 0.25 V is generated using voltage controlled voltage source (VCVS) as test bench setup.

The objective of the simulation is to demonstrate feasibility of power efficiency, linear tuning of G_m offering low harmonics with the help of separate bias control of cross-coupled amplifiers at 50 MHz and above. Different plots have been obtained to verify the designed aspects.

Plot in **Figure 3** shows the tunability of the proposed transconductor. The tuning voltage, V_{tune} is varied from 0.5 V to 1.0 V in steps of 0.1 V. The lower value (0.5 V) is kept slightly higher than the threshold voltage of input transistors M_5 and M_7 of LS and upper value is selected as per Equation (12) to keep them in saturation region. G_m is tuned between 390 µS to 195 µS. G_m is falling with increase in V_{tune} between ±0.25 V of v_{id} *i.e.* 1 $V_{p\text{-}p}$, However for higher values of v_{id}, (around ±0.5 V *i.e.* 2

V_{p-p}) the change in G_m w.r.t. V_{tune} is nonlinear and plots for different values of V_{tune} are almost merged at a point, indicates transconductance is independent of V_{tune}. The reason being that as per Equation (12), $V_1(or\,V_2) < V_{DD} + V_{thn}$, but at higher values, this condition is violated. At $V_1(or\,V_2) = V_{DD} + V_{thn}$ transistor M_5 and M_7 of **Figure 2** are at the verge of saturation, and variation in drain to source voltage across it is small enough, making output of level shifter is almost constant, *i.e.* independent of tuning voltage.

As shown in **Figure 4** the variation of transconductance with respect to tuning voltage is linear validating Equation (20). The small deviation may be attributed to body effect in LS transistors (M_5 and M_7) and voltage drop in tail transistors.

Figure 5 shows HD_3 variation with respect to differential input signal amplitude for different values of tuning voltage. Distortion increases rapidly for the small values *i.e.* upto approximately 150 mV (0.6 V_{p-p}) of the differential input signal amplitude but after that it in creases slowly due to cross-coupling effect. Harmonic distortion has also increased with the increase in tuning voltage due to decrease in DC current through MA. **Figure 6** shows variation of HD_3 with respect to V_{tune}.

Frequency response of the proposed transconductor for different values of tuning voltage is given in **Figure 7**. The 3 dB frequency of the transconductor is above 53 MHz for the complete range of variation of transconductance.

G_m, HD_3, P_{Diss} and G_m/I_{DD} for the three different values of G_m obtained from the simulation are given in **Table 1**. It may be noted that at lower values of transconductance current efficiency reduces. The reasons are twofold: firstly, transconductance is low and secondly lower transconductance obtained at higher value of tuning voltage, gives high overdrive voltage to LS transistors which in turn draws higher current through LS.

The performance is compared on eight metric points with other reported circuits as given in **Table 2**. The proposed transconductor offers better current efficiency

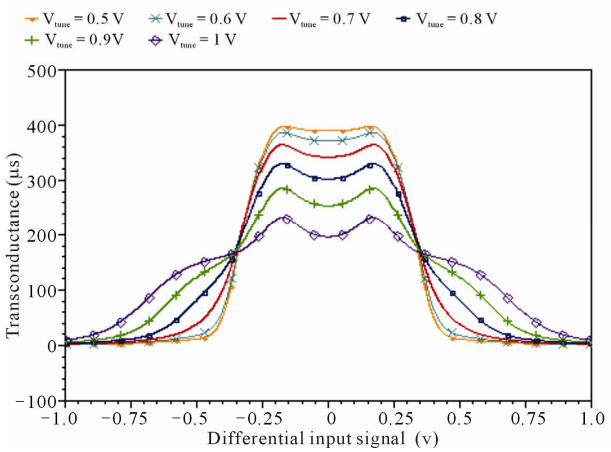

Figure 3. Transconductance (G_m) vs differential signal input (v_{id}) at different values of tuning voltage (V_{tune}).

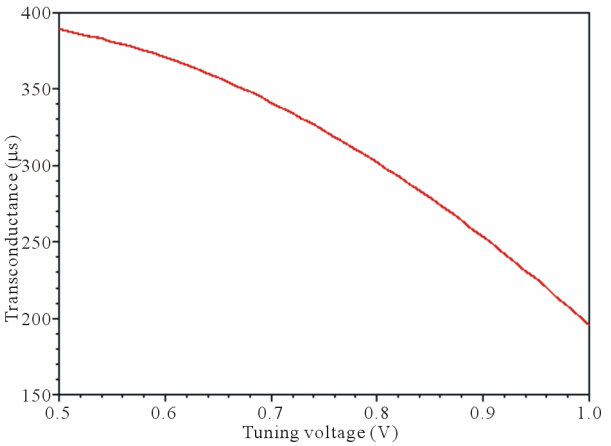

Figure 4. Transconductance (G_m) vs tuning voltage (V_{tune}) at differential signal input (v_{id}) = 0 V.

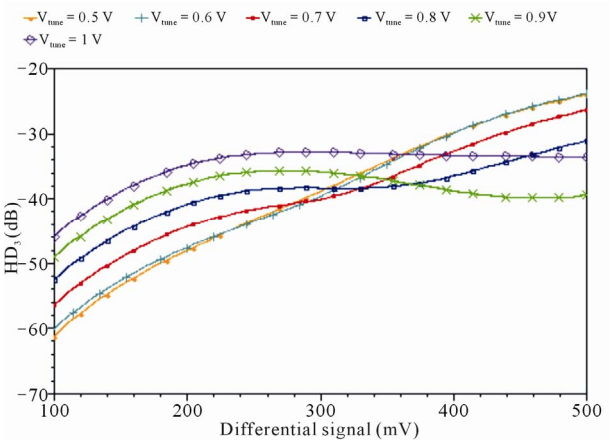

Figure 5. HD_3 vs differential signal input (v_{id}) at different tuning voltage (V_{tune}).

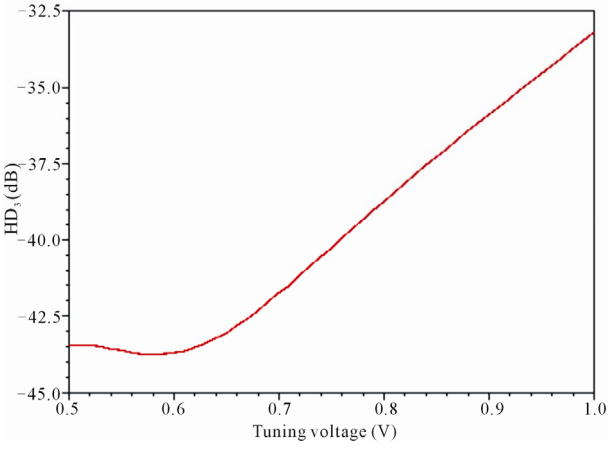

Figure 6. HD_3 vs Tuning voltage at differential signal input (v_{id}) = 0.25 V.

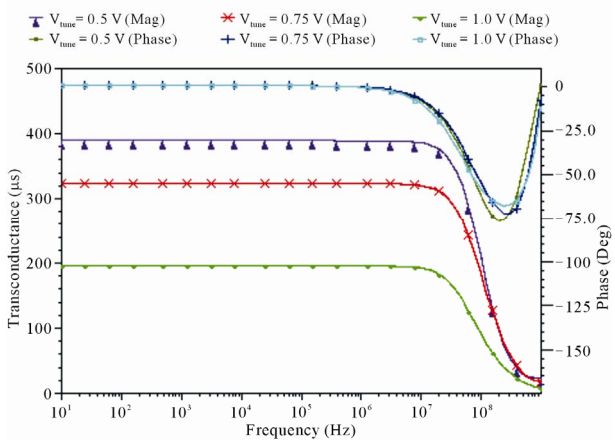

Figure 7. Transconductance vs frequency at different tuning voltage (V_{tune}).

(1.18 V^{-1}) and transconductance (390 µS) with lower harmonics (–43.7 dB), at input swing of 1 V_{p-p} @50 MHz in comparison to the others. However, the transconductance reported in [9] is higher than the proposed at the cost of high supply voltage (5 V) and very low current efficiency (0.1 V^{-1} to 0.07 V^{-1}).

4. Conclusions

A power efficient linearly tunable high G_m, cross-coupled transconductor with separate bias currents (for low third harmonic distortion) is designed and analyzed in this paper. Results have been obtained with diode mode transistors as load extendable for MOTA, which is necessary for current mode signal processing. Transconductance is varied in linear manner. G_m is tuned between 195 to 390 µS when the tuning voltage is varied from 1.0 V to 0.5 V. Maximum current efficiency of 1.18 V^{-1} and minimum HD_3 less than –43.7 dB is obtained at 1 V_{p-p} @ 50 MHz at the tuning voltage of 0.5 V. Comparative study reveals that the proposed circuit consumes low power and gives high current efficiency, with low HD_3 and high tunable transconductance for high frequency of operation compared to others.

5. Acknowledgements

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Table 1. Performance of proposed transconductor.

Performance Parameter	Simulation results		
Transconductance (G_m)	G_m = 390 µS (V_{tune}= 0.5 V)	G_m = 323 µS (V_{tune}= 0.75 V)	G_m = 195 µS (V_{tune}= 1.0 V)
(HD_3) at 1 V_{p-p}	– 43.7dB	– 40.5dB	– 33.2 dB
Power consumption (P_{diss})	0.60 mW	0.79 mW	1.20 mW
Current efficiency (G_m/I_{DD})	1.18 V^{-1}	0.74 V^{-1}	0.30 V^{-1}
3 dB Frequency	70 MHz	71 MHz	53 MHz

Table 2. Performance comparison of proposed transconductors with others.

Reference No.	[6]	[9]	[16]	[17]	[22]	[23]	Proposed
Supply voltage in V	1.8	5.0	3.3	2.5	1.8	1.8	1.8
Technology in µm	0.18	2.00	0.35	0.35	0.18	0.18	0.18
G_m in µS	8 to 131	166 to 575	160 to 340	3 to 30	110	310 to 100	390 to 195
Input Swing in V_{p-p}	1.0	1.0	1.4	1.0	0.1 – 0.9	1.0	1.0
HD_3 /THD in dB	– 40	– 40	– 70	– 42 to –50	– 27 to – 43	– 30	– 43.7
Power consumption in mW	0.58[$]	8.24 to 41.50	6.60	0.38 to 0.24	0.42[$]	0.64[$$]	0.60 to 1.20
#Current efficiency in V^{-1}	0.02 to 0.41	0.10 to 0.07	0.08 to 0.17	0.02 to 0.31	0.47	0.60	1.18 to 0.30
Frequency in MHz	10	10	26	1	50	50	50

Legend: # Calculated from the given data/average value in the references. [$]: Authors did not mention G_m at which the Power consumption values are reported. [$$]: Power at a specific G_m.

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