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Single-Stage Vernier Time-to-Digital Converter with Sub-Gate Delay Time Resolution

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Abstract

This paper presents a single-stage Vernier Time-to-Digital Converter (VTDC) that utilizes the dynamic-logic phase detector. The zero dead-zone characteristic of this phase detector allows for the single-stage VTDC to deliver sub-gate delay time resolution. The single-stage VTDC has been designed in 0.13 μm CMOS technology. The simulation results demonstrate a linear input-output characteristic for input dynamic range from 0 to 1.6 ns with a time resolution of 25 ps.

Keywords: Vernier Time-to-Digital Converter, Dynamic-Logic Phase Frequency Detector

1. Introduction

The Vernier Time-to-Digital Converter (VTDC) is a circuit that has been commonly used to provide on-chip timing measurement with fine resolution. These circuits are being implemented in PLL-based frequency synthesis systems [1,2], for on-chip PLL jitter measurement [3,4], and for time-of-flight measurement units in particle physics and medical imaging, such as Positron-Emission Tomography (PET) imaging [5]. In all these applications the adaptation of the Vernier method allows to achieve sub-gate delay time resolution. Despite this fine time resolution characteristic, the conventional VTDC still has some disadvantages due to the linear structure of the Vernier Delay Line (VDL), since the length of the VDL determines the measurement range of the VTDC. Hence, increasing the measurement range will increase the chip area and the power consumption of the circuit. Moreover, since the measurement accuracy of VTDC depends on the matching of the delay cells, the mismatches in the VDL delay cells lead to differential non-linearity (DNL) and integral non-linearity (INL) errors. Although careful layout techniques can help to minimize these mismatches, these problems cannot be completely eliminated in the design of VTDC. In order to improve the time resolution, the TDC architecture has evolved from multistage VDL [3,6] to 2-dimensional [7] and 3-dimensional [8] delay-space scheme, and to the Δ-Σ architecture [9], leading to a dramatic increase in circuit complexity. However, the increased complexity makes the circuits more susceptible to process variation. In order to eliminate the problems caused by the large structures of VDL, single-stage VTDC designs have been proposed [4]. In a single-stage VTDC circuit, the linear VDL has been replaced by a single Vernier stage that consists of two triggerable oscillators featuring different oscillation periods, T_s and T_f (**Figure 1**).

The input signals of the single-stage VTDC, START and STOP, are used to trigger oscillators. When the START signal arrives at the single-stage VTDC, the slow oscillator is triggered and starts to oscillate with a period of T_s. On the arrival of the STOP signal, the fast oscillator is activated to oscillate with a period of T_f, and the counter starts to count the number of its oscillations. After both oscillators have been triggered, the phase difference between signals ST_s and ST_f is initially equal T_{in}. Since T_f is smaller than T_s, the phase difference between ST_f and ST_s gets reduced each cycle by an oscillation period difference of $(T_s - T_f)$, and the signal edge of ST_f gradually catches up with ST_s. When these two signal edges are coincident, the phase detector signal will disable the counter. The input phase difference, T_{in}, can be determined using the following equation:

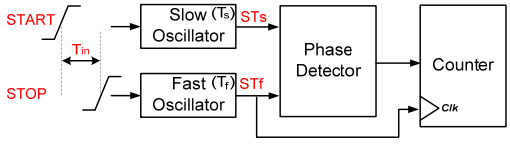

Figure 1. Concept of a single-stage Vernier Time-to-Digital Converter [4].

$$T_{in} = \left(T_s - T_f\right) \times \mathrm{CNT} \quad (1)$$

where CNT is the number of oscillation cycles counted by the counter. The performance of the single-stage VTDC surpasses the conventional VTDC in measurement accuracy, chip size, and power consumption. However, the measurement resolution of a single-stage VTDC is limited by the phase detectors' performance. The resolution of a single-stage VTDC cannot be smaller than the minimum detectable phase error of its phase detector. The measurement range of the single-stage VTDC is also limited by the detection range of the phase detector. Although the use of single-stage VTDC alleviates the component mismatch problems in the conventional VTDC, the single-stage VTDC can be still unable to achieve sub-gate delay time resolution due to the limitations of the adopted phase detector [4]. This paper presents a single-stage VTDC with a dynamic-logic phase detector that has an extended phase detection range and zero dead-zone characteristics, allowing for reliable sub-gate delay time resolution.

This paper is organized as follows. Section II describes the single-stage VTDC with classic register type phase detectors. The design details of the single-stage VTDC with a dynamic-logic phase detector proposed in this work are presented in Section III. The simulation results are in Section IV and Section V provides conclusions and a summary.

2. Single-Stage Vernier Time-to-Digital Converter with Classic Register Type Phase Detector

A single-stage VTDC is the VTDC that utilizes two triggerable oscillators with a precise oscillation frequency difference to replace the VDL in the conventional VTDC. In the previously reported implementation of the single-stage VTDC [4], the classic phase detector with two D-type registers and an AND gate has been utilized in to control the timing measurement process (**Figure 2**). The phase detector keeps track of the history of the phase difference between two oscillators and stops the measurement process once ST_f begins to lead ST_s. On the first rising ST_f edge after the rising edge of ST_s, the output of the first register Q1 goes high. On the following rising edge of ST_f, the second register keeps the value of Q1 and switches Q2 to high. When the signal edge of ST_f catches up with ST_s, the output QB1 rises and switches the output of the AND gate to generate the Phase Detected signal, as shown in **Figure 3**. The Phase Detected signal is fed to the counter where it stops the time measurement process.

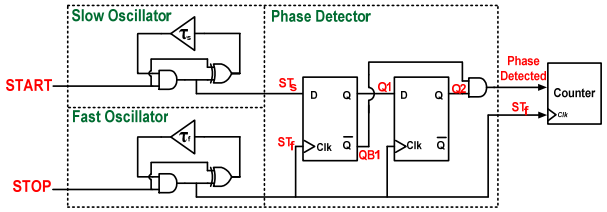

Figure 2. Single-stage VTDC with a classic two-register phase detector [4].

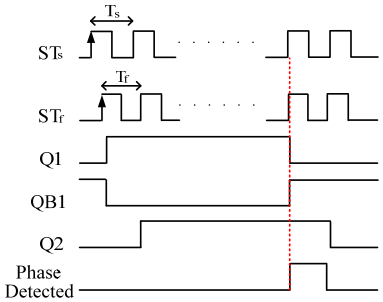

Figure 3. Timing diagram of the correct phase detection [4].

The classic two-register phase detection mechanism relies on the proper operation of D-type register. However, if the time difference between the rising edges of Clock and Data signals violates the setup time constraint of the registers, the outputs of the registers will not be correct. This problem is generally referred as meta-stability [10]. In order to prevent the meta-stability, the Data signal should be held steady for certain amount of time before the Clock event, and the minimum value of this time constraint is called a setup time. The meta-stability is likely to happen in the classic two-register phase detector, when the ST_f signal catches up with ST_s signal and the phase difference between these two signals is smaller than the required setup time. The unpredictable outputs of the registers will further cause the phase detector unable to stop the measurement process accurately. Therefore, the requirement for the non-zero setup time in the classic two-register phase detector is equivalent to the dead-zone characteristic of the phase detector. Due to the dead-zone characteristic, the single-stage VTDC designed with a classic two-register phase detector will feature a serious limitation on the time measurement resolution. The single-stage VTDC with the two-register phase detector built in 0.18 μm CMOS technology has been reported to achieve only a 54.5 ps measurement resolution [4].

Hence, it becomes evident that any further improvements in the time resolution of the single-stage VTDC would require the using of the phase detector that is not limited by the meta-stability error and thus eliminates the dead-zone in the phase detector.

3. The Single-Stage Vernier Time-to-Digital Converter with Dynamic-Logic Phase Detector

3.1. The Architecture of the Single-Stage VTDC with the Dynamic-Logic Phase Detector

The new single-stage VTDC (**Figure 4**) exploits the concept of the single-stage Vernier circuit, similar to the circuit proposed by [4]. In order to further improve the measurement resolution of the single-stage VTDC, a dynamic-logic phase detector with zero dead-zone is proposed in this work. The dynamic-logic Delayed-Input-Pulse Phase Frequency Detector (DIP-PFD) is known to have zero dead-zone and an extended detection range [11]. Therefore it is a promising candidate to improve the time measurement resolution of the VTDC. The proposed single-stage VTDC (**Figure 4**) is composed of two triggerable ring oscillators, the dynamic-logic phase detector, and the counter. The functional blocks of the single-stage VTDC are described below.

3.2. Triggerable Voltage-Controlled Ring Oscillators

The triggerable voltage-controlled ring oscillators are built similarly to the circuit proposed by [6]. However, for the simplicity, we do not use Phase-Locked Loops (PLL) to stabilize the oscillator frequencies. The triggerable ring oscillators have been designed using voltage controlled delay cells and NAND gates, as shown in **Figure 5**. Instead of generating different oscillation frequencies by using PLLs [6], the different oscillation frequencies are generated by using voltage-controlled delay cells. This solution is sufficient for the proof of the concept and also provides a degree of controllability to the time measurement resolution.

The NAND gate is used to accommodate the triggering signal, START or STOP. When the triggering signal is high, the NAND gate operates as an inverter closing the feedback loop, and creating the conditions for oscillations to take place. When the triggering signal is low, the NAND gate deactivates the feedback loop and stops the circuit from oscillating. The schematic of the triggerable voltage-controlled oscillator is shown in **Figure 6**.

The slow and fast triggerable voltage-controlled oscillators have the same architecture. The different oscillation frequencies are achieved by applying different control voltages. The control voltage of the fast oscillator is connected to the V_{DD} allowing a fast oscillation frequency. Meanwhile, the control voltage of the slow oscillator is connected to a lower externally controlled voltage, producing a slower but tunable oscillation frequency (**Figure 7**). The slow oscillator features a tunable oscillation period of 4.47 ns down to 2.61 ns that depends on the control voltage within the 0.5 V to 1.2 V range, while the fast oscillator has a steady oscillation period of 2.61 ns. In order to achieve a measurement resolution of 25 ps, the oscillation period of the slow oscillator is kept at 2.635 ns by applying the control voltage around 1.1 V.

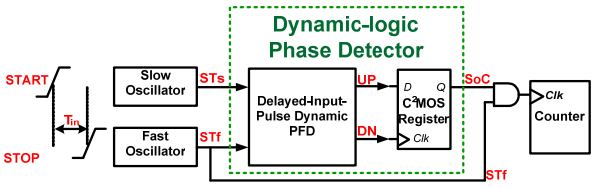

Figure 4. Single-stage VTDC with dynamic-logic phase detector.

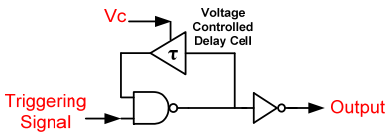

Figure 5. Concept of the triggerable voltage-controlled oscillator.

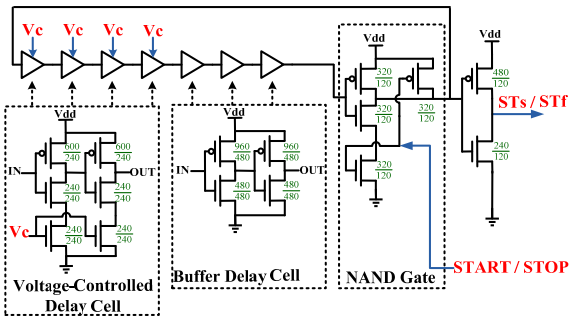

Figure 6. Schematic of the triggerable voltage-controlled oscillator.

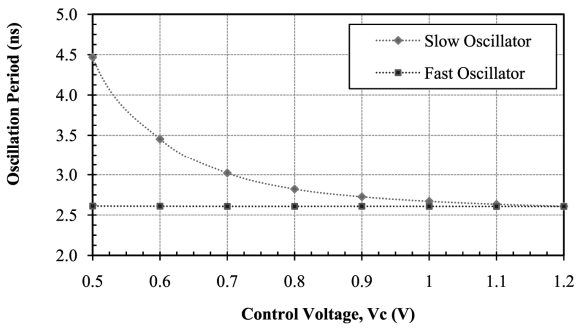

Figure 7. Oscillation periods of the voltage-controlled oscillators versus control voltage.

3.3. Dynamic-Logic Phase Detector

The dynamic-logic phase detector is a two stage phase detector constructed with a Delayed-Input-Pulse Dynamic Phase Frequency Detector (DIP-PFD) [11] followed by a C^{2}MOS register (**Figure 8**). The dynamic-logic phase detector compares the phase difference between the ST_s and the ST_f signals and generates the Start-of-Conversion signal (SoC) to control the measurement process.

The first stage of the dynamic-logic phase detector is the Delayed-Input Pulse Phase-Frequency Detector (DIP-PFD) proposed in [11]. It has been chosen because of its zero dead-zone and extended detection range characteristics. The PFD (**Figure 9**) compares the phases and frequencies of the input signals, andgenerates the UP and DN error pulses based on the phase and frequency difference between the input signals.

In this DIP-PFD, when the ST_s and ST_f signals are low, the U1 and D1 nodes are precharged high. When ST_s rises, the UPb node is discharged, producing the UP pulse. On the arrival of the rising edge of ST_f, the DNb node is pulled low, generating the DN pulse. When both outputs UP and DN are high, the U1 and D1 node will be pulled low, causing the UPb and DNb nodes to go high. This condition will deactivate the UP and DN pulses and reset the PFD. The difference in the pulse width between the UP and DN signals is therefore equal to the phase difference between ST_s and ST_f. Since the dynamic-logic PFD uses its own output signals directly to reset itself, there is virtually no dead-zone in this design. The DIP-PFD was simulated with the ring oscillators presented in the previous section. The outputs of the ring oscillators have been connected to the DIP-PFD to verify the dead-zone characteristic. The triggerable ring oscillators were triggered by two rising signal edges with a phase difference of 500 ps. The phase difference between ST_s and ST_f was gradually decreasing (by 25 ps in each oscillation cycle), finally reaching zero in the 21st cycle. The simulation result (**Figure 10**) shows that the DIP-PFD is capable of detecting phase error in a single picosecond range. This makes the DIP-PFD a good solution to eliminate the dead-zone of the phase detector in single-stage VTDCs.

The second stage of the dynamic-logic phase detector (**Figure 8**) is a C^{2}MOS register. The error signals, UP and DN, generated by the DIP-PFD are connected to a C^{2}MOS register (**Figure 11**). The register is used to sample the UP signal by the DN signal as the clock. In the case when the UP signal leads the DN signal, the C^{2}MOS register will generate SoC signal to enable the counter clock. When ST_f catches up to ST_s, the UP and DN signals will overlap each other. The Data input signal of the C^{2}MOS register will change at the same time as the Clock signal so that the output signal, SoC, will fall to deactivate the counter clock (**Figure 12**).

However, since the required setup time of the C^{2}MOS register is sensitive to process variation, the SoC signal may remain high for additional oscillation cycles. This will result a minor time offset to the time measurement. This time offset can be easily determined and removed

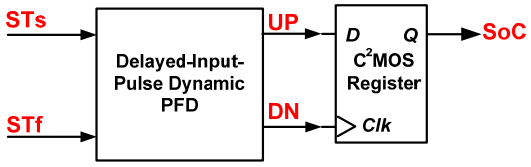

Figure 8. Dynamic-logic phase detector.

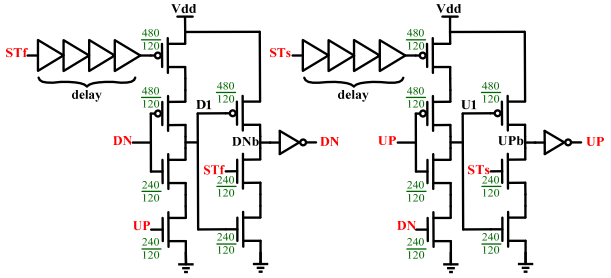

Figure 9. Delay-input-pulse phase frequency detector [11].

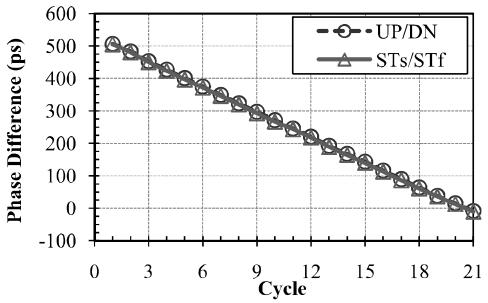

Figure 10. Zero dead-zone characteristic of the Delayed-Input-Pulse Phase Frequency Detector.

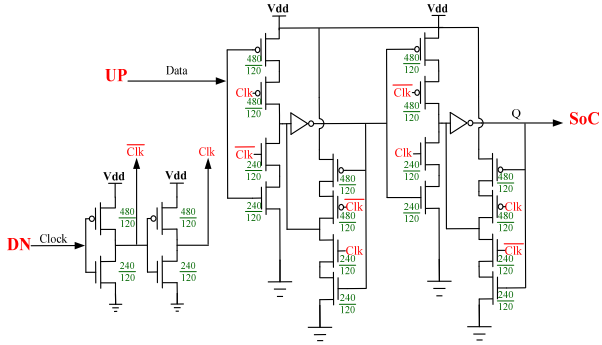

Figure 11. C^2 MOS register.

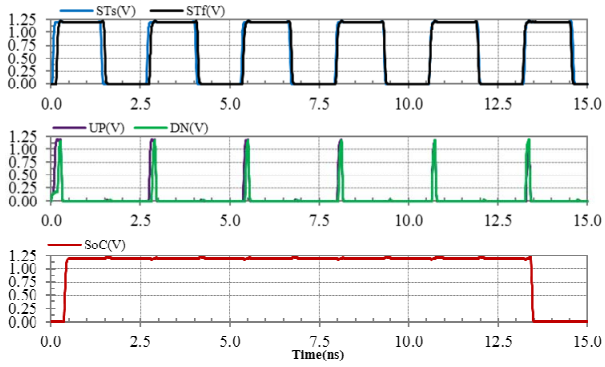

Figure 12. Timing diagram of dynamic-logic phase detector.

by measuring zero input phase difference [4]. Due to the offset, the input phase different T_{in} calculation must be modified. Taking offset into account, the measured input phase difference T_{in} is equal:

$$T_{in} = \left(T_s - T_f\right) \times \left(\mathrm{CNT} - \mathrm{offset}\right) \quad (2)$$

3.4. Counter

The SoC signal generated by the dynamic-logic phase detector controls the operation of a counter, which counts the number of cycles the measurement takes (CNT). A 6-bit counter has been designed with C^{2}MOS registers, as shown **Figure 13**. The counter is enabled by the SoC signal and clocked by the ST_f signal. Each stage of the counter divides the clock frequency signal by half. Therefore, the output signal of each register oscillates two times slower than its input clock signal. The final output signal levels [Q0:Q5] can be interpreted as the binary value of the CNT. The input phase difference, T_{in}, can be calculated with the CNT by using Equation (2).

4. Simulation Result

The single-stage VTDC with the dynamic-logic phase detector has been designed using the 0.13 μm IBM CMOS technology using the 1.2 V power supply. The **Figure 14** shows the schematic diagram of the single-stage VTDC with dynamic-logic phase detector.

The **Figure 15** shows digital output as a function of the input phase difference, simulated in the typical-typical (TT) technology corner. The control voltage has been set to 1.10V to achieve the resolution approximately 25 ps. The output characteristics of the single-stage VTDC with dynamic-logic phase detector are linear within the time range from 0 to 1600 ps. These results demonstrate that the circuit can correctly detect the phase difference and control the measurement process even at an oscillation period difference of 25 ps.

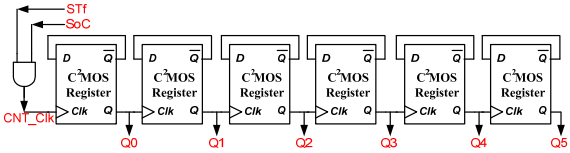

Figure 13. Block diagram of the 6-bit counter.

Next we compared the characteristics of the single-stage VTDC with the dynamic-logic phase detector with those of the single-stage VTDC with a classic register-type phase detector (**Figure 16**) implemented in the TSMC 0.35 μm CMOS as reported in [6]. The corresponding time resolution of this design was 37.5ps, and the characteristics offset estimated as 125 ps. [6]. The single-stage VTDC with the dynamic-logic phase detector has much smaller offset, in the order of 25 ps. We attribute the large offset of this VTDC [6] to the classic register-type phase detector. The offset results from a substantial dead-zone of the classic register-type phase detector, when for small phase differences (smaller than the width of the detector's dead-zone) the VTDC is unable to produce a digital output. Using the dynamic-logic phase detector clearly decreases the characteristics offset and makes measurements of small phase differences possible.

The ability to vary the VCO's oscillation frequency can be used to control the resolution of the single-stage VTDC with the dynamic-logic phase detector. Example results (**Figure 17**) show that varying the control voltage, one can achieve better resolution of the time measurements and further minimization of the offset. The increased resolution leads to a smaller input time range. Hence, the control voltage adjustment can be used for applications that require different time resolutions and input time ranges.

We also observed that without the PLL-type stabilization of the VCO, the single-stage VTDC characteristics will vary with process variations. The results presented in **Figure 18** show significant variations in time measurement resolution, and in the circuit gain and offset. To diminish this effect while keeping the circuit architecture simple, we postulate to compensate the process variations through appropriate adjustment of the control voltage, which varies the VCO oscillation frequency. The compensated results are shown in **Figure 19**, demonstrating that it is possible to obtain nearly identical output characteristics in different process corners by adjusting the control voltage. The characteristics in the TT corner (V_c = 1.10 V, **Figure 19(a)**, are almost the same as in the FF corner (but for V_c = 1.06 V, **Figure 19(b)**, and as in the SS corner (but for V_c = 1.13 V, **Figure 19(c)**. Hence, the control voltage can be used not only for setting up the parameters of the single-stage VTDC, but also for calibration if necessary.

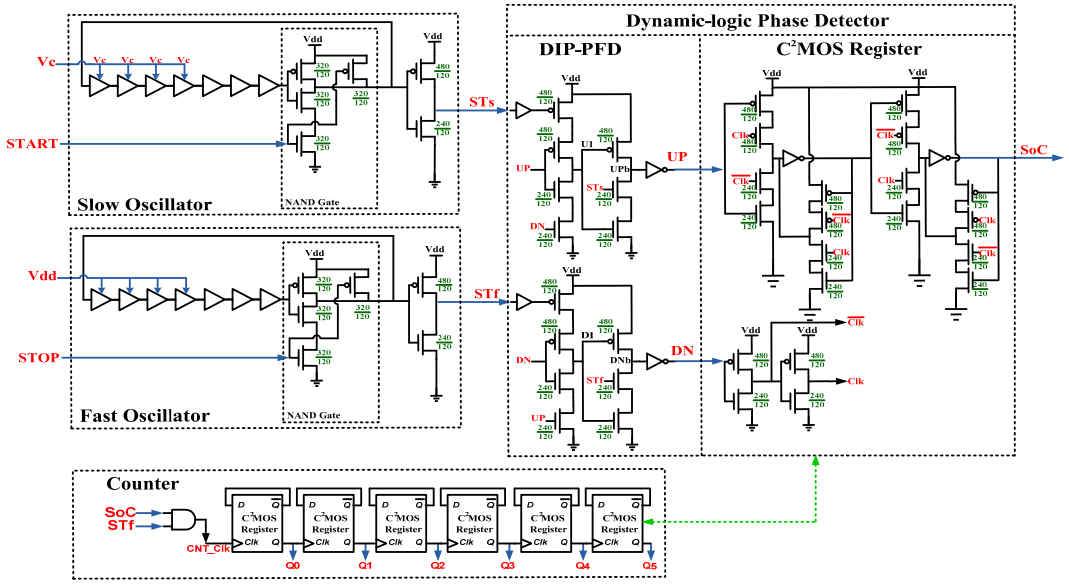

Figure 14. Schematic diagram of the single-stage VTDC.

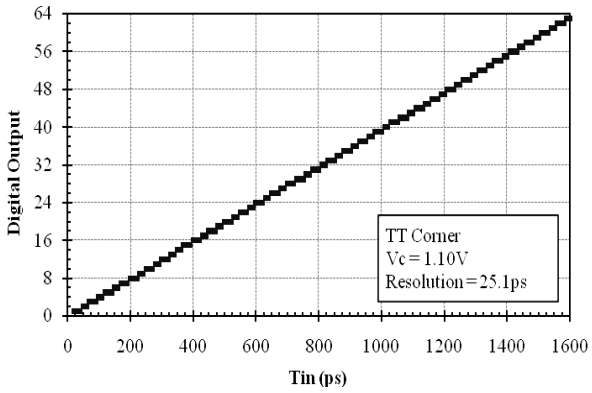

Figure 15. Digital output characteristic of the single-stage VTDC with the dynamic-logic phase detector (TT corner).

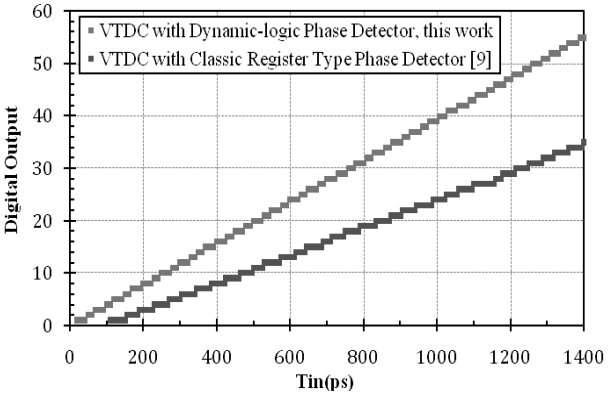

Figure 16. Comparison of the digital output characteristics of the single-stage VTDC with the dynamic-logic phase detector with the characteristics of the single-stage VTDC with the classic register-type phase detector from [6].

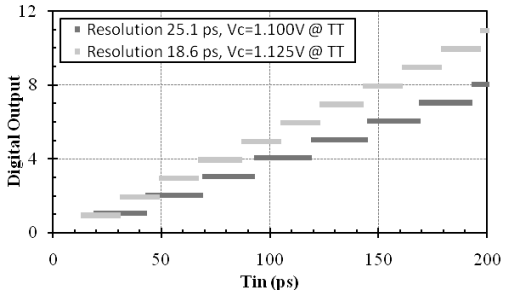

Figure 17. Digital output characteristics of the single-stage VTDC with the dynamic-logic phase detector in which the control voltage has been used to set up different time measurement resolution. Only the 0 - 200 ps fraction of the entire time scale has been shown for simplicity. (A small vertical offset in the digital output has been introduced for better readability).

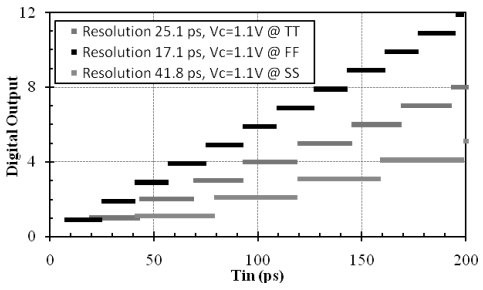

Figure 18. Variability of the digital output characteristics of the single-stage VTDC with the dynamic-logic phase detector as a function of process variations (in the TT, FF, and SS process corners), for a constant control voltage, V_c = 1.10 V. Only the 0 - 200 ps fraction of the time scale has been shown for simplicity. (A small vertical offset in the digital output has been introduced for better readability).

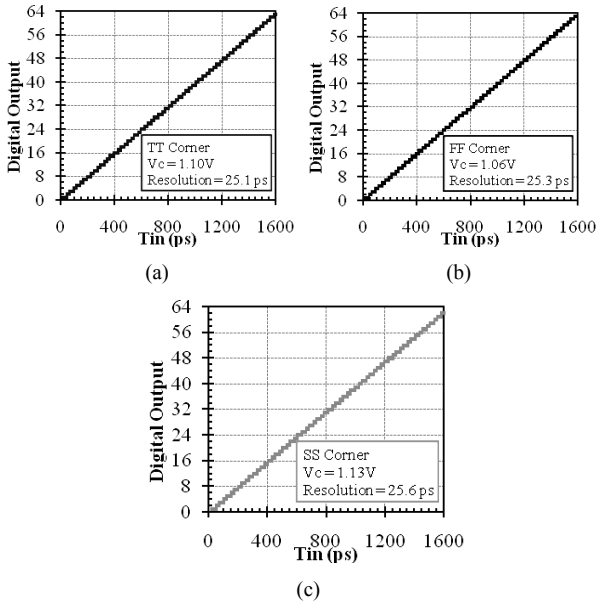

Figure 19. Digital output characteristics of the single-stage VTDC with the dynamic-logic phase detector in the different process corners compensated using different values of the control voltage (a) TT corner V_c = 1.10 V; (b) FF corner, V_c = 1.06V; (c) SS corner, V_c = 1.13 V.

5. Conclusions

This paper presents a single-stage Vernier Time-to-Digital Converter with sub-gate delay time resolution. By utilizing the dynamic-logic phase detector that eliminates the dead-zone problem, the single-stage Vernier Time-to-Digital Converter in this work has demonstrated a linear digital output characteristic with a 25 ps time resolution. The presented simulation results have confirmed the very important role of the phase detector quality for the performance of single-stage Vernier Time-to-Digital Converters with sub-gate delay resolutions.

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