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Integrated Off-Line Ballast for High Brightness LEDs with Dimming Capability

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Abstract

This paper presents an off-line integrated full ballast to supply a 35 W assembly of Power LEDs. The proposed solution integrates an input PFC stage (a flyback converter operating in DCM) and a DC-DC output converter (a buck converter) into a single switch power stage, operating with peak current control. As it will be shown, this control scheme maintains the current through the load constant, regardless of the instantaneous value of the DC link voltage. This issue allows the use of a small capacitor for the DC link, which enhances the overall system reliability. The complete ballast has full dimming capability, and all the analysis and design steps are presented, thus ensuring the fulfilling of the existing regulations. The novelty of the final solution comes from the simplicity and robustness of the control scheme in an integrated compact single-switch power stage. A final prototype of the ballast has been built and tested, and experimental results are shown in the last part of the paper. Finally, conclusions and future developments are shown.

Keywords: High Brightness LEDs, Light Dimming, Electrolytic Capacitor Avoidance, Integration of Stages

1. Introduction

At present, significant efforts are being performed in the development of lighting electronic systems, as one of the major research fields related to energy savings and sustainable development. Among other causes, this is due to the continuous improvement of High Brightness (HB) and Power LEDs as outstanding light sources [1-8]. In fact, these devices exhibit a continuous increase in its luminous efficiency and a high operating life and reliability. These features turn them the preferred device for an increasing number of applications [5-8].

Both the thermal and electrical behaviors of such devices make necessary the use of drivers with current limiting capability, in order to achieve stable operation The most efficient approach for this driver is the use of multi-stage Switch-Mode Power Supplies (SMPS) [9-19]. **Figure 1** shows a typical block diagram of such a driver supplied from AC mains.

The overall components count of such drivers is relatively high, due the number of stages. Moreover, this scheme implies the use of a low ripple voltage DC link after the input Power Factor Correction (PFC) stage, commonly provided by an electrolytic capacitor. As these devices have a relatively small operating life, it penalizes the overall life span of the system [2,20-22].

In this paper, a novel complete integrated electronic dimmer for Power LEDs is presented to overcome these drawbacks. The input stage of the proposed design operates from AC mains and delivers energy to a DC bus. The output stage with the proposed peak current control provides a DC current to the assembly of LEDs, regardless of the DC bus voltage. Thus, the DC bus voltage ripple can be significantly high, so the electrolytic capacitor can be removed and substituted by a small capacitance device. Provided that both power stages are single-switch topologies, the integration of the circuitry can be explored as an optimization strategy. As it will be shown in the present work, this integration is feasible, yielding to a final electronic driver with a single con

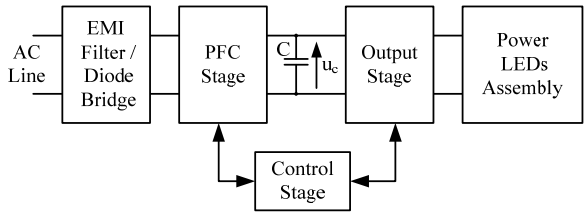


Figure 1. Block diagram of an offline electronic driver for Power LEDs.

trolled switch, presenting a block diagram as the one shown in **Figure 2**. The proposed solution allows the use of a simple and reliable control method, particularly effective in a circuit that avoids the use of electrolytic capacitors [21,22]. This simplicity and robustness, along with the compact scheme inherent to integrated power stages, provides a new feasible solution for power LEDs drivers.

In addition, light dimming can also be studied as a key issue of the full ballast. The most used diming schemes, AM and PWM dimming, will be investigated applied to the resulting integrated topology. As it will be shown, AM dimming can be attained by simply changing the peak control reference, while PWM dimming can be carried out by modulating the HF switching scheme of the integrated switch.

This paper analyzes more deeply the basic scheme presented in [22]. The effects of the integration in both the waveforms and the size of the power switches is considered. A revised design procedure is presented, and the design implications considering universal input line voltage condition are also presented. Both PWM and AM dimming schemes are also discussed in this paper.

The paper is organized as follows. Section 2 takes care of the power stage and the control strategy of the output converter. Later, Section 3 deals with the input PFC stage. Section 4 covers the topics related with the integration of stages and the design constraints, as well as with the effects on the input Power Factor (PF) and current harmonics. After that, Section 5 summarizes a design procedure for the full power operation of the driver. Section 6 deals with the experimental setup for the full power nominal operation of a built prototype, while section 7 takes care of both AM and PWM dimming procedures for the proposed topology. A final discussion on the extension of the design for universal AC input voltage is carried out in Section 8, while Section 9 comments on the conclusions and future developments of this work.

2. The Output Stage

Figure 3 shows the output stage, used in the full ballast

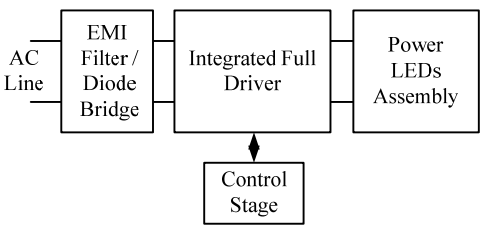


Figure 2. Block diagram of an integrated electronic driver for Power LEDs.

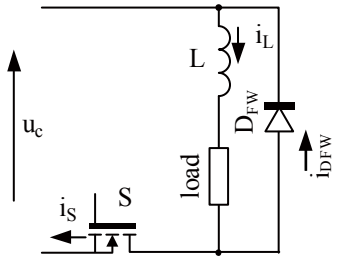


Figure 3. Scheme of the output stage

presented in [21]. It is a reverse buck converter stage, but removing the output filter capacitor. The final circuit is formed by the inductor L, the freewheeling diode D_{FW} and the controlled switch S. As it is shown, the current through the LEDs (modeled by the block called 'load') is the inductor current. Thus, ensuring a low AC ripple at the inductor current guarantees a proper current waveform to supply the LEDs.

2.1. The Power Stage

The operation of the converter is the same than in the usual buck converter. Although the output capacitor has been removed, the equivalent output characteristic of the LEDs assembly [23], resembles a voltage source, and thus the charging and discharging subintervals of the inductor can be considered at constant voltage [21,22]. This issue allows the usual analysis of the operation of the buck converter.

Thus, the expression of the inductor current, considering Continuous Conduction Mode (CCM), can be calculated as:

$$i_L(t) = \begin{cases} i_0 + \dfrac{u_C - u_{LEDs}}{L} \cdot t & 0 \le t < T_{ON} \\ i_{MAX} - \dfrac{u_{LEDs}}{L} \cdot (t - T_{ON}) & T_{ON} \le t < T \end{cases} \quad (1)$$

where i_0 and i_{MAX} are the initial and peak value of the inductor current, respectively, u_C is the input voltage, u_{LEDs} is the output voltage, L is the inductance, and T_{ON} and T are the turn-on time and the switching period of the switch S, respectively.

Obviously, the static gain expression of this converter can be defined as:

$$\frac{V_{out}}{V_{in}} = \frac{u_{LEDs}}{u_C} = \frac{T_{ON}}{T} = d \quad (2)$$

where d is the duty ratio of the converter.

Figure 4 shows the main theoretical waveforms of this converter.

Also, the current through the switch S, i_S, can be easily calculated:

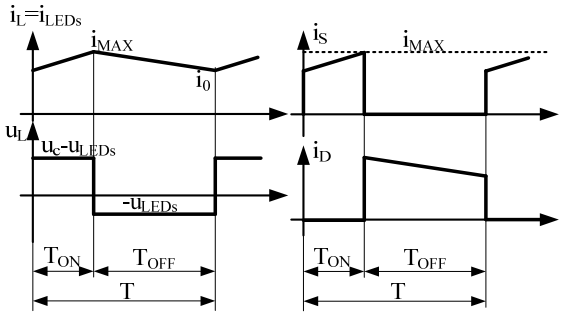


Figure 4. Main waveforms at the buck converter.

$$i_S(t)=\begin{cases} i_0+\dfrac{u_C-u_{LEDs}}{L}\cdot t & 0\le t<T_{ON} \\ 0 & T_{ON}\le t<T \end{cases} \tag{3}$$

The average value of this input current in one high frequency switching period, i_{SAVG}, can be obtained from (3):

$$i_{SAVG}=\frac{i_0+i_{MAX}}{2}\cdot d \tag{4}$$

2.2. The Control Stage

Different control strategies can be implemented to drive this stage. In order to supply properly the LEDs, an output current control mode must be considered. The proposed control method fixes the maximum current through the switch and the turn-off time of the switch, T_{OFF}. Obviously,

$$T=T_{ON}+T_{OFF} \tag{5}$$

Considering (1) and (5), if T_{OFF} and I_{MAX} are fixed, the value of the current i_0, and hence that of the current ripple through the LEDs, Δi_{LEDs}, is also fixed:

$$i_{MAX}-i_0=\Delta i_{LEDs}=\frac{u_{LEDs}}{L}\cdot T_{OFF} \tag{6}$$

Thus, the i_{MAX} - T_{OFF} control ensures a maximum peak current value through the LEDs as well as a fixed current ripple through the LEDs. Notice how this assertion is true whatever the voltage u_C is present (provided that u_C is greater than u_{LEDs}, and hence the inductor can be charged during T_{ON}). That is to say, for every value of u_C greater than u_{LEDs}, the control ensures a current waveform of a fixed maximum value and ripple.

Another consequence of this control is that the turn-on time of the switch, T_{ON}, is not an independent variable of the system for the selected control scheme. From (2) and (5), T_{ON} can be expressed as:

$$T_{ON}=\frac{u_{LEDs}}{u_C-u_{LEDs}}\cdot T_{OFF} \tag{7}$$

Thus, T_{ON} depends on the input voltage, u_C, and hence the switching frequency of the converter also depends on u_C:

$$f=\frac{1}{T}=\frac{1}{T_{ON}+T_{OFF}}=\frac{u_C-u_{LEDs}}{u_C\cdot T_{OFF}} \tag{8}$$

In order to define the operation of the complete system it is interesting to express the average input current as a function of the input and output voltages as well as of the control parameters. From (4), (6) and (7), the expression of the average input current, i_{SAVG}, can be rewritten as a function of i_{MAX}, T_{OFF} and u_C, yielding to:

$$i_{SAVG}=\frac{2\cdot i_{MAX}-\dfrac{u_{LEDs}}{L}\cdot T_{OFF}}{2}\cdot\frac{u_{LEDs}}{u_C} \tag{9}$$

So finally, it can be seen how the average input current is also a function of u_C.

3. The Input Stage

The input PFC stage is a flyback converter, operating in Discontinuous Conduction Mode (DCM). The schematic diagram of this stage is shown in **Figure 5**. Prior to the integration of both stages, an analysis of the main waveforms must be carried out. The current flowing through the magnetizing inductor at the primary side of the flyback transformer, i_{LF}, can be expressed as:

$$i_{LF}(t)=\begin{cases} \dfrac{V_{INPK}\cdot|\sin(\theta)|}{L_F}\cdot t & 0\le t<T_{ONF} \\ i_{LFPK}-\dfrac{N_P}{N_S}\dfrac{u_C}{L_F}\cdot(t-T_{ONF}) & T_{ONF}\le t<T_{ONF}+T_d \\ 0 & T_{ONF}+T_d\le t<T_F \end{cases} \tag{10}$$

where $V_{INPK}\cdot\sin(\theta)$ is the line input voltage, considered constant during the switching period of the flyback stage, T_F; L_F is the magnetizing inductance at the primary side of the transformer; N_P and N_S are the turns ratio at the primary and secondary side of the transformer, respectively;

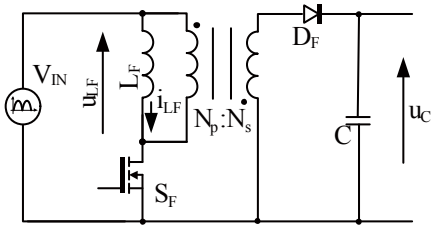


Figure 5. Schematics of the flyback input stage.

T_{ONF} is the interval during which the switch S_F is turned on, T_d is the demagnetizing time of L_F, u_C is the output voltage of this stage, and i_{LFPK} is the peak value of the current through the magnetizing inductor. This value can be described as:

$$i_{LFPK} = \frac{V_{INPK} \cdot \left|\sin(\theta)\right|}{L_F} \cdot T_{ONF} \tag{11}$$

Figure 6 depicts the voltage and current waveforms in the magnetizing inductor at the primary side of the transformer.

On the other hand, the instant current waveform, i_{IN}, at the input (line input current) can be easily obtained considering (10):

$$i_{IN}(t,\theta) = \begin{cases} \dfrac{V_{INPK} \cdot \left|\sin(\theta)\right|}{L_F} \cdot t & 0 \le t < T_{ONF} \\ 0 & T_{ONF} \le t < T_F \end{cases} \tag{12}$$

The average value of this input current in a switching period, i_{INAVG}, can be calculated as:

$$i_{INAVG}(\theta) = \frac{V_{INPK} \cdot \left|\sin(\theta)\right| \cdot {T_{ONF}}^2}{L_F \cdot T_F \cdot 2} \tag{13}$$

The current in the secondary side of the transformer, that is to say, the forward current of the diode D_F, can be expressed by (14):

The demagnetizing time, T_d, can be expressed from (14):

$$T_d = \frac{V_{INPK} \cdot \left|\sin(\theta)\right|}{u_C} \cdot T_{ONF} \cdot \frac{N_S}{N_P} \tag{15}$$

Thus, the average value of the output current in a switching period, i_{DFAVG}, can be calculated as:

$$i_{DFAVG} = \frac{V_{INPK} \cdot \left|\sin(\theta)\right|}{2 \cdot L_F} \cdot \frac{N_P}{N_S} \cdot T_{ONF} \cdot \frac{T_d}{T_F} \tag{16}$$

From (15) and (16), this expression can be calculated as:

$$i_{DFAVG} = \frac{{V_{INPK}}^2 \cdot \sin^2(\theta)}{2 \cdot L_F \cdot u_C} \cdot \frac{{T_{ONF}}^2}{T_F} \tag{17}$$

4. Dealing with the Integration

Figure 7 depicts the resulting full ballast, with the proposed stages connected in series. Each stage has a controlled switch, represented by a MOSFET, with its source terminal connected to ground. The integration can be carried out by equaling the switching periods of both stages and their turn-on times:

$$T_{ONF} = T_{ON};\ T_F = T \tag{18}$$

A scheme of the final ballast can be seen in **Figure 8**, while **Figure 9** depicts the switching intervals of the integrated ballast operation. When the integrated switch, S_{INT}, is turned on (T_{ON}), the input current charges the magnetizing inductance of the primary side of the transformer (**Figure 9(a)**). At the same time, the capacitor C provides the current that flows through the inductor L and through the load in the output converter. This interval corresponds to the turn-on intervals of the input and output stages.

After the current through inductor reaches i_{MAX}, S_{INT} is turned off. The magnetizing inductance at the primary side of the flyback transformer discharges through D_F towards the capacitor (**Figure 9(b)**). Also, the freewheeling diode D_{FW} turns on, thus discharging L through the load. At a certain time after being started, the demagnetizing of the flyback transformer ends up, and the diode D_F turns off again (**Figure 9(c)**). Nevertheless, the output stage remains unchanged.

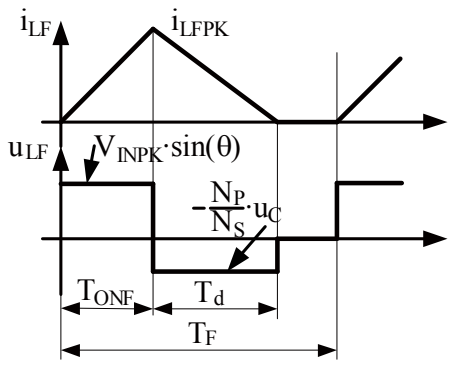


Figure 6. Main waveforms in the magnetizing inductor at the primary side of the transformer of the input stage.

$$i_{DF}(t) = \begin{cases} 0 & 0 \le t < T_{ONF} \\ i_{LFPK} \cdot \dfrac{N_P}{N_S} - \dfrac{{N_P}^2}{{N_S}^2} \cdot \dfrac{u_C}{L_F} \cdot (t - T_{ONF}) & T_{ONF} \le t < T_{ONF} + T_d \\ 0 & T_{ONF} + T_d \le t < T_F \end{cases} \tag{14}$$

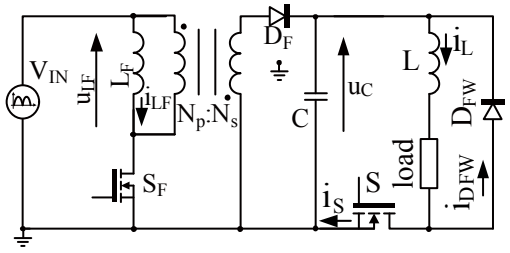


Figure 7. Full ballast with the proposed stages.

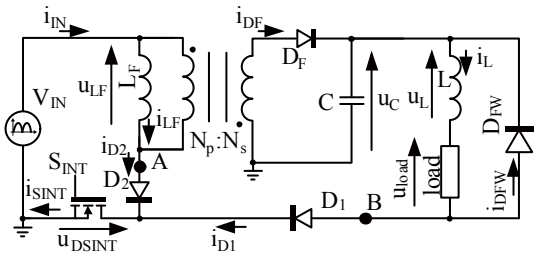


Figure 8. Full ballast with the integration of the stages.

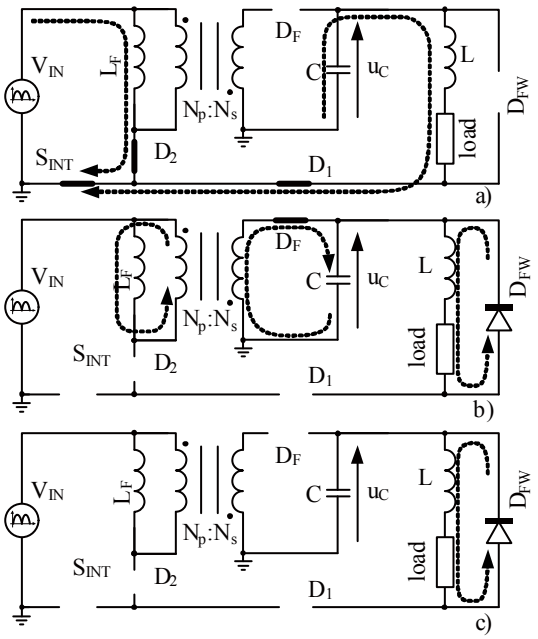


Figure 9. Switching modes of the integrated proposed driver.

In order to dimension the switches of the proposed topology, a study of the obtained waveforms has been carried out, taking into account the requirements for the new semiconductors after the integration, S_{INT}, D_1 and D_2.

From the point of view of the current stresses, **Figure 9(a)** shows how the current flowing through S_{INT} is the sum of the input switch (S in **Figure 7**) and output switch (S_F in **Figure 7**) currents. Provided that the operation of the independent stages is the one previously discussed (**Figures 3** and **6**), the main current waveforms of the proposed topology are depicted in **Figure 10**. In fact, as it can be seen, the peak current trough S_{INT}, i_{SINTPK}, is the sum of both peak currents:

$$i_{SINTPK} = i_{MAX} + i_{LFPK} \tag{19}$$

The current waveform through diode D_1 is the same current waveform obtained for the input switch (S in **Figure 7**), whereas the current through D_2 is the one obtained for the output switch (S_F in **Figure 7**). The currents through the rest of devices are the same that were obtained at the analysis of the input and output independent stages.

The analysis of the voltage waveforms is not so easy, as the voltage waveforms in D_1 and D_2 change depending on the relative value of the line instant voltage and the capacitor voltage, which in turn depends on the turns ratio, N_P/N_S. In order to simplify the study, it is assumed that:

$$N_P > N_S \tag{20}$$

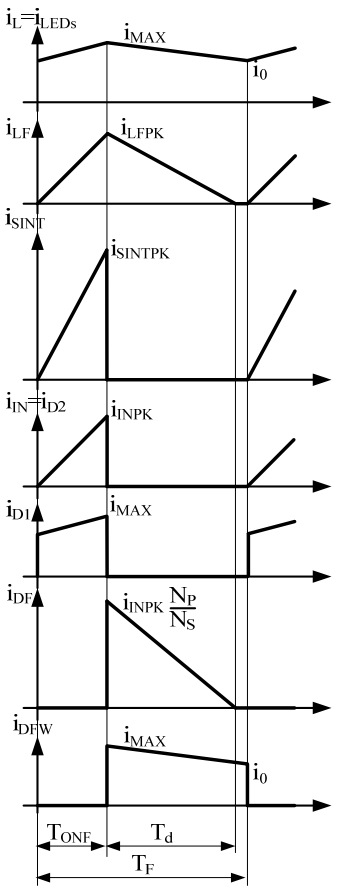


Figure 10. Main current waveforms at the proposed topology.

This assumption will be justified later, in the design section. Depending on these relative values, two different conditions of the input line voltage are present.

4.1. Relative Values of V_A and V_B during the Demagnetization Interval

When S_{INT} is turned on, D_1 and D_2 are forward biased, and no voltage requirement is obtained. However, once the main switch is turned off, the resulting waveforms depend on the line instant angle, θ.

While the flyback rectifying diode, D_F, is directly biased, the voltage at the anode of D_2 (point A in **Figure 8**) is defined by:

$$V_A = V_{INPK} \cdot \left|\sin(\theta)\right| + \frac{N_P}{N_S} \cdot u_C \tag{21}$$

On the other hand, the voltage at the anode of D_1 (point *B* in **Figure 8**), can be expressed by:

$$V_B = u_C \tag{22}$$

as the diode D_{FW} is directly biased, and thus withstands no voltage. Considering (20), (21) and (22), the relative values of V_A and V_B yield to:

$$V_A = V_{INPK} \cdot \left|\sin(\theta)\right| + \frac{N_P}{N_S} u_C > u_C = V_B \Rightarrow V_A > V_B \tag{23}$$

This condition reversely biases the diode D_1, which withstands the following voltage:

$$V_{D1AK} = V_{INPK} \cdot \left|\sin(\theta)\right| + \left(\frac{N_P}{N_S} - 1\right) u_C \tag{24}$$

On the other hand, diode D_2 is directly biased, but with no current passing through. Provided that (20) is fulfilled, this condition is satisfied for every line instant.

4.2. Relative Values of V_A and V_B after the Demagnetization Interval

Once the demagnetization of the magnetizing inductance L_F ends up, the value of V_B is still represented by (22), but diode D_F turns off, and the voltage at node *A* changes yielding to:

$$V_A = V_{INPK} \cdot \left|\sin(\theta)\right| \tag{25}$$

Now, the relative values of V_A and V_B depend on the line input voltage instant. In fact, at high instant input voltage values, the following equation if fulfilled:

$$V_{INPK} \cdot \left|\sin(\theta)\right| > u_C \tag{26}$$

what yields again to the condition

$$V_A > V_B \tag{27}$$

and diodes D_1 and D_2 remain as in the previous stage.

However, for low instant input voltage (near the zero crossing of the line voltage), the following equation is eventually satisfied:

$$V_{INPK} \cdot \left|\sin(\theta)\right| < u_C \tag{28}$$

what yields to the opposite condition:

$$V_A < V_B \tag{29}$$

In this case, this condition reversely biases D_2, that withstands a voltage given by:

$$V_{D1AK} = u_C - V_{INPK} \cdot \sin(\theta) \tag{30}$$

In this case, D_1 remains directly biased but without driving forward current.

Thus, depending of the relative values of the instant line rectified input voltage and the capacitor voltage, the state of the diodes D_1 and D_2 change. **Figure 11(a)** depicts the voltage waveforms for high instant line voltage, given by (26), while **Figure 11(b)** shows the voltage waveforms for the alternate low instant line voltage condition, defined by (28).

The value of this capacitor, *C*, is the key parameter of the operation of the converter. This capacitance fixes the DC link voltage instant waveform. As the flyback input current is a function of this DC link voltage, the line input current depends also on the capacitance *C*. Thus, to properly design the ballast, the waveform of the capacitor voltage, as a function of the capacitance *C*, must be calculated. The average current in a switching period flowing into the capacitor *C* can be calculated. As can be seen, the input current of the capacitor is the output current of the input stage, and the output current of the capacitor is the input current through the output stage.

$$i_{CAVG} = i_{DFAVG} - i_{SAVG} \tag{31}$$

Thus, from (9), (17) and (31): (32)

Considering (5) and (18), this current can be expressed as a function of the control parameters, i_{MAX} and T_{OFF} (33)

$$i_{CAVG} = \frac{{V_{INPK}}^2 \cdot \sin^2(\theta)}{2 \cdot L_F \cdot u_C} \cdot \frac{{T_{ONF}}^2}{T_F} - \frac{2 \cdot i_{MAX} - \frac{u_{LEDs}}{L} \cdot T_{OFF}}{2} \cdot \frac{u_{LEDs}}{u_C} \tag{32}$$

$$i_{CAVG} = \frac{{V_{INPK}}^2 \cdot \sin^2(\theta) \cdot {u_{LEDs}}^2}{2 \cdot L_F \cdot {u_C}^2 \cdot (u_C - u_{LEDs})} T_{OFF} - \frac{u_{LEDs}}{u_C}\left(i_{MAX} - \frac{u_{LEDs}}{2 \cdot L} \cdot T_{OFF}\right) \tag{33}$$

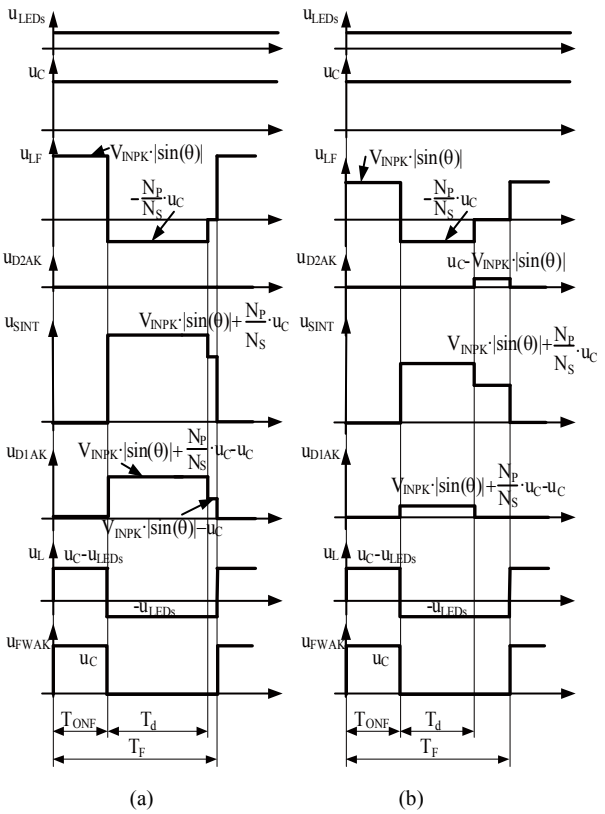


Figure 11. Main voltage waveforms at the proposed topology. (a) High line instant input voltage condition. (b) Low line instant voltage condition.

The fundamental equation of a capacitor, combined with (33), yield to: (34)

This differential equation must be solved numerically. The time expression of the capacitor voltage can be solved as a function of the control parameters, i_{MAX} and T_{OFF}, and the capacitance C:

$$u_C(\theta) = f(\theta, i_{MAX}, T_{OFF}, C) \tag{35}$$

After the integration, the expression of the input line current as a function of the line angle can be expressed from (2), (8) and (13) as: (36)

Finally, substituting (35) in (36), the final expression of the input current value is found, what yields to the calculation of both the power factor and the input current harmonics.

5. Design Procedure for 115 V_{RMS}-60 Hz Line Voltage

This section proposes the design procedure for a LED driver, calculating the input current harmonics to verify if they fulfill the corresponding regulations. In a first approach ideal components will be considered.

The selected input is the American input mains voltage range, 115 V_{RMS}-60 Hz, and an allowed variation of ±20% in the amplitude will be considered. At the final part of this section, once the rest of the components are designed, the rated voltage and current values of the main switches will be selected for this input condition. This will yield to a proper sizing of these devices. An additional discussion at the final part of the paper will consider the Universal input mains voltage range, and its effects on the design procedure.

5.1. Desired Operation Parameters

The first thing to settle is the target load and its nominal operation point. In this case, a 32 W assembly of Power LEDs will be the target load. The selected device is the Luxeon LXK2-PW14-U00, from Lumileds Lighting [23]. To obtain such a power load, the selected assembly is formed by the series connection of 10 LEDs. In previous works, it has been demonstrated how the proposed control scheme allows a proper operation of the system, regardless the evolution of the electric and thermal parameters of the LEDs [21].

Thus, the rated electrical parameters of this load are:

$$P_{LEDs} = 32\ \text{W} \quad u_{LEDs} = 32\ \text{V} \quad i_{LEDs} = 1\ \text{A} \tag{37}$$

where u_{LEDs} is the total voltage drop of the assembly of LEDs.

The design current ripple has been selected as:

$$\Delta i_{LEDs} = i_{MAX} - i_0 = 0.1\ \text{A} = 10\% \tag{38}$$

and, in order to keep the average forward value selected in (37), the values of i_{MAX} and i_0 are:

$$i_{MAX} = i_{LEDs} + \frac{\Delta i_{LEDs}}{2} = 1.05\ \text{A} \tag{39}$$

$$i_0 = i_{LEDs} - \frac{\Delta i_{LEDs}}{2} = 0.95\ \text{A} \tag{40}$$

$$2\pi f_L C \cdot \frac{\mathrm{d}u_C}{\mathrm{d}\theta} = \frac{{V_{INPK}}^2 \cdot \sin^2(\theta) \cdot {u_{LEDs}}^2}{2 \cdot L_F \cdot {u_C}^2 (u_C - u_{LEDs})} T_{OFF} - \frac{u_{LEDs}\left(i_{MAX} - \frac{u_{LEDs} \cdot T_{OFF}}{2 \cdot L}\right)}{u_C} \tag{34}$$

$$i_{INAVG}(\theta) = \frac{V_{INPK} \cdot |\sin(\theta)| \cdot {T_{ON}}^2}{L_F \cdot T_F \cdot 2} = \frac{V_{INPK} \cdot |\sin(\theta)| \cdot {u_{LEDs}}^2 \cdot T_{OFF}}{2 \cdot L_F \cdot u_C(\theta) \cdot (u_C(\theta) - u_{LEDs})} \tag{36}$$

As described in previous sections, the values of T_{ON}, and hence of T and d, are a function of θ. Nevertheless, the averaged values of these parameters must be settled in order to start the design. Thus, the selected average switching frequency will be 100 kHz, whereas the target duty ratio will be 50%:

$$f = 100 \text{ kHz} \quad T = 10 \text{ µs} \quad T_{OFF} = 5 \text{ µs} \tag{41}$$

With these initial design parameters, the values of the rest of the circuit parameters can be calculated.

5.2. Calculation of the Magnetic Components

The value of the inductor at the output stage can be obtained from (6):

$$L = \frac{u_{LEDs}}{\Delta i_{LEDs}} \cdot T_{OFF} = 1.67 \text{ mH} \tag{42}$$

Although this inductance is high, it must be noticed that the current ripple through the inductor will be very low. This condition makes possible the design optimization of the magnetic device, thus maintaining low enough the power losses in this component.

The flyback transformer must now be calculated. To ensure the DCM, the demagnetizing time of the transformer, T_d, must fulfill:

$$T_d \le T_{OFF} \tag{43}$$

From (15) and (43), the limit value of the turns ratio, N_P/N_S, that keeps DCM condition can be obtained:

$$\frac{N_P}{N_S} \ge \frac{T_{ON}(\theta)}{T_{OFF}} \cdot \frac{V_{INPK} \cdot \left|\sin(\theta)\right|}{u_C(\theta)} \tag{44}$$

Taking into account (7),

$$\frac{N_P}{N_S} \ge \frac{u_{LEDs}}{u_C(\theta) - u_{LEDs}} \cdot \frac{V_{INPK} \cdot \sin(\theta)}{u_C(\theta)} \tag{45}$$

Notice how in (44) and (45) the V_{INPK} value is the highest possible. For instance, considering the ±20% input line variation, in this case a 120% of V_{INPK} should be selected.

It can also be seen how prior to settle the turns ratio of the transformer, the limit values of u_C must be calculated. Nevertheless, the magnetizing inductance at the primary side of the transformer can be calculated considering the equation that expresses the average input power in a switching period. Considering (36), the instant input power as a function of the line angle, θ, can be calculated as:

$$P_{IN}(\theta) = \frac{{V_{INPK}}^2 \cdot \sin^2(\theta) \cdot {T_{ON}}^2}{2 \cdot L_F \cdot T} \tag{46}$$

And finally, the average input power in a line period can be obtained:

$$P_{IN-AVG} = \frac{{V_{INPK}}^2 \cdot {T_{ON}}^2}{4 \cdot L_F \cdot T} \tag{47}$$

If an efficiency of η is considered, the maximum allowable value of the input inductor can be solved:

$$P_{IN-AVG} = P_{LEDs} \cdot \eta \quad \Rightarrow \quad L_F \le \frac{{V_{INPK}}^2 \cdot {T_{ON}}^2}{4 \cdot P_{LEDs} \cdot \eta \cdot T} \tag{48}$$

In this case V_{INPK} value must be the smallest possible. For the aforementioned specification of ±20% input voltage variation, now a 80% of V_{INPK} should be selected.

From (41) and (48), and considering η = 0.85, the magnetizing inductor L_F is: (43)

$$L_F \le 425 \text{ µH} \quad \Rightarrow \quad L_F = 420 \text{ µH} \tag{49}$$

5.3. Solution of the Equation of the Capacitor Voltage

Equation (34) has been solved numerically for different capacitor values. The obtained voltage waveforms at the capacitor, u_C, have been plotted in **Figure 12**.

After analyzing the value of $u_C(\theta)$, it has been verified that the minimum value of C that allows a correct operation of the system is:

$$C_{MIN} = 18 \text{ µF} \tag{50}$$

For lower values, $u_C(\theta)$ reaches voltage values smaller than u_{LEDs}, which would imply negative currents through the LEDs (obviously an impossible condition). For greater capacitance values, the system operates properly, and the larger the C value, the smaller the DC link voltage ripple, as shown in **Figure 12**.

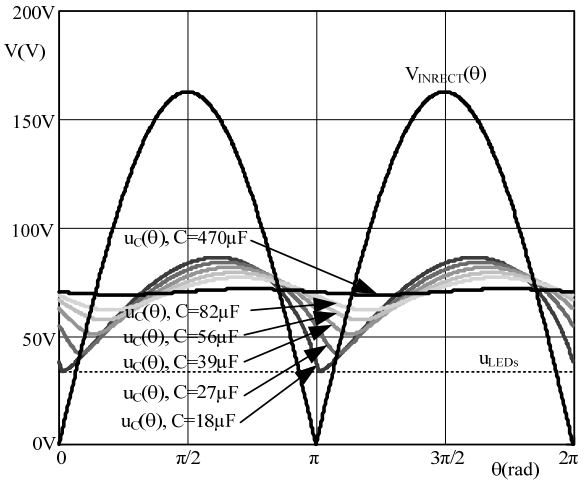


Figure 12. Theoretical waveforms of the capacitor voltage, u_C, as a function of different capacitance values.

Although the output stage will operate properly for capacitance values greater than C_{MIN}, the input current will present different shapes depending on C. **Figure 13** plots this input current for different values of C. As can be seen, the current trends to be sinusoidal for high values of C, while high distortion is present for low C values. To quantify this distortion, the values of PF and THD, as a function of C, have been calculated. **Figure 14** plots both parameters as a function of C. The amplitudes of the line current harmonics, as a function of C, have been obtained, and they are shown in **Figure 15**.

In order to choose an appropriate value of C, the fulfilling of the corresponding standards must be verified. For this driver, both the limits provided by the IEC61000-3-2 and the Energy Star Program Requirements for Solid-State Lighting Products are applicable. The latter sets the minimum PF as 0.7 for residential and as 0.9 for commercial applications. The values corresponding to the IEC61000-3-2 are given in **Table 1**. This table also shows the values of the theoretical current harmonics calculated for different C values. In bold letters are those values that fulfill the mentioned standard. As can be seen, the minimum capacitance value to verify the standards is C = 47 µF. Moreover, this capacitance value also fulfills the Energy Star standards for residential and commercial applications, as the PF raises above 0.9. The theoretical current harmonics for this capacitor value, as well as the limits provided by the standard are depicted in **Figure 16**.

Solving (34) also provides a relationship between the maximum voltage values and C. This relationship, depicted in **Figure 17**, can be used to size the capacitor. As it can be seen, in this case the maximum voltage value for the selected capacitor, u_{CMAX}, is given by:

$$u_{CMAX} = 81\ \text{V} \tag{51}$$

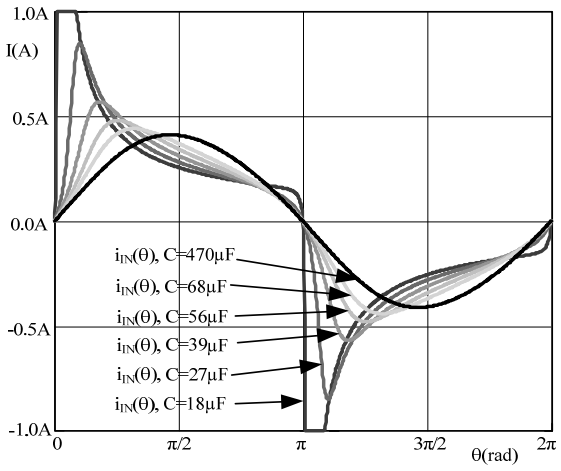


Figure 13. Theoretical waveforms of the AC line input current, i_{IN}, as a function of different capacitance values.

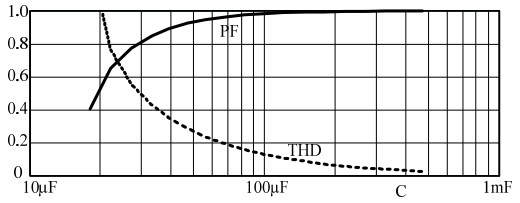


Figure 14. Theoretical values of *PF* (filled line) and THD (dotted line) of the input current, for different *C* values.

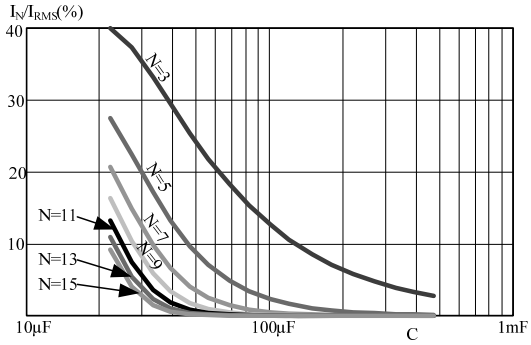


Figure 15. Theoretical values of the amplitudes of the line current harmonics for different capacitance values.

Table 1. Current harmonics of the input current limited by IEC-61000-3-2, and theoretical values for different *C* values.

Current Harmonics	*PF*	1st	3rd	5th	7th	9th	11th to 39th
Standard (%)		-	30·PF	10	7	5	3
Theor. (%) C = 18 µF	0.407	60.1	36.8 (12.2)	28.8	24.2	21.1	≤19
Theor. (%) C = 27 µF	0.774	87.5	37.3 (23.2)	22.4	14.9	10.4	≤8.0
Theor. (%) C = 33 µF	0.850	91.9	33.2 (25.5)	17.2	9.80	5.88	≤4.0
Theor. (%) C = 39 µF	0.892	94.3	29.5 (26.8)	13.2	6.57	3.43	≤1.9
Theor. (%) C = 47 µF	0.926	96.1	25.4 (27.7)	9.65	4.06	1.79	≤0.8

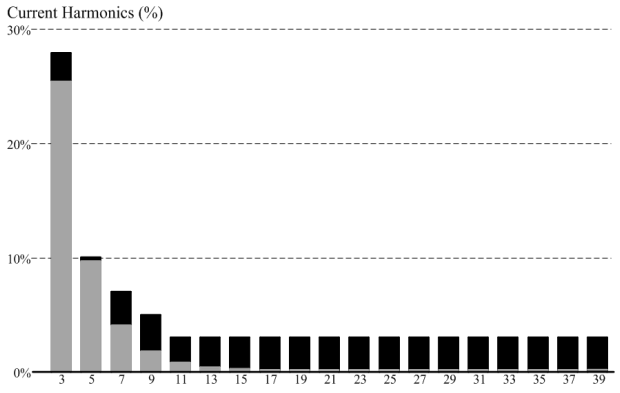


Figure 16. Theoretical harmonics of the input current of the integrated ballast for the selected value of 47 µF (grey), and current harmonic limits given by IEC 61000-3-2 (black).

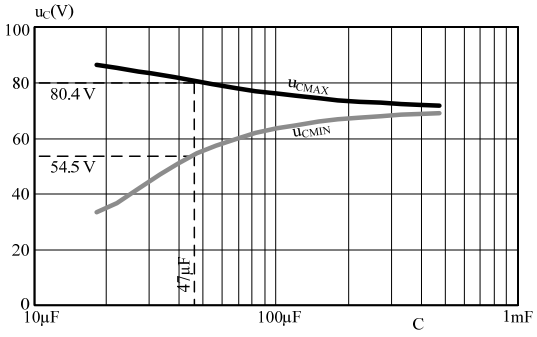


Figure 17. Theoretical value of the peak (maximum) and valley (minimum) voltage values in a line period at capacitor *C* for different capacitance values.

Also, the final turns ratio of the transformer can be designed. Considering (45), for the selected value of *C*, the value of the turns ratio is:

$$\frac{N_P}{N_S} \geq 3.1 = 4 \tag{52}$$

5.4. Dimension of the Power Switches

From the above discussion, the values of the absolute maximum voltage and current values for the switches of the converter can be selected considering **Figure 11**. Considering (51) and (52), the maximum voltage at the drain of the integrated switch is given by:

$$u_{SINT\_MAX} = V_{INPK} + \frac{N_P}{N_S} \cdot u_{CMAX} = 520 \text{ V} \tag{53}$$

The maximum reverse voltages in diodes D_1 and D_2 can also be calculated from **Figure 11**:

$$u_{D1AK\_MAX} = V_{INPK} + \left(\frac{N_P}{N_S} - 1 \right) \cdot u_{CMAX} = 438 \text{ V} \tag{54}$$

$$u_{D2AK\_MAX} = u_{CMAX} = 81 \text{ V} \tag{55}$$

Equations (53) and (54) have been calculated considering the aforementioned ±20% input line variation. It must also be noticed that these calculations do not consider an input clamp voltage snubber to store the energy handled by the leakage inductance of the primary side of the transformer. This snubber rises up significantly the maximum drain voltage, usually around 20% - 25%, what must be considered in the final implementation.

6. Built Prototype and Experimental Results

A built prototype of the integrated driver has been built and tested, for the stated load of 10 power LEDs connected in series.

Figure 18 shows experimental waveforms measured in the built prototype in steady state. **Figure 18(a)** depicts the capacitor voltage, the voltage and current through the LEDs, and the drain to source voltage at the switch S_{INT}, for an input voltage of 100 V ($\theta \approx 50^\circ$). **Figure 18(b)** shows these waveforms for an input voltage of 162 V ($\theta = 90^\circ$)

The line frequency waveforms of the prototype are shown in **Figure 19(a)**. As can be seen, the current through the LEDs is kept constant through all the line cycle, although the capacitor voltage, u_C, presents a significant voltage ripple. **Figure 19(b)** plots the experimental and theoretical waveforms of the capacitor voltage, u_C, and the line input current, i_{IN}. As can be seen, the experimental waveforms are in good agreement with the expected values.

Table 2 shows the PF and the amplitude of the input current harmonics for both the theoretical and the experimental waveforms. The experimental input current harmonics are depicted in **Figure 20**, along with the limits given by the IEC 61000-3-2 standard. As can be seen, the waveform fulfills these standards, although the experimental values of the current harmonics are slightly greater than the theoretical ones. In fact, the experimental THD is 36%, while the theoretical THD is 25%. The

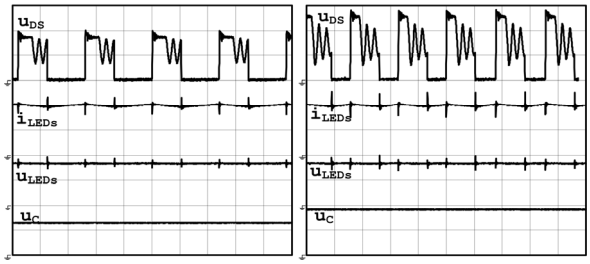


Figure 18. Main experimental high frequency waveforms in the built prototype, at different line angles. (a) V_{IN} = 100 V ($\theta \approx 50^\circ$). (b) V_{IN} = 162 V ($\theta \approx 90^\circ$). (all traces: u_C 50 V/div; u_{LEDs}: 20 V/div; u_{DS}: 200 V/div, i_{LEDs}: 500 mA/div; time: 5 µs/div).

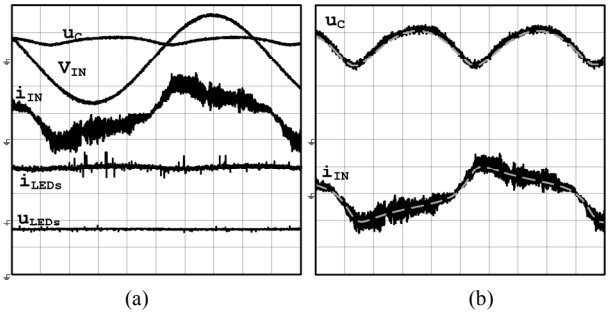


Figure 19. (a) Main experimental line frequency waveforms (u_C and u_{LEDs}: 50 V/div; u_{RECT}: 100 V/div; i_{LEDs}: 1 A/div; i_{IN}: 500 mA/div; time: 2 ms/div); (b) Comparison between theoretical and experimental waveforms of u_C and i_{IN} (u_C 20 V/div; i_{IN}: 500 mA/div; time: 2 ms/div).

Table 2. Theoretical vs. experimental values of the input current harmonics.

Current Harm.	*PF*	1st	3rd	5th	7th	9th	11th to 39th
Standard (%)		-	30·PF	10	7	5	3
Theor.(%) $C = 47$ µF	0.926	96.1	25.4 (27.7)	9.65	4.06	1.79	≤0.8
Exp. (%) $C = 47$ µF	0.911	95.2	26.3 (27.7)	9.01	2.67	2.28	≤2.47

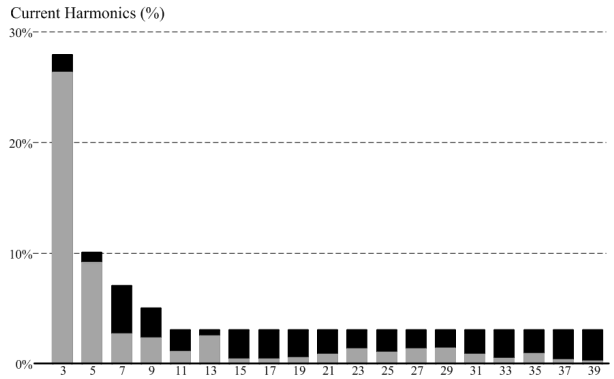


Figure 20. Experimental harmonics of the input current of the integrated ballast for the selected value of 47 µF (grey), and current harmonic limits given by IEC 61000-3-2 (black)

overall system efficiency is 85.8%, while the output power is 31.2 W.

7. The Dimming Procedure

As it has been mentioned before, both AM and PWM dimming schemes can be carried out in the proposed integrated ballast. This section explains the main advantages and drawbacks of both strategies in the proposed ballast, and finally selects the best dimming option.

7.1. PWM Dimming

For the PWM dimming scheme, the basic idea is to modulate the operation of switch S_{INT} at a low fixed frequency, with a duty ratio d_{DIM} proportional to the output light level required. Thus, a PWM dimming scheme will be obtained at the output current waveform. As the proposed topology is an integrated circuit, with only one controlled switch, the PWM diming scheme can only be implemented by completely turning on and off the full converter. Thus, the dimming frequency is limited by the dynamic behavior of the whole ballast. The theoretical current through the LEDs and the line input current, both in a line period, have been depicted in **Figure 21**. **Figure 21(a)** shows the theoretical line and LEDs currents at full power operation, that is to say without dimming, while **Figure 21(b)** shows the same waveforms if operated under PWM dimming scheme (modulated with a low frequency). In fact, **Figure 21(b)** shows the typical PWM dimming current waveform. Notice how if this scheme is carried out, the input current would be pulsated at the dimming frequency (**Figure 21(b)**). Thus, the input EMI filter must guarantee a correct filtering of the input current, at the dimming frequency rather than at the switching frequency. In order to achieve a feasible driver, this dimming frequency should be high enough as to allow reasonable values for the EMI filter values. **Figure 22** shows the LEDs current for a PWM scheme, by turning on and off the complete driver at a frequency of 500 Hz. As can be seen, the turn on and turn off transients seen in the current waveform prevent the use of higher frequencies for the dimming scheme, which yields to non-practical too bulky EMI filters. **Figure 23** shows the main waveforms of the converter for different PWM dimming ratios. Particularly, **Figure 23(a)** shows the input current waveforms for those dimming ratios (100%, 50% and 10%). As can be seen, the pulsating input current waveforms increase significantly the THD and decrease the PF to non-admissible values. Thus, this dimming scheme is not feasible for this topology.

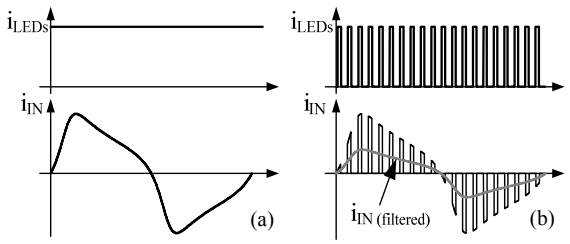


Figure 21. Current through the LEDs, i_{LEDs}, and line input current, i_{IN}, for a line period. (a) without PWM dimming; (b) with PWM dimming.

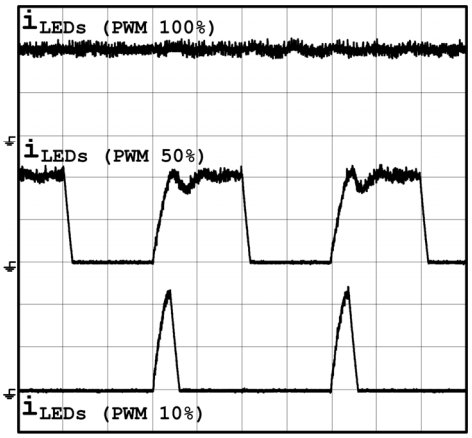


Figure 22. Experimental waveforms of the current through the LEDs for PWM dimmed operation of converter (PWM dimming 100%, 50% and 10%). All traces 500 mA/div, 500 µs/div.

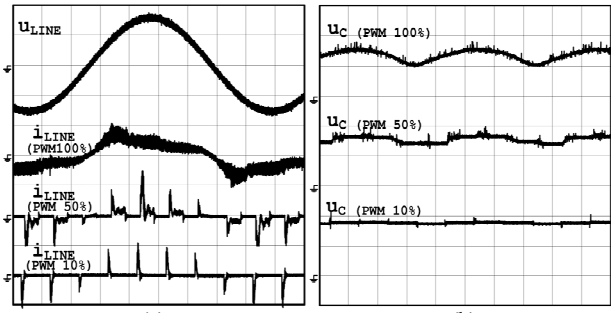


Figure 23. (a) Input AC line voltage, u_{LINE} (50 V/div), input AC line current, i_{LINE} (1 A/div), for different PWM dimming ratios (100%, 50% and 10%); time 2 ms/div. (b) DC link capacitor voltage, u_C (50 V/div), for different PWM dimming ratios (100%, 50% and 10%); time 2 ms/div.

7.2. AM Dimming

AM dimming scheme consists in changing the DC current level flowing through the LEDs. For this topology, it can be easily done by changing the peak current reference of the control stage, in the high frequency switching scheme. As the output current level decreases, the output power level also decreases. As the power flows through the output through the DC link capacitor, that is loaded from the input stage at twice the line frequency, a smaller power output yields to a smaller voltage ripple in the DC link capacitor voltage. This yields to an input current waveform with smaller harmonics, and hence the THD and the PF increase for higher AM dimming ratios. This can be observed in **Figures 24-26**, where the main waveforms of the proposed converter for AM diming ratios of 100%, 50% and 10%, respectively, are shown. It can be seen how the line input current is more sinusoidal as the diming ratio increases. It can also be seen how the voltage ripple in the DC link capacitor is also smaller for higher dimming ratios. Hence, this dimming scheme is selected for this application as the best option.

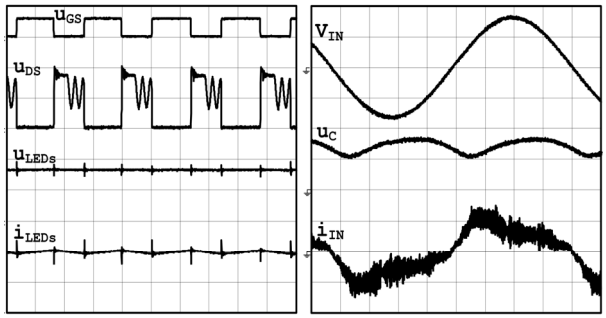
8. Design Considerations for Universal Input Voltage

This section deals with an analysis of the effect in the design parameters when considering Universal input voltage range in the proposed ballast. To carry out an effective comparison, it is necessary to explore which are the design parameters affected by this input margin increase. In fact, the lower limit remains constant at 115 V_{RMS} (–20%), while the higher voltage limit considered will be 230 V_{RMS} (+20%). The frequency range considered will be 50 - 60 Hz.

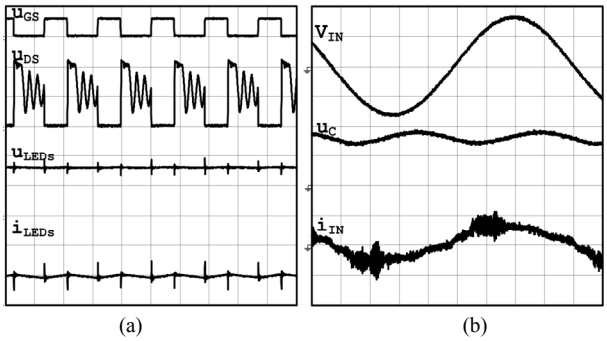
The main design parameters for American and Universal input voltage ranges are presented in **Table 3**.

The values of the magnetizing inductance of the primary side of the transformer, L_F, and the bulk DC capacitor, C, were calculated in (49) and (51) respectively for the minimum input voltage range, thus their design values are not affected by the input range increase. Analogously, the turns ratio can be calculated from (45) for the new input margin, but as the most restrictive condition comes from the smaller input voltage, this parameter also remains constant.

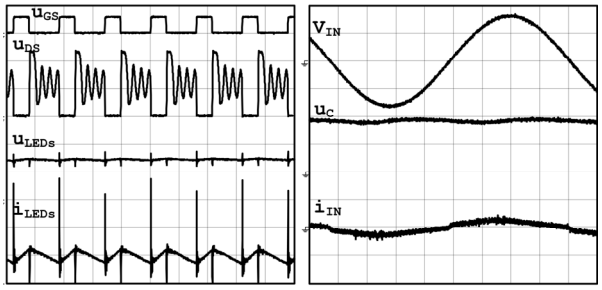
However, the maximum capacitor voltage depends on the maximum input voltage range, and thus this value increases significantly for the one calculated for American input range. A similar capacitor voltage plot (like the one depicted in **Figure 17**) can be calculated but for universal input voltage, yielding to an increase in the capacitor maximum voltage from 81 V to 130 V.



Figures 24. Experimental waveforms for full power operation of converter (AM dimming 100%). (a) Gate to source voltage, U_{GS} (20 V/div); drain to source voltage, U_{DS} (200 V/div); LEDs forward current, i_{LEDs} (500 mA/div) and LEDs voltage, u_{LEDs} (20 V/div); time 5 μs/div; (b) Input AC line voltage, u_{LINE} (100 V/div), input AC line current, i_{LINE} (500 mA/div), DC link capacitor voltage, u_C (50 V/div); time 2 ms/div.



Figures 25. Experimental waveforms for 50% AM dimmed operation of converter (AM dimming 50%). (a) Gate to source voltage, U_{GS} (20 V/div); drain to source voltage, U_{DS} (200 V/div); LEDs forward current, i_{LEDs} (500 mA/div) and LEDs voltage, u_{LEDs} (20 V/div); time 5 μs/div; (b) Input AC line voltage, u_{LINE} (50 V/div), input AC line current, i_{LINE} (500 mA/div), DC link capacitor voltage, u_C (50 V/div); time 2 ms/div.



(a) (b)

Figures 26. Experimental waveforms for 10% AM dimmed operation of converter (AM dimming 10%). (a) Gate to source voltage, U_{GS} (20 V/div); drain to source voltage, U_{DS} (200 V/div); LEDs forward current, i_{LEDs} (200 mA/div) and LEDs voltage, u_{LEDs} (20 V/div); time 5 µs/div; (b) Input AC line voltage, u_{LINE} (50 V/div), input AC line current, i_{LINE} (500 mA/div), DC link capacitor voltage, u_C (50 V/div); time 2 ms/div.

Table 3. Design values for American and Universal input voltage range.

Input voltage range.	L_F	C	N_P/N_S	u_{C_MAX}	$u_{SINT\ MAX}$	$u_{D1AK\ MAX}$	$u_{D2AK\ MAX}$
115 V_{RMS} (±20%), 60 Hz	420 µH	47 µF	4	81 V	520 V	438 V	81 V
115 V_{RMS} (–20%) - 230 V_{RMS} (+20%), 50 - 60 Hz.	420 µH	47 µF	4	130 V	898 V	767 V	130 V

Also, the peak limit voltage values of the switches depend on this input voltage, and thus the values of u_{SINT_MAX}, u_{D1AK_MAX} and u_{D2AK_MAX} can be recalculated from (53), (54) and (55) for this new voltage condition. The results of this calculations are presented in **Table 3**.

As can be seen, the obtained voltage ratings for the universal input voltage range, up to 900 V in the case of the integrated switch, are too high, even without considering the increase in these values that will provide the clamp voltage snubber at the primary side of the transformer. Thus, this Universal input range design is beyond the scope of this paper, and will be addressed in future developments.

9. Conclusions and Future Developments

A novel integrated ballast for driving power LEDs from AC mains has been presented, deeply analyzed, designed, built and tested. The proposed driver has only one controlled switch, thus obtaining a simpler and more cost-effective system. Also, the obtained value of capacitance and voltage rating of the DC capacitor, 47 µF/81 V, allows the use of a non-electrolytic device, which also increases the reliability of the whole ballast. The proposed driver also allows AM dimming very easily, which is enough for a number of applications with no special constraints in color rendering, which are the target uses for this converter (e.g. emergency lighting systems, street lighting, etc.).

The main drawbacks are the low efficiency and the high stresses of the electronic devices. Also, and although the input current fulfills the harmonic regulations, the harmonic distortion of this waveform is relatively high. Another drawback is the lack of galvanic isolation due the integration process, although this drawback is not as critical as it could be in other kind of lamps (for instance HID lamps, where very high input voltage pulses must be provided to the lamp).

Future developments include a deep study of the design for Universal input voltage range, as well as the circuit optimization to increase efficiency. There are significant losses due to the high current values at turn-off of the semiconductors. Operating the input stage in CCM would decrease those current stresses. In fact, this optimization of the efficiency has both design aspects and constructive aspects, which must be discussed in future works.

10. Acknowledgements

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