

# Low Noise Phase CMOS Quadrature VCO with Superharmonic Coupling Using Cross-Couple Pair\*

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Received June 25, 2011; revised July 27, 2011; accepted August 25, 2011

## Abstract

This paper aims to introduce a quadrature VCO (voltage control oscillator) which applies superharmonic coupling. The presented quadrature VCO is suitable to be used, both with  $2 \times$  subharmonic mixers, as well as  $4 \times$  subharmonic mixers. It would be impossible to avoid the presence of harmonics in CMOS VCO circuits. These harmonics are in general, undesirable signals which tend to accompany the desired fundamental signal. There are common-mode nodes (similar to those in the two source nodes in a cross-coupled VCO) in differential VCO at which higher-order harmonics are present while the fundamental is absent in essence. We can make use of these second-order harmonics which are present at the common-mode nodes of two VCO in order to implement a quadrature connection between the fundamental outputs. The technique through which this is done is called superharmonic coupling. This CMOS quadrature VCO which applies active superharmonic coupling puts an excellent performance in show, with an output power  $-0.942$  dBm for fundamental and  $-9.751$  dBm for subharmonic, phase noise  $-107.2$  dBc/Hz for fundamental and  $-114.8$  dBc/Hz at a 1MHz offset. All of circuit applied are designed and simulated by ADS, 2008.

**Keywords:** Quadrature VCO, Cross-Couple, Phase Noise, CMOS

## 1. Introduction

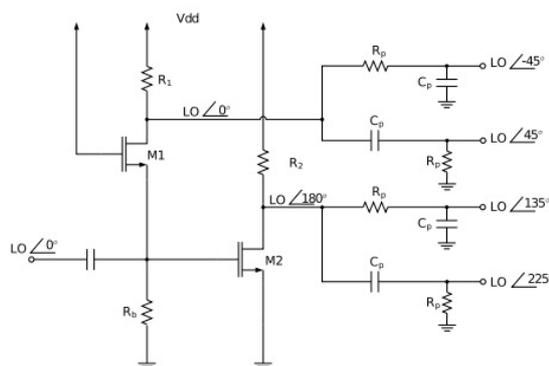
Oscillators are fundamental components in wireless communications systems that can be used for several applications. Communication systems that use phase shift keying modulation frequently require a pair of LO signals that are in quadrature, or  $90^\circ$  out-of-phase.

Quadrature VCO (voltage control oscillator) is one of the most important components in direct conversion transceivers. These VCOs are of a basic role in image-rejection techniques which are based on the appropriate phasing of the signals. Furthermore, they eliminate the immense and non-planar high-frequency filters. It also should be added that, some digital radio communication systems (e.g. GSM and DECT) in which complex digital modulation schemes are applied in order to reduce the signal bandwidth to the possible minimum level, need quadrature VCO [1]. In all the applications mentioned above, departures from the quadrature phase or the existence of an amplitude imbalance between the two signals leads to a damaging effect on the performance of the whole system. There are a number of techniques

which can be applied to produce quadrature signals.

1) The first technique is a standard VCO which a RC-CR phase-shift network follows. If the real values of R and C are not accurate, it may result in errors in the quadrature which, in turn, necessitate compensation of some form [2].

The complete LO input circuit with balun and phase shifters is shown in **Figure 1** with relative phase shifts indicated at the output for clarity. Using a reference  $0^\circ$



**Figure 1.** RC-CR phase-shift network.

\*This work was supported in part by N.S.T.R.I Tehran, Iran.

phase of an LO input signal, the phase shift at the outputs in **Figure 1** would be  $-45^\circ, 45^\circ, 135^\circ, 225^\circ$  from top output to bottom relative to the input phase.

2) The second technique which can be applied is a VCO which runs at double frequency and a digital frequency divider based on flip-flops follows it. Here, the sections of the circuit which work at the double frequency may turn into a speed or power bottleneck.

3) Another technique is employing two cross-coupled VCO's [3].

4) Using active polyphase filters such as ring oscillator designs is another technique in this list. In four-delay stage ring oscillators, for example, taps at diametrically opposite points yield quadrature phases [4].

An alternative method for obtaining quadrature VCO based on the differential coupling at the second harmonics of two differential VCOs is introduced in this paper. As a matter of fact, if a 180-degree phase shift occurs between the second harmonics of two VCOs, their basic frequency components will be in quadrature states.

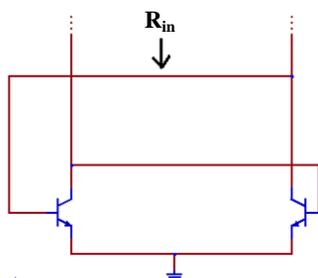
## 2. Design of a 4.8 GHz VCO

The cross-coupled VCO is the most frequently used microwave VCO topology in CMOS technology. We can prepare a model of a LC VCO with the capacitor and inductor, parallel with a resistor to simulate the losses in the tank, and also a negative resistance to simulate the active device. In order to produce the negative resistance to compensate for the losses in the LC tank, employing a cross-coupled differential pair, as shown in **Figure 2**, would be a choice. The resistance,  $R_{in}$  looking into the cross-coupled pair is obtained by:

$$R_{in} = -\frac{2}{g_m} \tag{1}$$

$g_m$  is the transconductance of each of the BJTs in the cross-coupled pair.

Therefore, by choosing a proper device size and biasing, the value of negative resistance necessary to counteract, we are able to find the losses in the tank.



**Figure 2. Negative resistance generated from cross-coupled BJT.**

**Figure 3** illustrates a frequently employed LC VCO circuit using the cross coupled differential pair. A moderately low supply voltage is possible to be used for this implementation because there are only two levels of transistors. However, it calls for two inductors, which require considerable chip area.

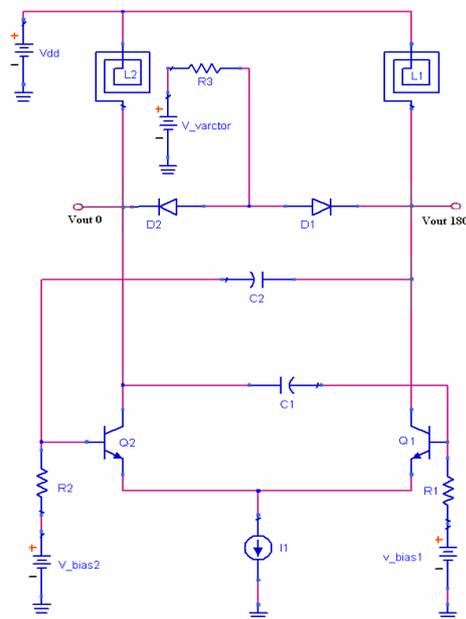
The VCO topology illustrated in **Figure 3** was applied (with BJT transistor) in [5].

CMOS technology was applied to design fundamental C band VCO for the present experiment. The Diode varactor illustrated in **Figure 2** allows the tuning of frequency.

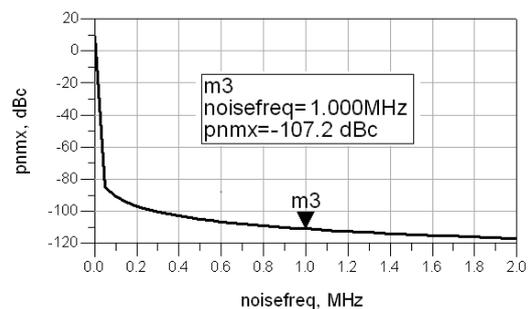
### Simulation Results for Cross-Coupled VCO

The signal output power was about 0.942 dBm and the phase noise at a 1 MHz offset was  $-107.2$  dBc/Hz.

**Figure 4** illustrates the phase noise graph. **Figure 5** illustrates the output power spectrum and **Figure 6** illustrates Time-domain VCO outputs.



**Figure 3. Cross-coupled BJT VCO.**



**Figure 4. Phase noise 4.8 GHz VCO.**

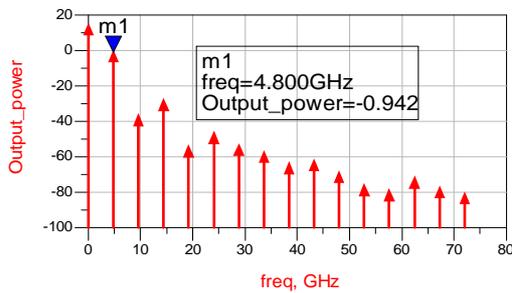


Figure 5. Output power VCO.

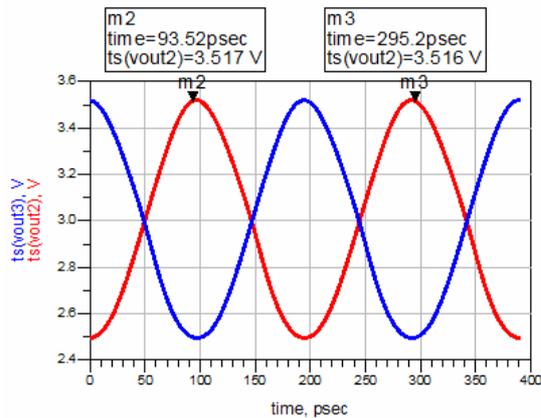


Figure 6. Time-domain VCO outputs.

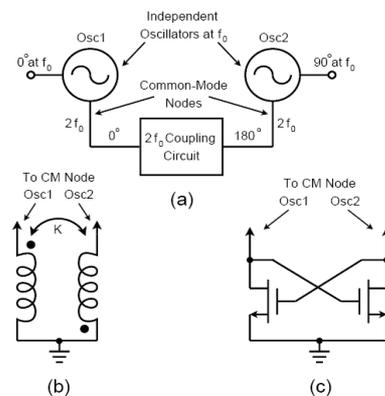
### 3. Concept of the Quadrature VCO

In most CMOS processes, resistors are particularly of large tolerances. Hence, this method may result in a low degree of accuracy in the quadrature signals that generated. In order to generate quadrature signals, another method is to employ a digital frequency divider which follows a VCO running at the frequency two times larger than the fundamental frequency [6]. There are some essential restrictions against using this technique at high frequencies for it calls for a VCO operating at double the desired frequency. A third frequent technique is to force two VCOs to run in quadrature through applying coupling transistors running at the fundamental frequency [7]. The problem with this technique is a trade-off between quadrature accuracy and phase noise which is due to the effects the coupling circuit imposes on the oscillation frequency. In order to overcome this problem, we may take advantage of realizing a quadrature VCO through superharmonic coupling. As shown in **Figure 7(a)**, quadrature signals are produced at the fundamental frequency by using differential coupling at the common-mode nodes where the second harmonic is predominant. In order to implement the coupling of the second harmonic with a  $180^\circ$  phase shift, the on-chip transformer has been inverted [8-10] (**Figure 7(b)**).

The method of superharmonic coupling implements a  $180^\circ$  connection between the even-ordered harmonics of the two VCO circuits, and this happens while both passive and active superharmonic coupling circuits are achievable. The performance of the two individual differential VCOs, as alongside with the coupling network will determine the performance of a quadrature VCO which applies the superharmonic coupling topology. This results in an anti-phase relationship between the second-order harmonics at the common-mode nodes.

### 4. Proposed Quadrature VCO

A frequently method used for implementing a CMOS differential LC VCO is applying a cross-coupled pair for generating the negative resistance needed for compensating for the losses in the tank. Hence, by choosing the proper device size and biasing, we are able to realize the negative resistance needed to counteract the losses in the tank. The core quadrature VCO circuit investigated in this work is shown in **Figure 8**. It is made of two cross-coupled VCOs connected through a cross coupled pair. It has been shown that the phase noise of the VCO can be enhanced notably by including cross-coupled inductor above the cross-coupled NPN transistors, due to the higher transconductance and faster switching speed of the corresponding structure [10]. We can find the oscillation frequency for each VCO via the common formula for finding the resonant frequency of an LC tank, in which  $L$  is the value of the on-chip spiral inductor and  $C$  is the total capacitance at the tank nodes. The inductors employed in this circuit of the capacitance less than 1.1 nH. The overall capacitance, including the lumped capacitor, and adding the parasitic capacitance was 0.925 pF which provided oscillation at 4.8 GHz.



**Figure 7. (a) Superharmonic coupling of the second harmonic to enforce quadrature at the fundamental; (b) Coupling using an inverting transformer; (c) Coupling using a cross-coupled pair.**

The network which is employed to implement the 180° phase difference in the second-order harmonics is a vital component of the quadrature VCO. This anti-phase association is the factor which generates the quadrature phase relationship at the fundamental frequency. Convenient common-mode nodes which are used for coupling the second harmonic are the common source nodes in each of the cross-coupled differential pairs, which are signified by CM1 and CM2 in the comprehensive VCO circuit schematic illustrated in **Figure 8**. DC blocking capacitors were used so that transistors N5-N6 could be biased for optimal coupling. Owing to the fact that any practical use of a VCO requires connecting its output to other circuitry, buffers are required to be employed in order to guarantee that loading does not disrupt the oscillations. For each of the four outputs we have used source follower buffers that we were able to measure the VCO using equipment with 50 Ω input impedances. The 180° and 270° outputs were terminated on-chip with 50 Ω loads and the 0° and 90° were linked to CPW pads for on-chip inquiring.

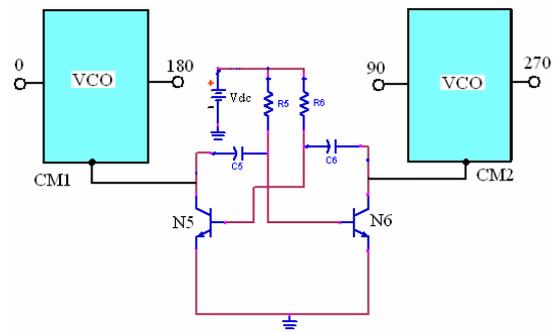
**Simulation Results for Quadrature Cross-Coupled VCO**

In Quadrature VCO at subharmonic frequency (9.6 GHz) the signal output power was approximately -9.751 dBm and the phase noise at a 1 MHz offset was -114.8 dBc/Hz.

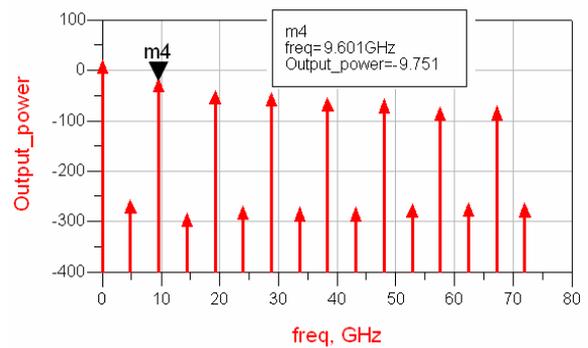
**Figure 9** shows spectrum of output power **Figure 10** shows Graph of phase noise. And **Figure 11** shows Time-domain VCO outputs. **Table 1** shows result of fundamental and subharmonic VCO. **Table 2** shows result of compare with other VCO designs.

**5. Conclusions**

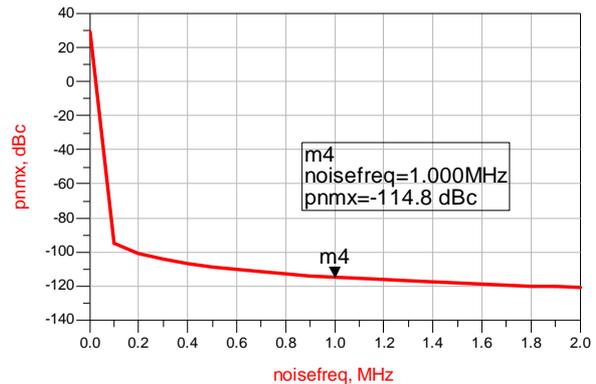
This paper represents a CMOS quadrature VCO which was designed at 4.8 GHz by applying superharmonic coupling. This technique focuses on coupling the second-order harmonics between two VCO and obliges an anti-phase connection, which, in turn, compels a quadrature relationship at the fundamental. In order for this coupling with a 180° phase shift to be implemented, a cross-coupled differential NPN pair was employed at the common-mode nodes. This CMOS quadrature VCO which employs an active superharmonic coupling demonstrates a very fine performance with an output power of -0.942 dBm for fundamental and -9.751 dBm for subharmonic, phase noise of -107.2 dBc/Hz for fundamental and -114.8 dBc/Hz at a 1 MHz offset. it creates the 180° phase shift in the second-order harmonics by using a cross-coupled differential pair.



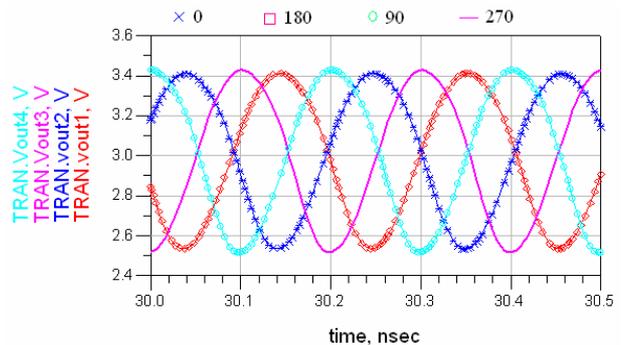
**Figure 8. Schematic quadrature VCO.**



**Figure 9. Output power quadrature VCO.**



**Figure 10. Phase noise quadrature VCO.**



**Figure 11. Time-domain Quadrature VCO.**

**Table 1. Compare fundamental and subharmonic VCO.**

	Fundamental	Subharmonic
Freq	4.8 GHz	9.6 GHz
Output Power	-0.942 dBm	-9.751 dBm
Phase Noise	-107.2 dBc/Hz	-114.8 dBc/Hz

**Table 2. Compare with other VCO designs.**

Reference	$f_c$ (GHz)	Phase noise(dBc/Hz)	Device
[11]	8.7	-110	SiGe BiCMOS
[12]	2.2	-111	CMOS0.35 $\mu$ m
[13]	11.02	-86.83	CMOS RF
[14]	1.6	-114.7	CMOS 0.18 $^\circ$ $\mu$ m
This Work	9.6	-114.8	CMOS 0.18 $^\circ$ $\mu$ m

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