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Precision Full-Wave Rectifier Using Two DDCCs

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Abstract

A new precision full-wave rectifier employing only two differential difference current conveyors, which is very suitable for CMOS technology implementation, is presented. The proposed rectifier is the voltage-mode circuit, which offers high-input and low-output impedance hence it can be directly connected to load without using any buffer circuits. PSPICE is used to verify the circuit performance. Simulated rectifier results based-on a 0.5 μm CMOS technology with ±2.5 V supply voltage demonstrates high precision rectification and excellent temperature stability. In addition, the application of proposed rectifier to pseudo RMS-to-DC conversion is also introduced.

Keywords: Full-Wave Rectifier, Voltage-Mode Circuit, DDCC, RMS-to-DC Conversion

1. Introduction

Full-wave rectifier is used in RF demodulator, piecewise linear function generator, AC voltmeter, watt meter and various nonlinear analog signal processing circuits. Typically, a conventional rectifier could be realized by using diodes for it rectification. However, this circuit would not be capable of rectifying incoming signals whose amplitudes are less than the threshold voltage (approximately 0.7 V for silicon diode and 0.3 for germanium diode). As a result, diode-only rectifiers are normally used in only those applications in which the precision in the range of threshold voltage is insignificant, such as RF demodulators and DC voltage supply rectifiers. For high precision applications, the diode-only rectifier cannot be used. This can be overcome by using integrated circuit rectifiers instead. The precision rectifiers based on operational amplifier (op-amp), diodes and resistors are presented [1-4]. However, the classical problem with conventional precision rectifiers based on op-amps and diodes is that during the non-conduction/conduction transition of the diodes, the op-amps must recover with a finite small-signal, dv/dt, (slew-rate) resulting in significant distortion during the zero crossing of the input signal. The use of the high slew-rate op-amps does not solve this problem because it is a small signal transient problem. The gain-bandwidth is a parameter of op-amp that limits the high frequency performance of this scheme. Moreover, since these structures use the op-amp and the resistors; therefore these circuits are not suitable for IC fabrication. Second-generation current conveyors (CCIIs) is possessed a very high slew rate and bandwidth if compared to the traditional op-amp. This makes the CCII of primary importance in the design of modern analog integrated circuits.

Several circuits based on CCII for realizing full-wave rectification have been reported in the literature [5-10]. The rectifier circuit in [5-7] employ diodes and resistors in addition to CCIIs. The circuit proposed in [8] employs bipolar current mirrors in addition to a CCII and a number of resistors. The rectifier circuit in [9] employs four CCCIIs and resistors. The circuit proposed in [10] employs two CCII and two MOS transistors. However, the use of resistor makes these circuits not ideal for integration. Recently, Chiu *et al.* [11] proposed a new current conveyor circuit called the differential difference current conveyor (DDCC). The DDCC has the advantages of both the CCII and the differential difference amplifier (DDA) (such as high input impedance and arithmetic operation capability).

In this paper, a new precision full-wave rectifier circuit using only two DDCCs is presented. Compared with previous rectifiers, the proposed structure is more suitable for integrated circuit fabrication. The circuit also offers a low output impedance terminal, which is suitable for low impedance load. Simulation results verifying the theoretical analysis are also included. To demonstrate the advantages of proposed configuration, pseudo RMS-

to-DC conversion is also introduced.

2. Circuit Realization

The electrical symbol of DDCC is shown in **Figure 1**. The DDCC has three voltage input terminals: Y_1, Y_2 and Y_3, which have high input impedance. The terminal X is a low impedance input terminal. There is a high impedance current output terminal Z. The CMOS realization for DDCC is shown in **Figure 2** [11]. The input-output characteristics of the ideal DDCC is described as

$$\begin{pmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_Z \end{pmatrix} = \begin{pmatrix} 1 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \end{pmatrix} \tag{1}$$

The proposed full-wave rectifier circuit is shown in **Figure 3**. The circuit employs only two DDCCs. Compared to previous rectifiers, the proposed rectifier is higher suitable for IC implementation. The $DDCC_1$ and $DDCC_2$ are operated as non-inverting and inverting unity-gain voltage buffers. The input voltage V_{in} is connected to Y_1 and Y_2 terminals of $DDCC_1$ and $DDCC_2$, respectively, while two outputs (X terminals) are connected. In this case, only positive peak will be appeared at the output voltage V_{out}.

The operation of the proposed full-wave rectifier is as follows: when $V_{in} > 0$, the $DDCC_1$ is on, the voltage V_{in} is followed by the $DDCC_1$ to the voltage V_{out} at X terminal. In addition, when $V_{in} < 0$, the voltage $-V_{in}$ is followed by the $DDCC_2$ to the voltage V_{out} at X terminal ($-V_{Y2} = V_X$). From the operation of the proposed full-wave rectifier explained, the relations between the input voltage, V_{in}, and the output voltage, V_{out}, can be expressed as

$$\left.\begin{aligned} V_{in} > 0 \;;\; V_{out} = V_{in} \;:\; \mathrm{DDCC_1 = on} \\ V_{in} < 0 \;;\; V_{out} = -V_{in} \;:\; \mathrm{DDCC_2 = on} \end{aligned}\right\} \tag{2}$$

The output voltage of the circuit in **Figure 3** can be expressed as

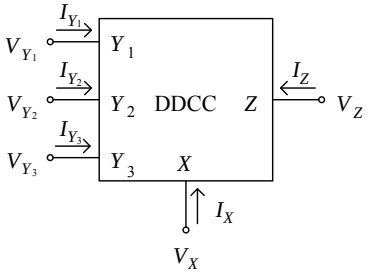

Figure 1. Electrical symbol for DDCC.

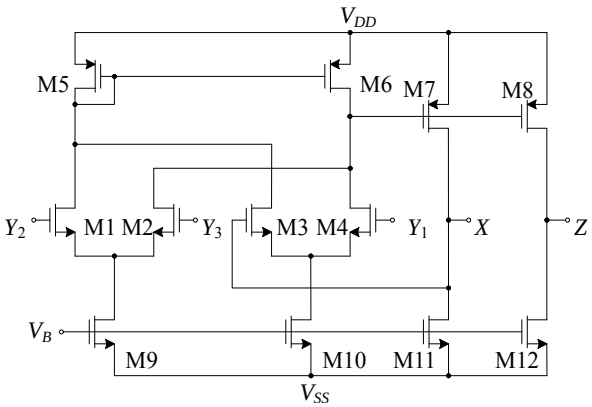

Figure 2. CMOS implementation for DDCC.

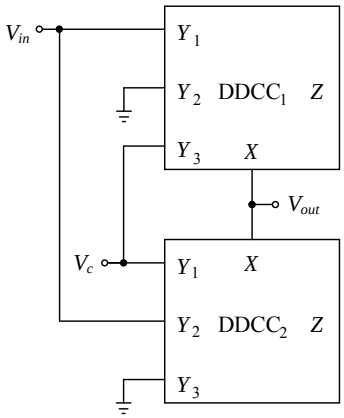

Figure 3. Proposed full-wave rectifier using DDCCs.

$$V_{out} = |V_{in}| \tag{3}$$

Therefore, the proposed circuit provides the full-wave rectification. It can be noted that the proposed circuit has high-input and low-output terminal, hence it is easy to drive loads without using a buffering device. The DC offset output voltage can be controlled by adjusting the voltage V_C.

3. Simulation Results

The proposed full-wave rectifier is simulated using PSPICE program to verify the given theoretical analysis. The DDCCs are simulated using CMOS structure of **Figure 2** that can be implemented using CMOS structures DDCC given in [12]. The aspect ratios of the MOS transistors of the CMOS DDCC are given in **Table 1**.

The device model parameters used for the PSPICE simulation are taken from MIETEC 0.5 μm CMOS process [12]. The supply voltages are selected as $V_{DD} = -V_{SS} = 2.5$ V and the bias voltage is set as $V_B = -1.7$ V. The DC transfer characteristic of the proposed full-wave rectifier is shown in **Figure 4**, which shows the operating

voltage ranging from –1 V to 1 V of the input voltage. The magnified zero crossing of **Figure 4** is shown in **Figure 5**. In this figure, the blunting region (b) is found as –2.5 mV < V_{in} < 2.5 mV. Applying the 200 m V_{peak} sine wave at the input of the proposed rectifier, the input and output signals at frequencies of 500 kHz and 1 MHz are shown in **Figures 6** and **7**, respectively. This results is confirms the operation that the proposed rectifier can provide the full-wave rectification at the input signal amplitude lower than the threshold voltage of diode (< 0.3 V). It is evident from **Figures 6** and **7** that undistorted full-wave rectified signals are produced at all two frequencies. However, as the input frequency increases to 1MHz and beyond, the output signals have errors at the crossover region, called "corner distortion". This corner distortion results from the non-conduction/conction transition problem of DDCCs. At the frequency of 1 MHz, we simulate the temperature performance of the proposed full-wave rectifier as shown in **Figure 3** by changing temperatures from 50˚C to 100˚C. **Figure 8** shows the output waveform of the proposed rectifier at temperatures of 50˚C, 75˚C and 100˚C. From simulation results in **Figure 8**, they show that the proposed circuit provides excellence temperature stability. This result is confirmed by Equation (3). The simulated peak outputs V_{out} for the circuit were 199.46 mV and 196.67 mV at 50˚C and 100˚C, respectively.

Table 1. Transistor aspect ratios of the used DDCC.

Transistor	W (μm)	L (μm)
M1-M4	1.6	1
M5-M6	8	1
M7-M9	20	1
M10-M11	29	1
M12-M14	90	1

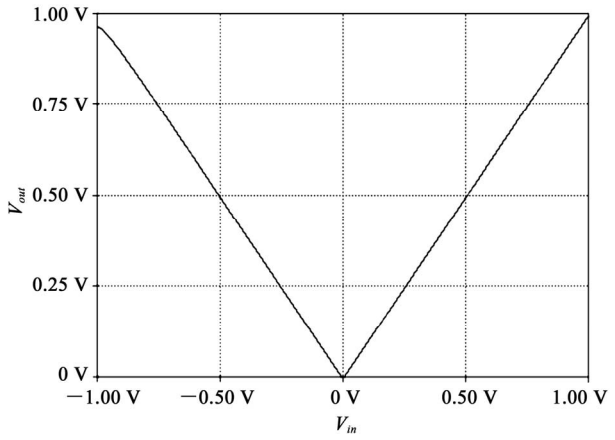

Figure 4. Simulated results for DC transfer characteristic.

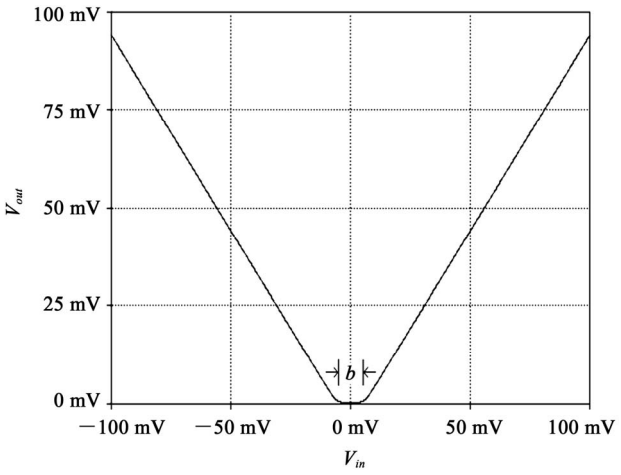

Figure 5. Simulated results for DC transfer characteristic at zero crossing regions.

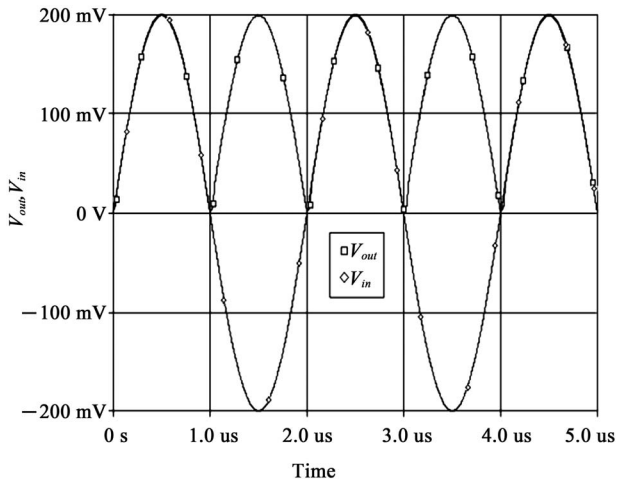

Figure 6. Operation of the proposed full-wave rectifier at 500 kHz frequency for V_{in} = 200 mV peak.

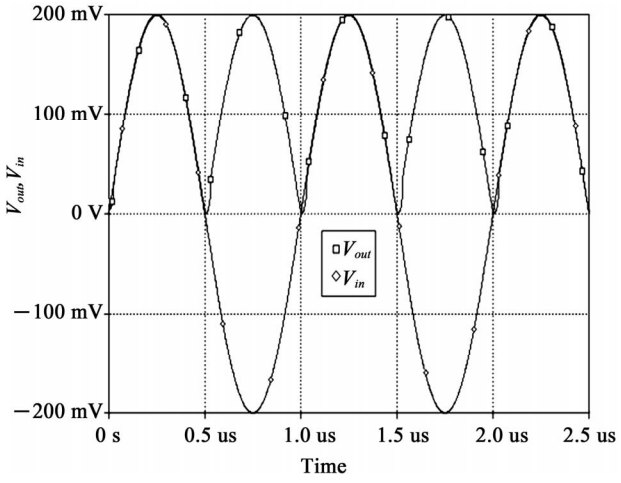

Figure 7. Operation of the proposed full-wave rectifier at 1 MHz frequency for V_{in} = 200 mV peak.

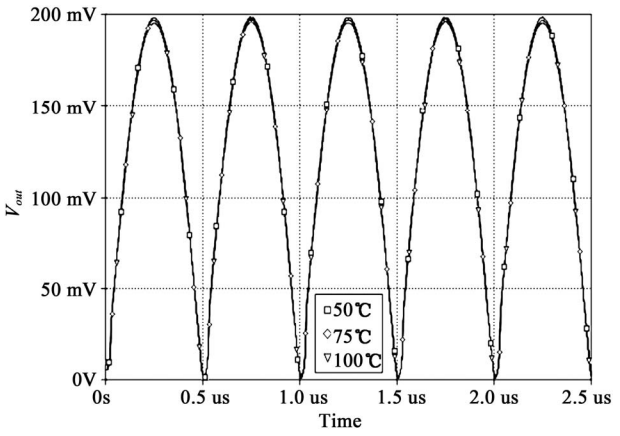

Figure 8. Operation of the proposed full-wave rectifier at different temperatures.

4. Application Examples

To show the advantage of proposed rectifier, author describes a pseudo root-mean-square (RMS)-to-DC conversion as an example. The well-known average value of a signal magnitude is defined by

$$V_{avg} = \frac{1}{T}\int_0^T \left|v(t)\right| \mathrm{d}t \tag{4}$$

where $v(t)$ is the AC signal, T is its period, and V_{avg} is the average value of the rectified signal of $v(t)$. To perform this operation, the AC signal is first full-wave rectified and then low-pass filtered to extract the DC component. For the case of a sinusoidal signal we have $v(t) = V_m \sin(2\pi f t)$, where V_m is the peak amplitude voltage and $f = 1/T$ is the frequency. Substituting $v(t)$ into (4) and integrating yields

$$V_{avg} = \frac{2}{\pi} V_m = 0.637 V_m \tag{5}$$

It is customary to calibrate the averaging circuits so that, with a sinusoidal input, the rms value is yield:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T v^2(t)\,\mathrm{d}t} \tag{6}$$

Substituting $v(t) = V_m \sin(2\pi f t)$ and solving yields

$$V_{rms} = \frac{1}{\sqrt{2}} V_m = 0.707 V_m \tag{7}$$

Comparing (5) and (7) we have [13]

$$\frac{V_{rms}}{V_{avg}} = \frac{\pi}{2\sqrt{2}} \approx 1.111 \tag{8}$$

which is the amount of amplification required to obtain V_{rms} from V_{avg}. By using proposed full-wave rectifier, both average value and RMS value of sinusoidal waveform can be readily implemented as shown in **Figure 9**. It should be noted that only grounded components are required. For more suitable IC implementation, all grounded resistors can be replaced by MOS resistor as shown in **Figure 10**. This resistor was presented in 1990 by Wang [14]. Assume MR_1 and MR_2 have the same characteristics and remaining in the saturation region. The resistance value of MOS resistor can be expressed as:

$$R_{eq} = \frac{1}{2K\left(V_{DD} - V_{TH}\right)} \tag{9}$$

where $K = \mu_o C_{ox}\left(W/L\right)$, V_{TH} is the threshold voltage and $V_{DD} = \left|V_{SS}\right|$ are the supply voltages. It can see that the value of resistor can vary by setting the appropriate aspect ratio.

A first-order low-pass filter is achieved with a properly specified R_L and C. The voltage V_{out} is converted to the input current of the filter in which the AC components are filtered through the capacitor C. The voltage value, V_{avg}, can be obtained by choosing R_{in} and R_{L1} identical. According to (8), V_{rms} can be obtained by setting $R_{L2}/R_{in} = 1.111$. For a symmetrical square input, the ratio of (8) becomes unity thus V_{avg} of **Figure 9** gives the exact RMS value because R_{in} and R_{L1} are identical. If $R_{L1}/R_{in} = 1.155$, the circuit may indicate the RMS value for either sinusoidal or triangular current signals. The criterion for specifying C_L (*i.e.* $C_L = C_{L1} = C_{L2}$) is that it must be large enough to keep the residual output ripple within specified limits, that is [13]

$$C_L \geq \frac{1}{4\pi f_{\min}} \tag{10}$$

where $f_{\min}$ is the low end of the frequency range of interest. C_L should usually exceed the right-hand term by the inverse of the fractional ripple error that can be tolerated at the output [14].

The RMS-to-DC converter in **Figure 9** is simulated using PSPICE program to verify the given theoretical analysis. For this simulation, three resistors (R_{in}, R_{L1} and

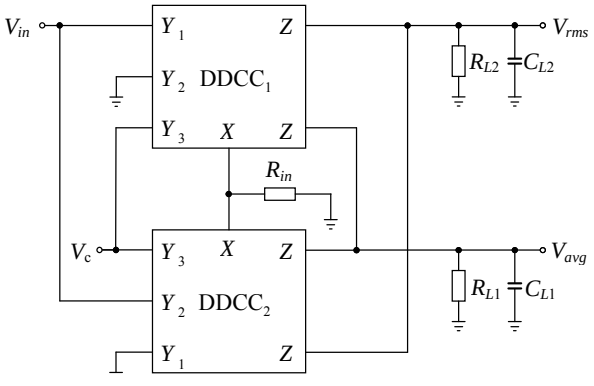

Figure 9. The full-wave rectifier-based RMS-to-DC converter for sinusoidal waveform.

R_{L2}) are replaced by MOS resistor as shown in **Figure 10** According to (8), when R_{in} and R_{L1} are identical to obtain V_{av}, then V_{rms} can be obtained by setting R_{L2}/R_{in} = 1.111. In this case, the aspect ratios (W/L) of MOS transistors, MR_1 and MR_2, for R_{in}, R_{L1} and R_{L2} are 2 µm/2 µm, 2 µm/ 2 µm and 1.8 µm/ 2µm, respectively ($R_{in} = R_{L1}$ = 3.457 kΩ and R_{L2} = 3.844 kΩ). A sinusoidal input with V_{in} = 200 mV and f = 1 MHz was applied to the converter and C = 1 nF. The supply voltages for DDCC are selected as $V_{DD} = -V_{SS}$ = 2.5 V and the bias voltage is set as V_B = −1.7 V. The multiple-output DDCC can be obtained by adding additional current mirrors. **Figure 11** shows the simulation results for V_{avg} = 126.63 mV and V_{rms} = 140.45 mV, with ripple less than 2%. In this case, the RMS voltage converter for both sinusoidal (output V_{rms}) and symmetrical square (output V_{avg}) waveform can be obtained. To achieve this case, the buffer circuits should be used.

5. Conclusions

In this paper, a new DDCC-based full-wave rectifier has been presented. The proposed circuit comprises only two DDCC which is suitable for IC implementation. The-proposed circuit has high-input and low-output impedance terminals, hence it easy to drive loads without using a buffering device. It can be applied to various nonlinear analog signal processing circuits. The performance of the proposed circuit is confirmed from PSPICE simulation results. Simulation results show that the proposed rectifier have excellent temperature stability. The application of proposed rectifier to pseudo RMS-to-DC conversion is also included.

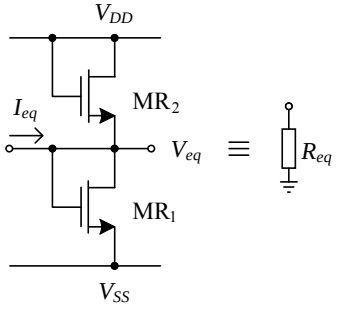

Figure 10. MOS resistor.

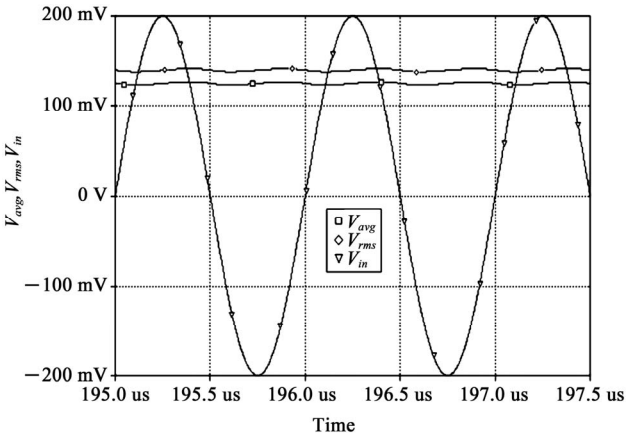

Figure 11. Simulated V_{avg} and V_{rms} for sinusoidal input with amplitude of 200 V_{Peak} and frequency of 1 MHz.

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