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Analysis and Design Aspects of a Series Power Semiconductor Array with Digital Waveform Control Capability for Single Phase AC Voltage Regulators and Other Applications

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Abstract

A series connected power semiconductor array, with digital control capability could be used for developing single phase AC regulators or other applications such as AC electronic loads. This technique together with an ordinary gapless transformer could be used to develop a low cost AC voltage regulator (AVR) to provide better or comparable specifications with bulky ferro-resonant AVR types. One primary advantage of the technique is that digital control can be used to minimize harmonics. Commencing with a review of AC voltage regulator techniques for single phase power conditioning systems, an analysis and design aspects of this technique is presented with experimental results for AVRs. Guidelines on how to utilize the technique in a generalized basis is also summarized together with a summary of a technique for achieving harmonic control.

Keywords: Power Conditioners, AC Voltage Regulators (AVR), Power Semiconductors, Digital Control, Electronic AC Loads

1. Introduction

With the proliferation of electronic systems based on submicron feature transistors, power quality (PQ) has become a major concern for end users as well as distribution authorities around the world [1-6]. Voltage sags and surges are a very common phenomenon in many distribution circuits, and it is particularly so in overloaded distribution systems. Voltage sags and surges seem to be distributed and tend to follow the daily loading patterns of the utility [2]. Extreme voltage fluctuations in many developing countries [7] and the need for lower cost products with easy manufacturability motivated the preliminary R & D work related to this specific technique. **Figure 1** indicates a typical pattern of voltage fluctuations in an urban location sub-circuit in Sri Lanka [7].

To improve the quality of power at the end user premises, three major considerations are voltage sags and surges, transient surges such as lightning or inductive energy dumps, and harmonics and flicker etc. An AC Voltage Regulator (AVR) is a particularly useful power conditioning equipment. The common AVR techniques used are: 1) motor driven variacs; 2) transformer tap changers; 3) ferro resonant regulators; 4) thyristor based

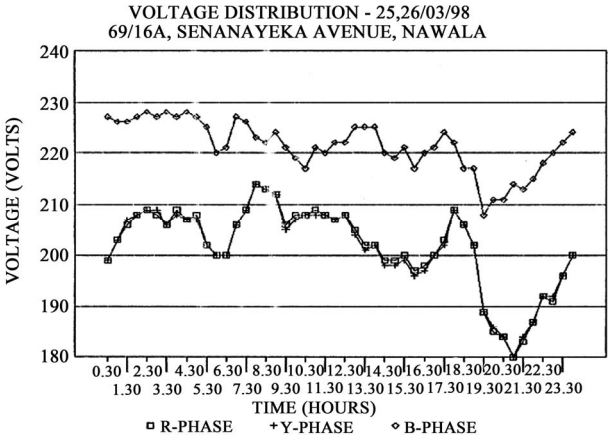


Figure 1. An example of a voltage variation in an overloaded distribution line (Source: Lanka Electricity Company).

systems (v) solid state AC regulators. **Table 1** summarizes the performance of these commercial families in a practical stand point in order to compare with the new technique we introduce in the paper. The information is particularly applicable to the single phase systems used by the end users and with output ratings from few 100Watts to few kilowatts. Magnetic amplifier techniques [8] usable in large capacity single or 3 phase systems etc are not discussed here.

Given the above variety of techniques used in commercial circumstances [9], a consistently popular technique has been the ferro-resonant type. Invented by Joseph Sola in the 1930s, this technique is popular due to its operational reliability, simple construction, and the ability to ride through a couple of AC cycles. However, this line frequency tuned LC resonant circuit based technique has the following disadvantages: 1) dissipates approximately 150 - 250 watts per each KVA of its output, due to the gapped transformer operating near saturation; 2) output regulation is dependant on the power factor of the connected load [10]; 3) various malfunctions when powered by a standby generator where the output frequency fluctuates with the load (due to LC circuit operating beyond resonance). Item 3) was a common occurrence in Sri Lanka during the drought periods with long power outages, where the first part of the work presented in the paper was carried out. In these cases frequent malfunctions of some commercial line interactive type UPS systems with ferro based AVRs were a common occurrence.

Apart from the above approaches used in commercial AVR techniques, there are few other published approaches to achieve AC voltage regulation in single phase power conditioners. Many of these are based on a series AC voltage component generated by a switching PWM scheme [11,12], or electronic transformers, which are also based on a PWM switching technique [13,14]. Another variation of a PWM based series connected AC regulator technique is described in [15,16]. The common problem in these are RFI/EMI due to PWM switching schemes, and the complex cost and manufacturing issues of adapting them to output power levels from few 100W to few kilowatts in single phase environments.

Given the above summary, key requirements in developing AVR techniques suitable for modern power conditioning requirements could be summarized as:

a) Reliability of operation in surge-prone PQ environments;

b) Efficiency under all load levels and load power factor situations;

c) RFI/EMI minimization;

d) Output harmonic minimization;

e) Speed of the control loops within the regulator;

f) Operability within the extremes of input line voltage limits;

g) Energy storage for short duration ride through requirements.

Table 1. Comparison of AC voltage regulators.

Family	Basic Technique used	Advantages	Disadvantages
Motor driven variacs	A servo motor based auto transformer with a voltage feedback loop	▪ Simple construction ▪ High capacity ▪ Simple electronics ▪ High efficiency	▪ Bulky ▪ Slow response ▪ Can get stuck at the lowest input voltage and create an over-voltage when the line voltage returns to normal
Transformer tap changers	A transformer with multiple taps and a feedback loop to automatically change the taps	▪ High efficiency ▪ Easy to design ▪ Simple construction ▪ Low cost	▪ If input voltage fluctuates frequently "tap dancing" could occur ▪ Arcing in taps can create problems, with inductive loads ▪ Voltage transients may appear at the output during tap changes
Thyristor based designs	A series secondary winding or an auto transformer is used with a thyristor phase controlled technique to maintain the RMS voltage constant	▪ Compact ▪ Low cost ▪ Efficient ▪ Fast response	▪ High harmonic content at the output ▪ Could cause problems with inductive loads ▪ Filtering at output may be necessary for reducing RFI/EMI issues
Ferro-resonant regulators	A precisely gapped transformer is used in resonance with a capacitor to create a resonant circuit, while core saturation is used for regulating the output voltage.	▪ Very reliable ▪ Simple design ▪ Can withstand a fractional or few cycle outage at the input side ▪ Differential mode transients can be tolerated	▪ Non sinusoidal output with flattened top ▪ Power factor dependant load regulation ▪ Extremely sensitive to frequency fluctuations on the input side (*i.e.*: when a small standby generator is used as the AC input) ▪ Low efficiency and no load power consumption of 20% - 30% of the VA rating
Solid state types	Either linear amplifier based technique or switching technique based compensation is used	▪ Wide input range is possible ▪ Compact design may be possible (with a switching technique for voltage buck or boost)	▪ Complex circuitry ▪ RFI/EMI problems (in switching technique based ones) ▪ Reliability issues in environments with high common mode transient surges

2. AC Power Control Technique Based on a Series Power Semiconductor Array

Given the above introduction to the commercial design approaches with key design requirements in AVRs, following section introduces the primary design concepts used in this technique. The technique discussed in this paper was developed for single phase end user equipment where the line voltage could fluctuate widely and to achieve a design without any ferro-resonant transformers for easy manufacturability.

This technique based on a series connected power semiconductor array [17-20] is suitable for situations where 230V AC rms voltage fluctuates widely between 160 V to 260 V. The technique has the following advantages and useful features:

1) Fast response and high efficiency at worst case sags
2) Gapless 50/60 Hz transformer;
3) True RMS output control;
4) Electrical isolation between low voltage control circuits and the power stage;
5) Minimum RFI/EMI issues;
6) Lower harmonic distortion at output and less dependence on the load power factor;
7) Equal power dissipation and voltage distribution among transistor elements.

This technique works for both sags and swells without any transformer configuration changes, compared to the technique described in [21]. The technique in [21] with a claim for a high efficiency near 96% is only for a limited range of regulated output which should be lower than the incoming rail with a minimum input voltage of just 4 volts above the regulated output.

The same design approach in [17-22] could also be used in developing an electronic AC load with digital control for harmonic minimization [23,24]. The rest of the paper describes the fundamentals and two applications of the technique, with an in depth discussion on the technique as applied to a single phase, low power AVR with the potential to minimize the harmonics at the output using a digital technique.

3. Concept of Impedance Control and Implementation

3.1. Basic Concept of Series Power Semiconductor Array

A conceptual approach for changing the effective overall AC resistance of a power BJT array over a wide range is shown in **Figure 2**. **Figure 2(a)** shows the simplified concept of control of the transistor. **Figure 2(b)** indicates how an opto isolator can be used to control current diversion in the power semiconductor. **Figure 2(c)** indicates how series connected infrared emitter diodes in an opto isolator can be used to control a series connected bipolar power transistor array with AC operational capability. When the transistor array is used in 230 V AC applications such as in an AC voltage regulator, the instantaneous values could often vary up to a maximum of approximately $330\sqrt{2}$ V for a range of input AC RMS voltages from 160V to 260V [25]. This high voltage requirement at high power loads suggests the use of multiple power semiconductors to share the loading.

For an n-element BJT array similar to the case of **Figure 2(c)**, it can be shown that,

$$R_{Array} \approx \frac{nR_B}{\beta}\left(1+\frac{i_x}{i_b}\right) \quad (1)$$

when

$$R_{B1}=\frac{R_B}{n}; R_{B2}=\frac{R_B}{(n-1)}; R_{B3}=\frac{R_B}{(n-2)}; \cdots R_{Bn}=R_B \quad (2)$$

where R_{Array} is the approximate effective instantaneous resistance at the AC input of the circuit in **Figure 2(c)**, i_b is the instantaneous base current, i_x is the amount of base current diverted by the opto transistors and R_B is the resistance between collector and base of the n^{th} transistor [22]. For the case of the 4 element array in **Figure 2(c)**,

$$R_{Array} \approx \frac{4R_B}{\beta}\left(1+\frac{i_x}{i_b}\right) \quad (3)$$

and,

$$R_1=\frac{R_B}{4}; R_2=\frac{R_B}{3}; R_3=\frac{R_B}{2}; R_4=R_B \quad (4)$$

Note that the base emitter voltage drops are neglected in these approximations.

Based on the simplified relationship in Equation (3), the resistance between the collector and the emitter can be easily controlled either by varying R_B or suitably changing i_x. This in effect indicates that we need to control the ratio i_x/i_b, which is defined as the base current diversion ratio (BCDR). This technique in addition provides the necessary electrical isolation between the low voltage control circuits and the power stage. In a practical application with Darlington pairs, the compound base emitter voltage will be between 1 to 2 Volts. This practically permits the concept of controlling the BCDR using opto isolators and similar low voltage control circuits. For details [23] is suggested. A similar design approach could be used with other power semiconductors such as MOSFETs and IGBTs, by modifying the above technique, a discussion of which is beyond the scope of the paper.

3.2. Limits and Boundaries of the Achievable AC Resistance

Due to Darlington pairs in **Figure 2(c)** a cutoff condition is reached when the compound V_{BE} value for the Darlington pair is approximately less than about 1.0 Volt. This occurs at a higher value of the opto transistor current and at that point the controllability of the array impedance diminishes. This is the case beyond the maximum BCDR, where the base current of each of the transistors is totally removed by the action of the optoisolators. Under this condition, the effective resistance of the array is not controlled by the transistors, except for the leakage effects. If the transistor leakage effects are neglected and the conditions in Equation (2) are maintained, the effective maximum resistance of the array reaches the value given by the series combination of the resistors R_{B1} to R_{Bn},

$$R_{CE\max} = R_B + \frac{R_B}{2} + \frac{R_B}{3} + \frac{R_B}{4} + \cdots \frac{R_B}{n} \tag{5}$$

At the other extreme, when the current through the input diodes of the optoisolators is zero (the case of minimum BCDR), the effective resistance of the array reduces to nR_B/β. In between these two limits the overall resistance of the array, R_{CE}, can be controlled by varying the current through the series connected diodes.

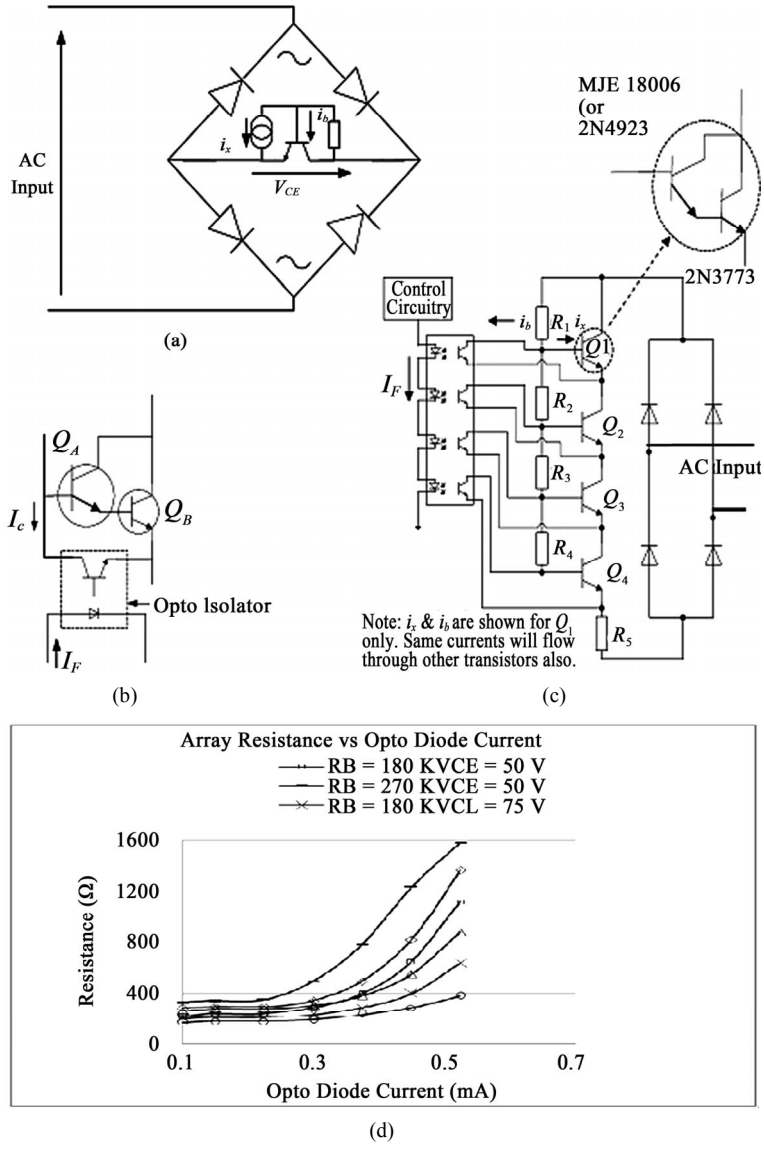


Figure 2. Concept of AC impedance control with a BJT array. (a) Simplified concept; (b) Control of the base current using opto transistor; (c) Implementation of a 4 element system; (d) Effective impedance (R_{array}) of a 4 element array versus opto diode current for R_B values of 180 kΩ and 270 kΩ.

From Equation (5) the maximum value of effective resistance for an array of 4 elements is approximately 2.1 R_B, neglecting the effects of leakage currents in transistors. Equation (3) indicates that the minimum resistance for the array is approximately $4R_B/\beta$. This clearly indicates a wide range of ideal performance possible within the boundaries. If the array is to work as a high voltage capable switching element, the value of R_B can be set to a suitable value for the designer to get the overall result of $4R_B/\beta$ to reach the lowest necessary, based on the circuit components. For a 4-element array the ratio of off-impedance/on-impedance is around β/1.9 and for a well configured Darlington pair this can be in the range of 3 orders.

Figure 2(d) depicts a typical example of the variation of the effective resistance versus control input I_F (opto-diode current) for R_B values of 270 kΩ and 180 kΩ for a four element array (as in **Figure 2(c)**) capable of 100W dissipation. It is clear that the lowest value reaches the theoretical value expected from $4R_B/\beta$. As indicated in **Figure 2(d)** for the case of 50 V AC input with R_B = 270 kΩ, the array reaches a maximum at higher values of I_F as per theoretical predictions and SPICE simulations. However the maximum value is significantly lower than the expected due to leakage effects.

Also the graphs indicate the dependence of the effective resistance on the AC line voltage, due to device nonlinearities and the dependence of β on the instantaneous collector current over the AC cycle. Another practical situation is that the transistors could have non identical β values. However it is easy to compensate for this variation by slightly adjusting the R_B values deviating from the relationship in Equation (2).

4. Application Examples

4.1. Design of an AC Regulator Based on the Technique

Figure 3(a) indicates the basic approach where the transformer T_1 allows the boost or buck operation. If you consider that the transformer is an ideal one, where the series winding has N times the turns as in the primary winding which is in series with the power semiconductor array placed across the bridge points of the full wave rectifier.

Under this arrangement, the following approximate relationship holds true, for any general load connected at the output.

$$\overline{V_{out}} = \overline{V_{in}}\left(1+N\right) - R_{array}N^2\overline{I_L} \qquad (6)$$

where $\overline{V_{Out}}$ and $\overline{V_{in}}$ are the output and input voltages and $\overline{I_L}$ is the load current in vectors respectively.

Figure 3(b) indicates the phasor diagrams for the case where the input voltage ($|V_{in}|$) is less than the required regulated output ($|V_{out}|$). In this example we consider the load current is lagging the input voltage by an angle Φ. Based on the relationship in Equation (6), and assuming that the impedance of the transistor array is purely resistive, and the transformer is ideal with no leakage inductances or resistances, the control circuits could regulate the output voltage, by maintaining the regulated V_{out} within the arc of the circle with a radius of $|V_{out}|$ in the region where the tangential points of the worst case phase angles of the load falls within $\pm\Phi_{max}$. Beyond these limits of the tangential points T and T' of the phasor diagram, regulation is not possible, for a given turns ratio N.

Few interesting and practically useful observation are that,

1) If the load is purely resistive, the regulated output voltage will be in phase with the input voltage;

2) For a given input voltage if the transformer is configured to have the case of $\overline{V_{out}} = \overline{V_{in}}\left(1+N\right)$, dissipation in the array is minimum;

3) Condition 2) above suggests having multiple taps in the transformer, to have the best efficiency under wide range of input voltage fluctuations;

4) When the transformer turns ratio increases, the allowable phase angle of the load decreases.

Figure 3(c) indicates the case of phasor diagram, where the input voltage is higher than the required regulated output voltage. In this situation, by creating a higher voltage across the array, and practically reversing the voltage at the primary winding, the regulation is achieved. In case the load is purely resistive, as expected the regulated output will be in phase with the input voltage. Also in this situation, when the input voltage rises above the required regulated output value, it is possible to reverse the connections of the primary winding, so that the dissipation across the array is reduced. In **Figures 3(b)** and **3(c)** the arc included within T and T' indicates the limits of the reactive component of the load to achieve regulation, assuming that the transformer is considered ideal.

As shown in the phasor diagrams the technique is useful in situations with non resistive loads as well, while regulating the output for both voltage sags and surges with out any transformer configuration changes.

Figure 4(a) indicates the implementation block diagram of a 230 V/50 Hz capable 1 KVA regulator based on the technique[17,18] developed to overcome the frequency sensitivity, waveform distortion and the lower overall efficiency of the commonly used ferro-resonant regulators and the slow response of motor driven variacs [26,27]. To cater for the worst case line voltage situations such as in [8], this AVR prototype was developed to operate within a wide range such as from 160 V to 260 V.

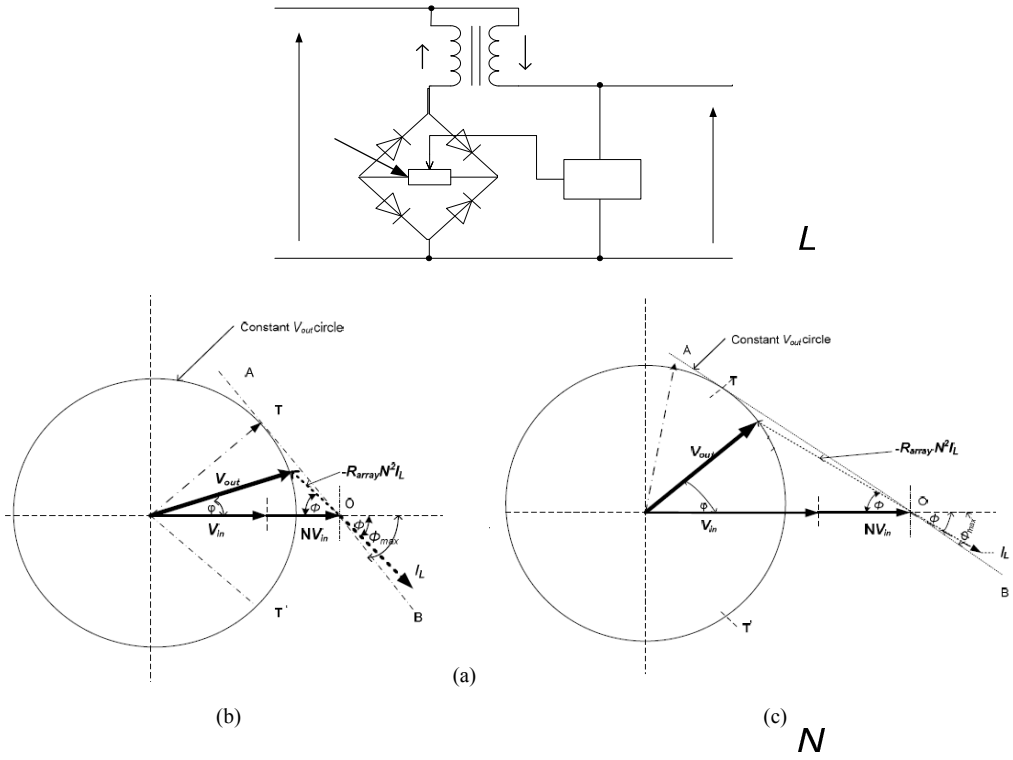


Figure 3. BJT array based AC regulator and phasor diagrams. (a) Basic concept; (b)Phasor diagram when input voltage is less than the regulated output; (c) Phasor diagram when input voltage is higher than the regulated output.

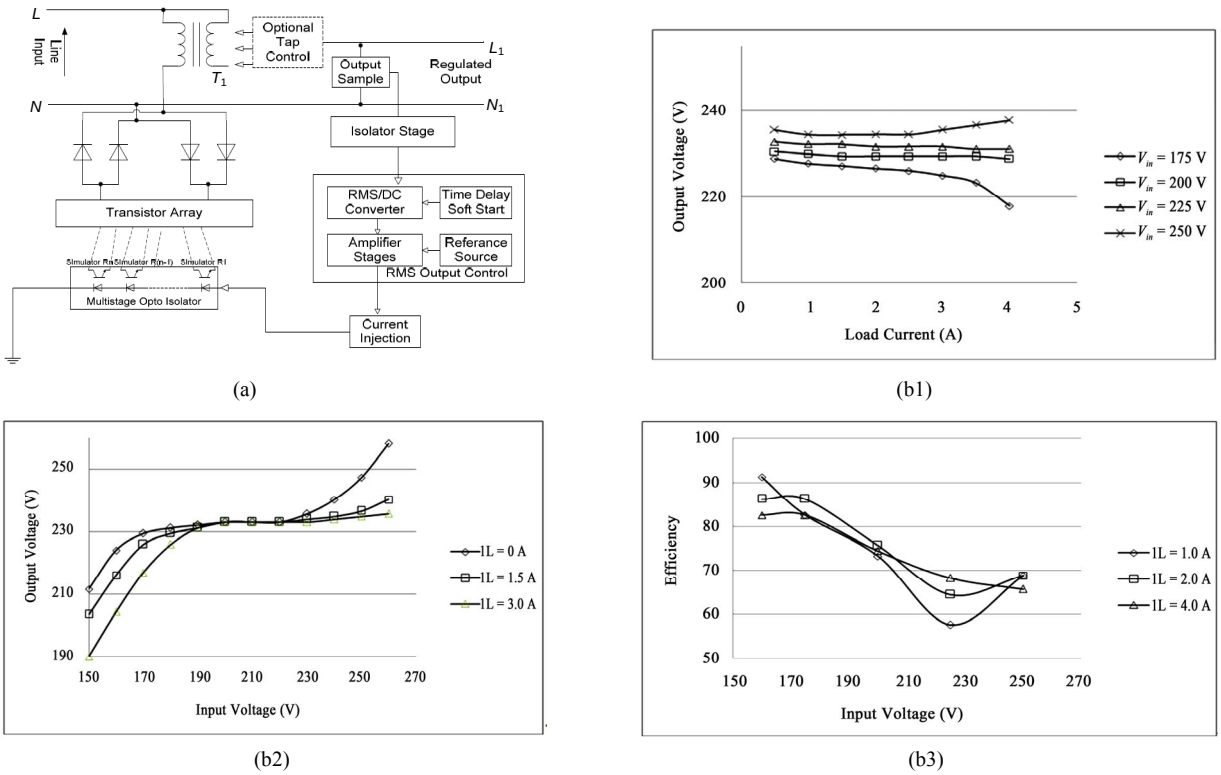


Figure 4. **AVR implementation of a 1 kVA prototype and measured performance. (a) Overall block diagram; (b1) Load regulation; (b2) Line regulation; (b3) Efficiency.**

For RMS output voltage control, the effective resistance of the array is varied depending on the load and the input voltage. RMS control circuit compares the actual AC output sample, converted to a DC value using an RMS-DC converter IC, with a reference DC voltage. Current injection circuit adjusts the current injected into the series connected input diodes of the opto isolator, based on the output of the RMS control circuits. This effectively controls the value of R_{array} in such a way that the loop keeps the output RMS value regulated at a preset value such as 230 V, for a wide range of input voltages.

Figures 4(b1) to **4(b3)** indicate the measured performance of an AVR prototype of output capacity of 1kVA based on Darlington pairs of 2N3773 and 2N4923 [17]. Load regulation graph in **Figure 4(b1)** indicates that the prototype regulates around 230 ± 6% V AC within an input voltage range of 170 V to over 250 V. The line regulation graph in **Figure 4(b2)** indicates that the technique is usable almost up to 160 V, however needs adjusting the lowest possible resistance of the array.

As per graph of **Figure 4(b3)** we see that the efficiency keeps dropping as the input voltage keeps increasing towards the nominal regulated value of 230 V. In the particular prototype tested [17], we have used a transformer with a turns ratio (N) of 70/160, where the array is expected to have the lowest resistance, at a worst case of input voltage of 160 V rms. If the input voltage reaches 230 V rms, the primary winding should have zero value so that the correction applied at the secondary side is zero. This indicates that the quantity $N^2 R_{Array} I_L$ should be equal to $230 * (70/160)$ V, for the case of a pure resistive load. Similarly if the input voltage goes towards a surge situation with over 230 V rms value, this quantity should be further increased, to generate a negative correction at the secondary winding.

In this prototype where the efficiency is optimized around 160 V, as the input voltage increases the efficiency drops. However the overall performance is comparable with a similar capacity ferro-resonant version. As discussed in a previous paragraph, by using multiple taps and reversing taps under surge voltage conditions at the input overall efficiency could be improved.

This gapless transformer based technique can be enhanced with a digital control subsystem to minimize the harmonics at the output. By suitable control circuitry, transformer tap changes can also be incorporated to further enhance the overall efficiency, recognizing the fact that the technique has a higher efficiency at the worst case sags, where only a minimum resistance value of the array is required as per Equation (6).

4.2. Electronic AC Load

Another useful application of the technique is in an electronic AC load. The design approach for an AC electronic load with processor control is indicated in [23-25]. A discussion on this is beyond the scope of this paper.

5. Processor Based Approach for Linearizing of the Array Resistance

Given the non-linear behaviour of the transistor array as per **Figure 2(d)**, the instantaneous current in the array will be nonlinear under general conditions, and will depend on the instantaneous AC line voltage as well as the dependency of the gain of transistor on its collector current. In order to control the non linearity of the value of R_{Array} which is equivalent to $\frac{V_{Array(rms)}}{I_{Array(rms)}}$, collector current in the opto transistors based on the following relationship could be controlled [27].

$$I_C = K\left(\frac{I_F}{I_{F'}}\right)^p \tag{7}$$

K, $I_{F'}$ and p are the parameters for opto isolator pairs [27].

From the basic transistor parameter relationships and assuming that all transistors are identical,

$$I_{Array} = I_S e^{qV_{BE}/kT} \tag{8}$$

where q is the electron charge, k is the Boltzmann constant and T is the absolute temperature of the transistor junction. I_s is the saturation current for the identical transistors Q_1 to Q_4 in **Figure 2(c)**.

By substituting the relationships in Equation (7) and (8) in Equation (3),

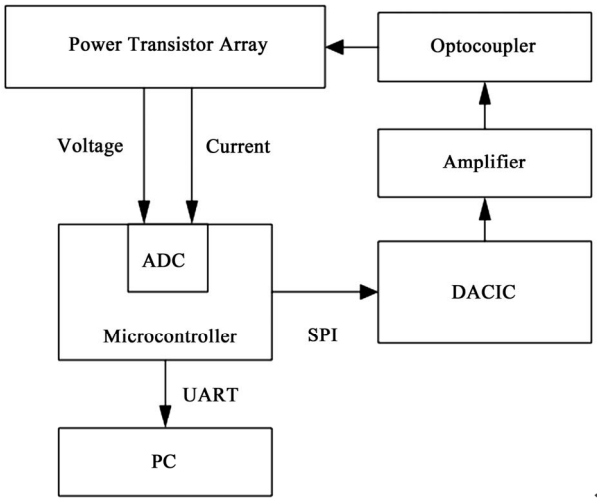
$$R_{CE} \approx \frac{4R_B}{\beta}\left[1+\beta\frac{K\left(\frac{I_F}{I_{F'}}\right)^p}{I_S e^{\frac{qV_{BE}}{kT}}}\right] \tag{9}$$

With suitable mathematical manipulations [23], we can also arrive at the following relationship for voltage across the array (V_{CE}) and the opto-diode forward current (I_F) for a given R_{CE} value, neglecting the v_{BE} compared to the instantaneous values of v_{CE}.

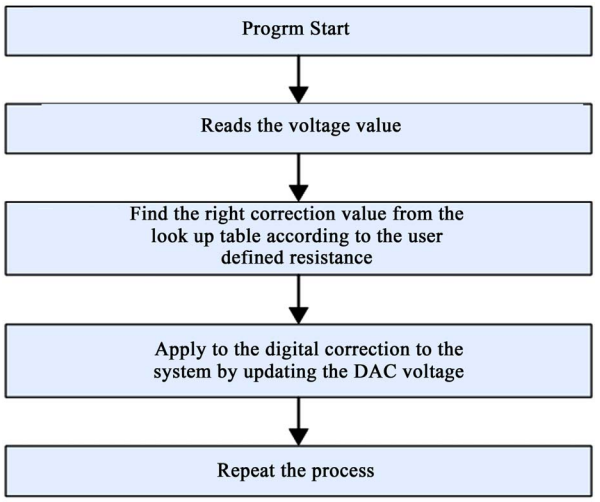
$$\ln V_{CE} = p \ln I_F + \frac{K\beta n R_B R_{CE}}{(\beta R_{CE} - n R_B) I_{F'}{}^p} \tag{10}$$

Based on the relationship of Equation (10) and using experimental data similar to **Figure 2(d)** for the circuit

arrangement in **Figure 2(c)**, curve fitting techniques can be used to obtain the logarithmic relationships for voltage across the array (V_{CE}) and the current fed through the photo diodes (I_F) of the opto isolator for each value of expected array resistance. Implementation of this is shown in **Figure 5** depicting the hardware block diagram and the flow chart applicable. By plotting these curves from the experimental results (which tallies with the SPICE simulation results) together with a straight line fit, it could be easily seen that a reasonably accurate values for m and c values for a straight line approximation can be obtained. Two selected examples from [25] are shown for array resistances of 500 Ω and 50 Ω in **Figure 6**. From these graphs, one can see that the relationship is very close to a straight line fit, with matching R^2 values close to 1.

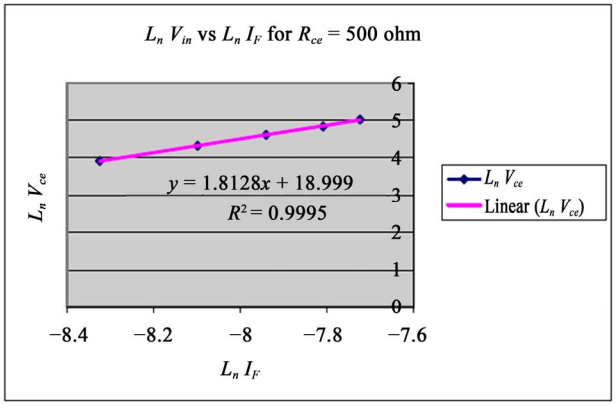


(a)

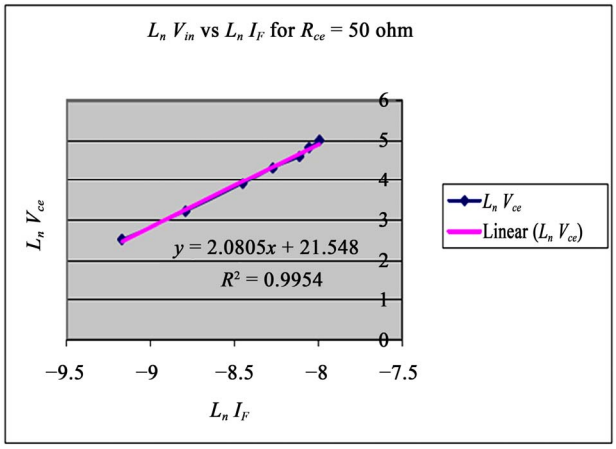


(b)

Figure 5. Approach to digital control of the harmonics at the output. (a) Processor and the control; (b) Flow chart.



(a)



(b)

Figure 6. Graphs of $\mathrm{Log_n}(V_{CE})$ versus $\mathrm{Log_n}(I_F)$ for two different R_{CE} values together with straight line fit in each case (a) For R_{CE} = 500 Ω; (b)For R_{CE} = 50 Ω.

Given these relationships for a particular case of a transistor array, the values of m and c can be fed into the digital control algorithm, in an overall arrangement as in **Figure 5(a)**. A look up table can store the experimental values for the particular array, and then derive the approximate values m and c suitable for each case of a straight line fit.

The above discussion leads towards the digital control approach to solve the linearity issue of the array, by controlling the two parameters m and c indicated above. Using a digital control algorithm, injected opto diode current can be controlled to adjust the instantaneous current through the array, by taking relatively larger number of samples of the AC voltage waveform via sampling. Overall effect of the processor based system is to control the opto diode current to achieve the expected impedance, based on the behaviour of the array as per **Figure 2(c)** during each sampling period. 1 kHz sampling rate was used in the proof of concept system. With the sampling of the instantaneous AC line voltage, microprocessor

program calculates the required opto diode current (output from the DAC) over each sampling period within the 50 or 60 Hz AC cycle. More details are available in [25] and a related US patent application.

Figure 7 compares the array performance with and without digital control at different resistance settings. It is clear from these oscillographs forms that the digital control technique reduces the harmonics in the waveform. These results were obtained in an electronic AC load capable of 150 VA capacity, based on an 8 bit Zilog Z8 Encore processor [25]. **Figure 8** indicates the fast Fourier transforms (FFT) of the current waveform at 1.3 A with and without the digital controller. This FFT plots indicates that the technique reduces the 3rd, 5th , 7th and 9th harmonic etc by significant amounts, proving that the algorithmic approaches used is clearly suitable. More information is available in [23].

Overall achievements in this work are:

1) A versatile AC impedance control technique which can be used in applications such as AVRs and power conditioners;

2) A new digital control technique where additional digital waveform control can be added to the system to minimize harmonics in the current waveforms.

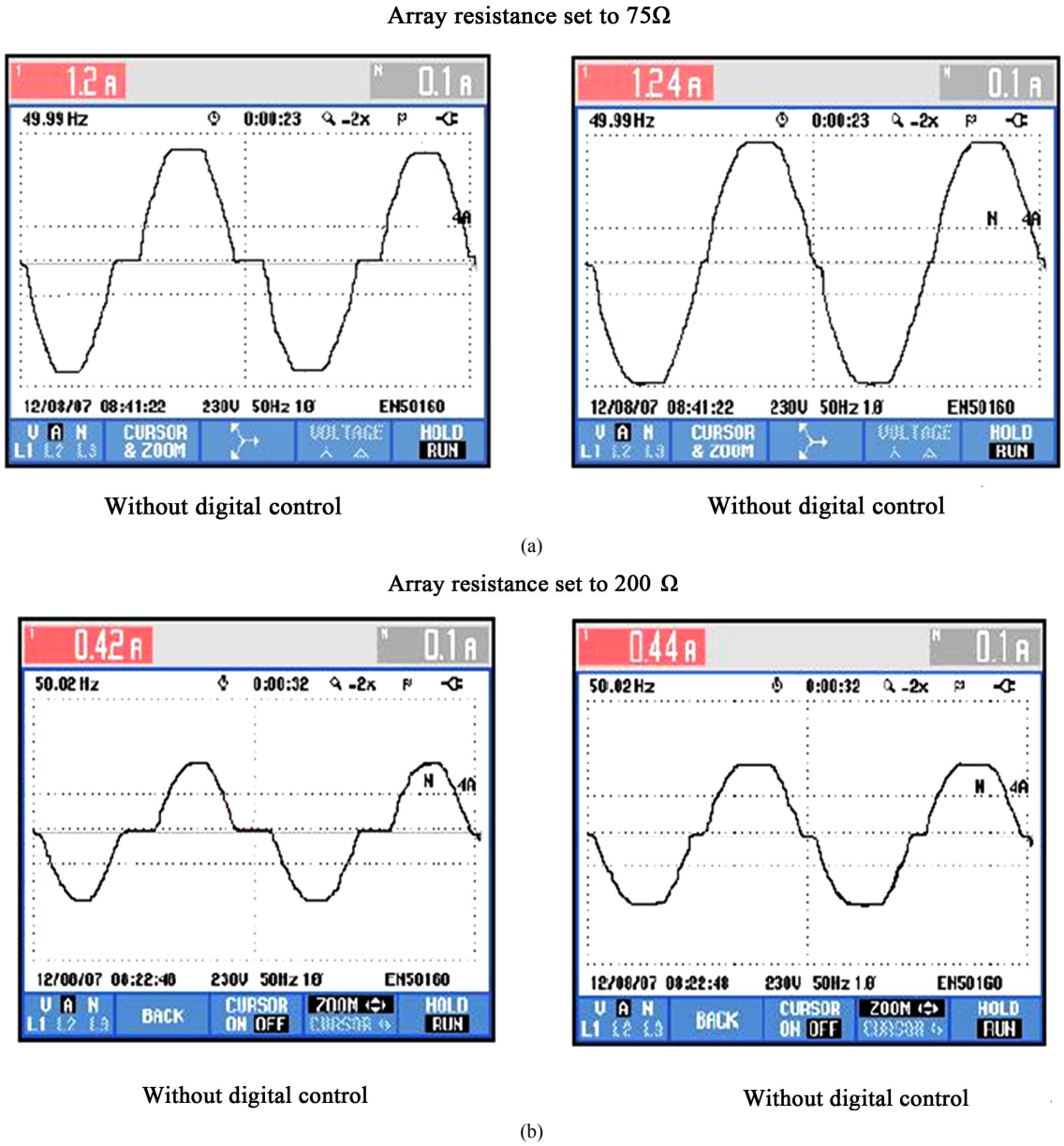


Figure 7. Current drawn by the array for a different setting of the array resistance with and without digital waveform correction (a)75 Ω setting; (b) 200 Ω setting control.

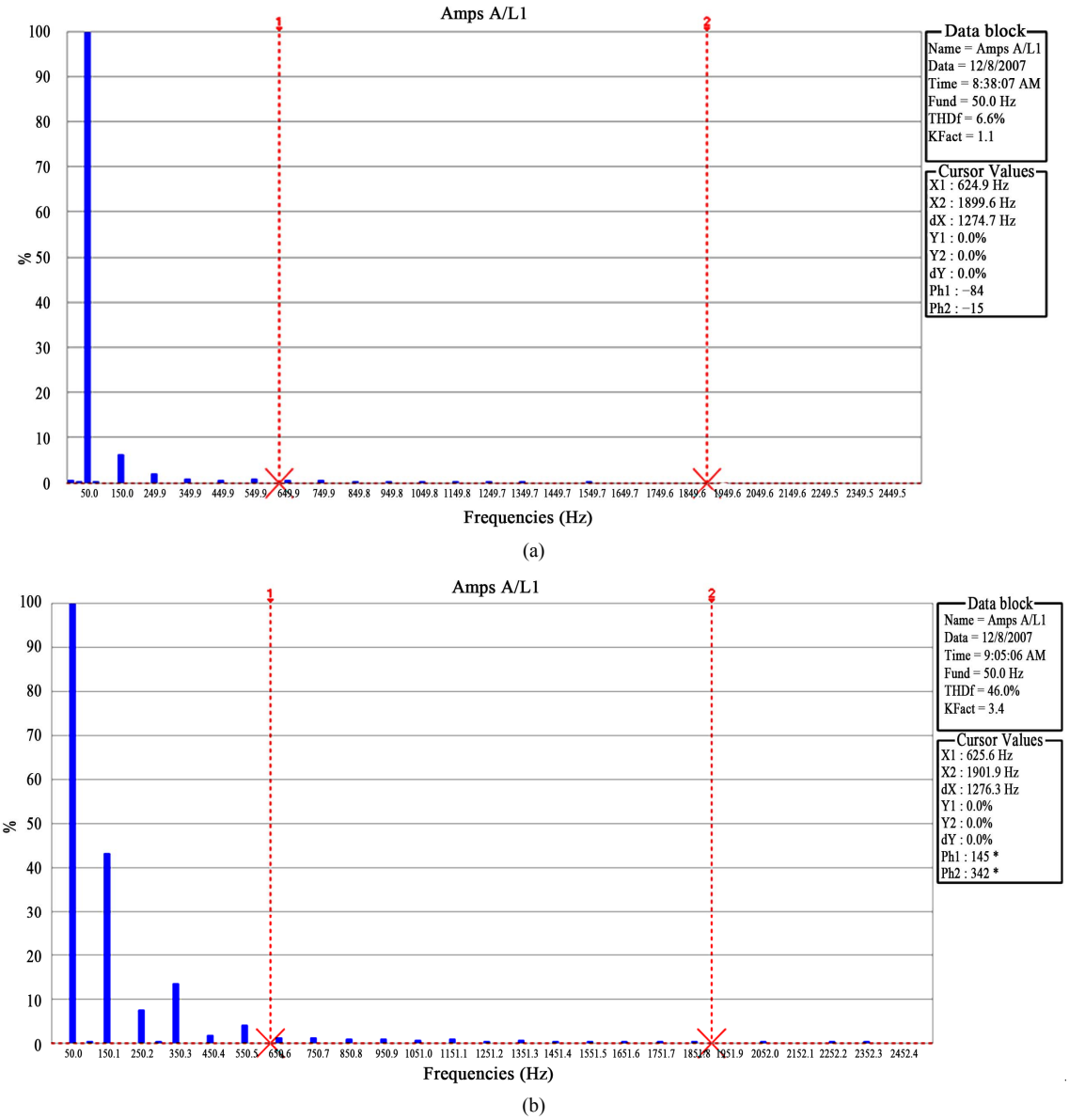


Figure 8. Comparison of the FFT of the current waveform at 1.3 A (a) with digital control; (b) without digital control.

7. Conclusions

The concept of using a series transistor array with opto isolator based isolation can be used in several AC power control applications suitable for low power and single phase requirements. Paper provides a general analysis of the array, and the design details of a 1 KVA capacity AVR prototype, which can be extended into other power levels. One secondary advantage of the technique is its ability to incorporate digital control algorithms to minimize harmonics due to the non linear nature of the power semiconductor array. Given these details, the technique could be used to develop AVRs with performance far superior to ferro-resonant versions and other slow responding transformer tap changers etc.

In addition, this technique has the potential to combine with common AVR techniques such as transformer tap changers etc for higher overall efficiency. Another possible application is in electronic AC loads with harmonic control.

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