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Voltage Controlled Ring Oscillator Design with Novel 3 Transistors XNOR/XOR Gates

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Abstract

In present work, improved designs for voltage controlled ring oscillators (VCO) using three transistors XNOR/XOR gates have been presented. Supply voltage has been varied from [1.8 - 1.2] V in proposed designs. In first method, the VCO design using three XNOR delay cells shows frequency variation of [1.900 - 0.964] GHz with [279.429 - 16.515] μW power consumption variation. VCO designed with five XNOR delay cells shows frequency variation of [1.152 - 0.575] GHz with varying power consumption of [465.715 - 27.526] μW. In the second method VCO having three XOR stages shows frequency variation [1.9176 - 1.029] GHz with power consumption variation from [296.393 - 19.051] μW. A five stage XOR based VCO design shows frequency variation [1.049 - 0.565] GHz with power consumption variation from [493.989 - 31.753] μW. Simulations have been performed by using SPICE based on TSMC 0.18μm CMOS technology. Power consumption and output frequency range of proposed VCOs have been compared with earlier reported circuits and proposed circuit's shows improved performance.

Keywords: CMOS, Delay Cell, Low Power, VCO, XOR and XNOR Gates

1. Introduction

The Phase locked loops (PLL) are widely used circuit component in data transmission systems and have extensive applications in data modulation, demodulation and mobile communication. Voltage control oscillators (VCO) are the critical and necessary building blocks of these PLL systems. Two widely used VCOs types are LC tank based and CMOS ring circuits. Combination of inductor and capacitor consumes large layout area in LC tank based oscillators [1-3]. CMOS ring based oscillators have advantages due to ease of controlling the output frequency and no requirement for on chip inductors [4,5]. CMOS based ring oscillators are easier to integrate and also gives wide tuning range. Due to flexibility of on chip integration, CMOS based ring oscillators have become essential building blocks in various battery operated mobile communication systems. Rising requirement of portable devices like cellular phones, notebooks, personal communication devices have aggressively enhanced attention for power saving in these devices. Power consumption in very large scale integration (VLSI) systems includes dynamic, static power and leakage power consumption. Dynamic power consumption results from switching of load capacitance between two different voltages and dependent on frequency of operation. Static power is contributed by direct path short circuits currents between supply (V_{dd}) and ground (V_{ss}) and it is dependent on leakage currents components [6,7]. VCOs being the major components in PLL system and is responsible for most of the power consumption. Some draw back of ring based oscillators includes large power consumption, phase noise and the limit of highest achievable frequency. In modern VCOs design power consumption and output frequency range are significant performance metrics [8-13]. A ring oscillator consist of delay stages, with output of last stage fed back to input of first stage. A VCO block diagram with single ended *N*-delay stages is shown in **Figure 1**.

The ring must provide a phase shift of 2π and unity voltage gain for oscillation occurrence. Each delay cell also gives a phase shift of π/*N*, where *N* is number of delay stages. The remaining π phase shift is provided by dc inversion using the inverter delay cells. For single

ended oscillator design the odd numbers of delay stage are required for dc inversion. Frequency of oscillation with N-single ended delay stages is given by $f_o = 1/(2Nt_d)$, where N is the number of delay stages and t_d is delay of each stage [9,14]. Delay stages are the basic building blocks in any VCO design and improved design of these delay cells will improve the overall performances of VCO. Various types of delay cells have been reported for VCO design including multiple-feed- back loops, dual-delay paths and single ended delays. These delay cells have been implemented by various approaches like simple inverter stage, latches, cross coupled cells etc. [15-18].

In present work modified VCOs circuits with three transistor XNOR/XOR delay cells have been presented with reduced the power consumption and wide output frequency range. The paper is organized as follows: In Section 2 three & five stages XNOR/XOR based ring VCOs have been presented. In Section 3 results for the three proposed VCOs have been obtained and comparisons with earlier reported structures have been made. Finally, in Section 4 conclusions have been drawn.

2. System Description

The frequency of single ended ring VCO is dependent on the delay provided by the each delay cell. In the proposed designs new delay cells based on three transistor XNOR/XOR gates have been used. Inverter operation has been implemented by XNOR/XOR gates. Direct path between V_{dd} and ground has been eliminated in proposed delay cells, due to which leakage power is reduced and the designs are power efficient. The circuits have been designed in 0.18 µm CMOS technology with supply voltage of 1.8 V. Supply voltage/control voltage has been varied from 1.8 to 1.2 V for obtaining the output frequency at different supply voltages.

First proposed delay cell is shown in **Figure 2**. XNOR delay stage is made up of two NMOS transistors and one PMOS transistor. Out of two input terminal of XNOR gate, one is connected to ground and signal is applied to other terminal. This circuits works as inverter without having direct path between V_{dd} and ground with saving in power consumption. A small capacitance of 0.01 pf at output of each delay cell has been included. The gate lengths of all three transistors have been taken as 0.18 µm. Widths (W_n) of NMOS transistors (N1 & N2) have been taken 2.5 µm and 0.5 µm respectively. Width (W_p) for transistor P1 has been taken as 1.0 µm. Output frequency is controlled by varying the supply voltage of XNOR delay stage. Three and five stages ring VCOs have been designed using proposed XNOR delay cell as shown in **Figures 3(a)** and **(b)**.

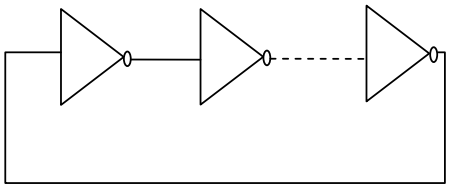


Figure 1. Block diagram of single ended VCO.

Figure 4 shows proposed XOR delay cell, which consist of two PMOS transistors (P1 & P2) and one NMOS transistor (N1). One input terminal of XOR gate is connected to control voltage (V_c) and signal is applied to other terminal so that circuit works as an inverter. The gate length of all three transistors has been taken as 0.18 µm in XNOR delay cell. Width (W_n) of NMOS transistor N1 has been taken 0.25 µm. Width (W_p) for P1 & P2 transistors has been taken as 2.0 µm. Output frequency is controlled by varying the control voltage (V_c) of second input terminal of XOR delay stage. Three and five stages ring VCOs have been designed using proposed XOR delay cell as shown in **Figures 5(a)** and **(b).**

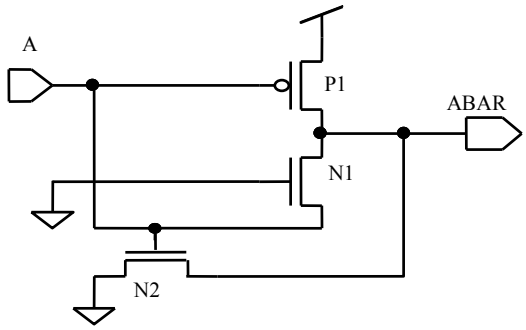
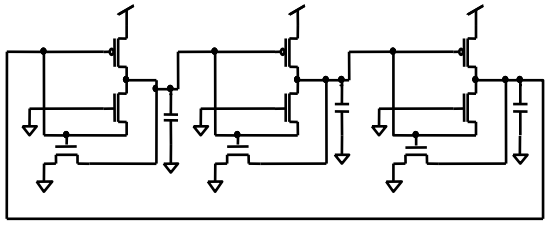
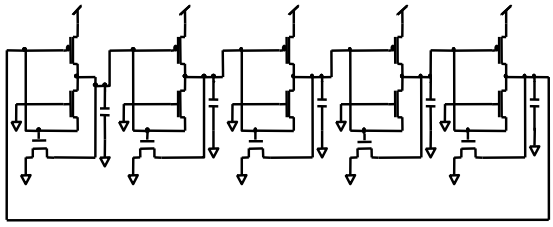


Figure 2. Proposed delay cell based on XNOR gate.



(a)



(b)

Figure 3. (a) 3 stages, (b) 5 stages ring VCO based on XNOR gate delay cell.

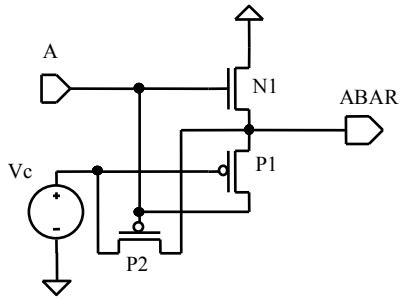


Figure 4. Proposed delay cell based on XOR gate.

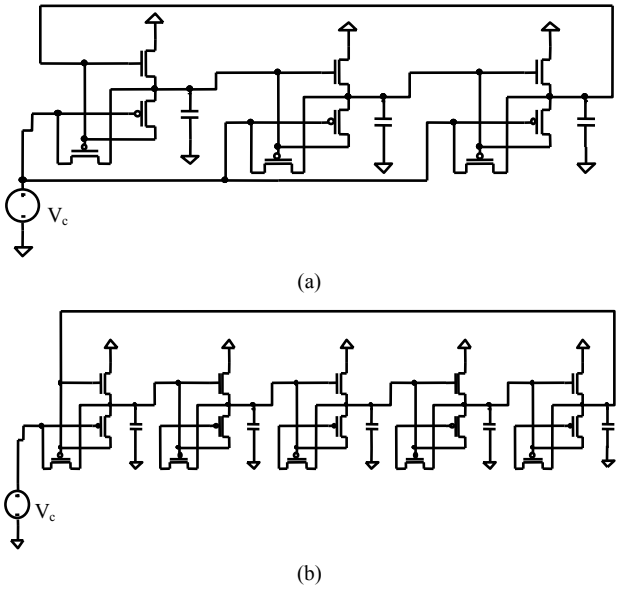


Figure 5. (a) 3 stages, (b) 5 stages ring VCO with on XOR gate delay cell.

3. Results and Discussions

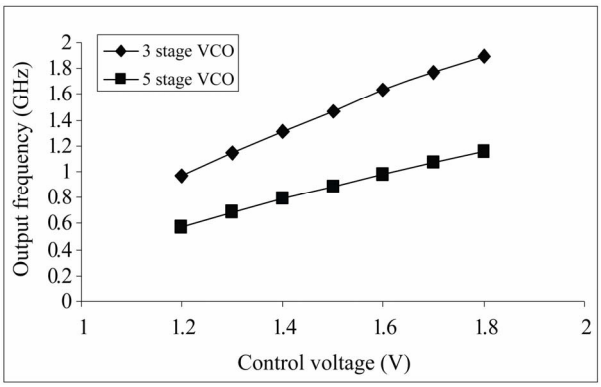
Simulations have been performed using SPICE based on TSMC 0.18 μm technology with supply voltage variations from [1.8 - 1.2] V. **Table 1** shows the results for three and five stages VCOs designed with XNOR delay cells. Supply /control voltage (V_c) has been varied from [1.8 - 1.2] V. Output frequency of three stage VCO shows variation from [1.900 - 0.964] GHz with power consumption variation of [279.429 - 16.515] μW. In five stages ring VCO frequency shows variation from [1.152 - 0.575] GHz with varying power consumption [465.715 - 27.526] μW. **Figures 6(a)** and **(b)** shows frequency and power consumption variation for three and five stages XNOR based ring VCOs.

Figure 7 shows output waveform for three & five stages XNOR VCOs at supply voltage of 1.8 V.

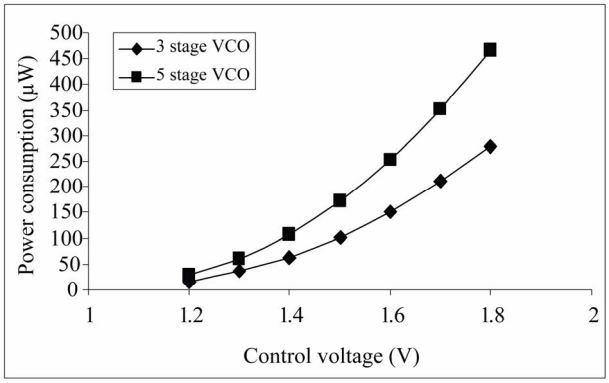
Table 2 shows results for three and five stages ring VCOs designed with XOR delay cells. Control voltage at the second input terminal of delay cells has been varied from [1.8 - 1.2] V. In three stage VCO, output frequency shows variation [1.917 - 1.029] GHz with varying power consumption of [296.393 - 19.051] μW. For five stage XOR VCO frequency varies from [1.049 - 0.565] GHz with varying power consumption of [493.989 - 31.753] μW. **Figures 8(a)** and **(b)** shows frequency and power consumption variation for three and five stages XOR based ring VCOs. **Figure 9** shows output waveform for three & five stages XOR based VCO at supply voltage of 1.8 V.

Table 1. Results for XNOR delay based VCO.

Control voltage (V)	Three stages XNOR VCO		Five stages XNOR VCO	
	Output frequency (GHz)	Power consumption (μW)	Output frequency (GHz)	Power consumption (μW)
1.8	1.900	279.429	1.152	465.715
1.7	1.773	210.349	1.071	350.582
1.6	1.632	151.432	0.978	252.388
1.5	1.469	102.570	0.884	170.950
1.4	1.312	63.786	0.789	106.311
1.3	1.144	35.179	0.686	58.632
1.2	0.964	16.515	0.575	27.526

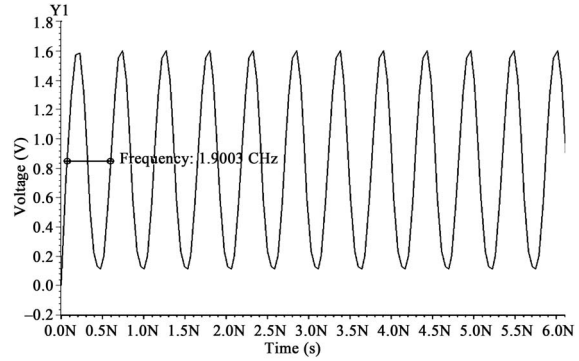


(a)

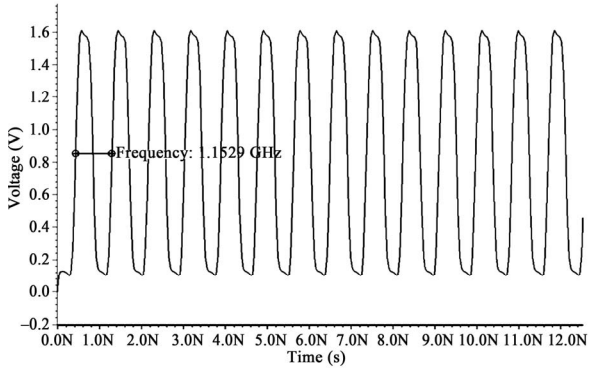


(b)

Figure 6. (a) Frequency, (b) power consumption variations of 3 and 5 stages XNOR based VCO.



(a)

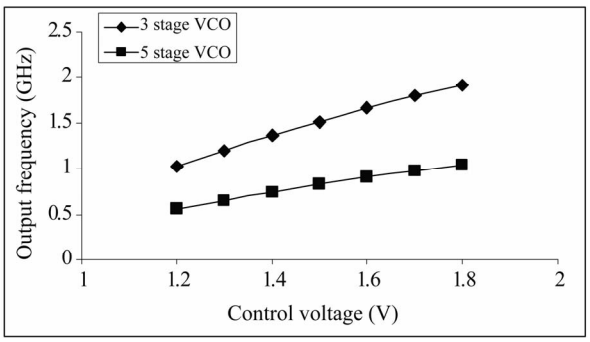


(b)

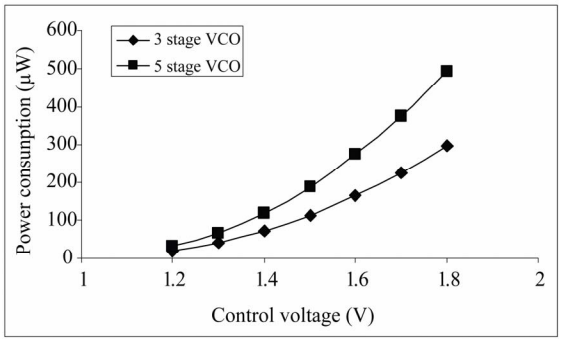
Figure 7. Wave forms at 1.8 V for (a) 3 stages XNOR VCO, (b) 5 stages XNOR VCO.

Table 2. Results for XOR delay based VCO.

Control Voltage (Vc) (V)	Three stages XOR VCO		Five stages XOR VCO	
	Output frequency (GHz)	Power Consumption (μW)	Output frequency (GHz)	Power Consumption (μW)
1.8	1.917	296.393	1.049	493.989
1.7	1.794	225.614	0.981	376.023
1.6	1.660	164.559	0.908	274.266
1.5	1.507	113.140	0.827	188.568
1.4	1.363	71.500	0.747	119.167
1.3	1.202	40.054	0.656	66.757
1.2	1.029	19.051	0.565	31.753

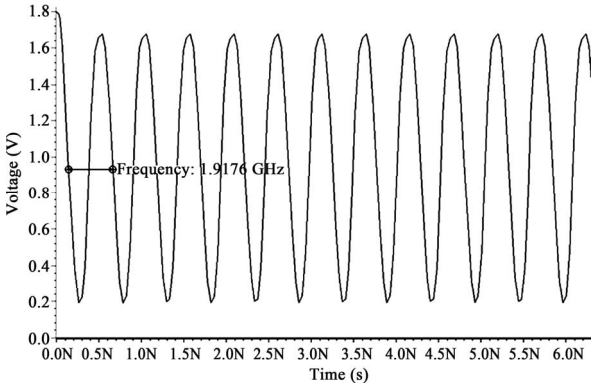


(a)

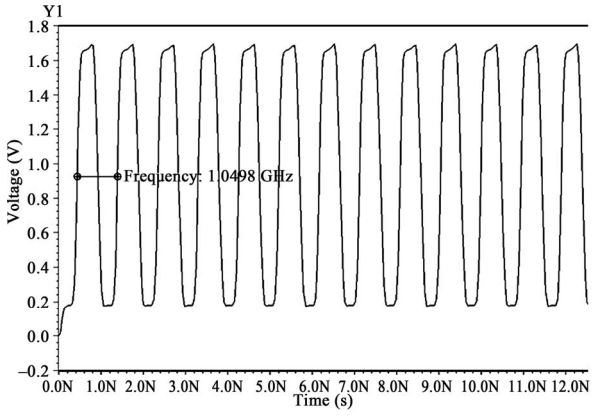


(b)

Figure 8. (a) Frequency, (b) power consumption variations of 3 and 5 stages XOR VCOs.



(a)



(b)

Figure 9. Wave forms at 1.8 V for (a) 3 stages, (b) 5 stages XOR VCO.

In reported circuits, power consumption is increasing with increase in number of delay stages whereas output frequency is showing downward trend. Number of stages may be decreased or increased depending upon the application, requirement for frequency range and power consumption. A comparison with earlier reported circuits in terms of power consumption and output frequency range is given in **Table 3**. Proposed circuits' shows better

Table 3. Comparison of VCO performance.

VCO designs	Operating frequency (GHz)	Vdd (V)	Technology (µm)	Power consumption
[1]	2.17 - 2.73	0.9	0.18	2.7 mW
[5]	0.39 - 1.41	1.8	0.18	12.5 mW
[10]	0.12 - 1.3	0.5	0.18	0.085 mW
[13]	1.57 - 3.57	1.8	0.090	16.8 mW
[16]	0.65 - 1.6	1.8	0.18	39 mW
Present work [3 stages XNOR]	1.900 - 0.964	1.8	0.18	[279.429 - 16.515] µW
Present work [5 stages XNOR]	1.152 - 0.575	1.8	0.18	[465.715 - 27.526] µW
Present work [3 stages XOR]	1.917 - 1.029	1.8	0.18	[296.393 - 19.051] µW
Present work [5 stages XOR]	1.049 - 0.565	1.8	0.18	[493.989 - 31.753] µW

performance in terms of power consumption and output frequency range than compared circuits.

4. Conclusions

In reported work improved power efficient designs for three and five stages CMOS ring VCOs have been presented. In first methodology design with XNOR delay stages have been presented. Three stages VCO with XNOR shows frequency variation [1.900 - 0.964] GHz with deviation in power consumption from [279.429 - 16.515] µW. Five stages XNOR delay based VCO gives output frequency range [1.152 - 0.575] GHz with power consumption variation [465.715 - 27.526] µW. In the second methodology VCO designed with three stages XOR based delay cell shows frequency variation [1.917 - 1.029] GHz with power consumption variation [296.393 - 19.051] µW. Finally the VCO designed with five stages XOR delay cells shows frequency variation [1.049 - 0.565] GHz with power consumption variation [493.989 - 31.753] µW. Proposed designs have been compared with previously reported design and present approach shows significant power saving with wide tuning range.

5. References

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