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A Thyristor-Only Input ESD Protection Scheme for CMOS RF ICs*

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Abstract

We propose an input protection scheme composed of thyristor devices only without using a clamp NMOS device in order to minimize the area consumed by a pad structure in CMOS RF ICs. For this purpose, we suggest low-voltage triggering thyristor protection device structures assuming usage of standard CMOS processes, and attempt an in-depth comparison study with a conventional thyristor protection scheme incorporating a clamp NMOS device. The comparison study mainly focuses on robustness against the HBM ESD in terms of peak voltages applied to gate oxides in an input buffer and lattice heating inside protection devices based on DC and mixed-mode transient analyses utilizing a 2-dimensional device simulator. We constructed an equivalent circuit for the input HBM test environment of the CMOS chip equipped with the input ESD protection devices. And by executing mixed-mode simulations including up to four protection devices and analyzing the results for five different test modes, we attempt a detailed analysis on the problems which can occur in real HBM tests. We figure out strength of the proposed thyristor-only protection scheme, and suggest guidelines relating the design of the protection devices and circuits.

Keywords: ESD Protection, HBM, Thyristor, Mixed-Mode Simulation, RF ICs

1. Introduction

CMOS chips are vulnerable to electrostatic discharge (ESD) due to thin gate oxides used, and therefore protection devices such as NMOS transistors are required at input pads. A large size for the protection devices is needed to reduce discharge current density and thereby to protect them against thermal-related problems. However, using a large size tends to increase parasitic capacitances added to input nodes generating problems such as gain reduction and poor noise characteristics in RF ICs [1].

To reduce the added parasitics, the protection schemes utilizing thyristor or diode protection devices were suggested [2,3] and have been used as fundamental protection schemes in RF ICs. In the protection scheme utilizing thyristor or diode protection devices, it is conventional to include a V_{DD}-V_{SS} clamp NMOS device in the input pad structure to provide discharge paths for all possible human-body model (HBM) test modes [4]. A large size for the clamp NMOS device is essential to prevent thermal device failure. Even though the clamp NMOS device does not add parasitics to the input node since it is not connected to it, adopting a large size makes the design to consume an excessive area for the pad structure. This requirement can be a serious limitation in a chip where a pad size is a critical issue in chip design.

In this paper, we suggest an input protection scheme utilizing low-voltage triggering thyristor devices only without using a clamp NMOS device in input pad structure. This scheme can be implemented into input pad structures of CMOS RF ICs to provide protection against HBM and MM (Machine mode) discharge events. We present a comparative analysis result of the proposed scheme and the conventional thyristor protection scheme incorporating a clamp NMOS device. The characteristics of the latter scheme are already presented in [4].

A 2-dimensional device simulator, together with a circuit simulator, is utilized as a tool for the comparative analysis. The analysis methodology utilizing a device simulator has been widely adopted with credibility [4-6] since it provides valuable information relating the mechanisms leading to device failure, which cannot be obtained by measurements only.

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In Section 2, we suggest low-voltage triggering thyristor protection device structures assuming usage of standard CMOS processes, and introduce device characteristics based on DC device simulations. In Section 3, we briefly explain discharge modes in HBM tests and introduce two input protection scheme utilizing the suggested protection devices. In Section 4, we construct an equivalent circuit model for CMOS chips equipped with the input protection devices to simulate various input HBM test situations, and execute mixed-mode transient simulations. Based on the simulation results, we figure out weak modes in real discharge tests, and present in-depth analysis results relating critical characteristics such as peak voltages developed across gate oxides in input buffers, locations of peak temperature inside protection devices, and so on. In Section 5, based on the simulation results, considerations relating device and circuit design are discussed.

2. Protection Device Structures and DC Characteristics

Figure 1 shows the NMOS protection device structure assumed in this work, which is utilized as a V_{DD}-V_{SS} clamp device. The structure is same with the one suggested in [4]. The p^+ junctions located at the upper left/right corners represent diffusions for substrate ground contacts. A series resistor of 1 MΩ·μm, which is not shown in **Figure 1**, is connected at the bottom substrate node considering distributed resistances leading to substrate contacts located far away.

DC simulations were performed using a 2-dimensional device simulator ATLAS [7]. All necessary physical models including an impact ionization model and lattice-heating models were included in the simulations. The source, the gate, and the substrate were grounded, and the drain bias was varied for simulation.

Figure 2 shows simulated drain current vs. voltage characteristics of the NMOS device in **Figure 1** in a semi-log scale. The underlying physics relating the characteristics in **Figure 2** are fully explained in [4] previously. The device shows an n^+-drain/p-sub junction breakdown when the drain voltage is increased above 9.3 V. A generated hole current by avalanche flows to the substrate terminal to increase the body potential. With a sufficient hole current flowing, a parasitic lateral npn bipolar transistor is triggered. The source, the body, and the drain act as an emitter, a base, and a collector, respectively. As the BJT is being triggered, the required drain-source voltage is reduced to show a snapback, as indicated as "BJT trigger" in **Figure 2**. After the snapback at about 9.4 V, the drain-source voltage drops to about 4.6 V of a bipolar holding voltage.

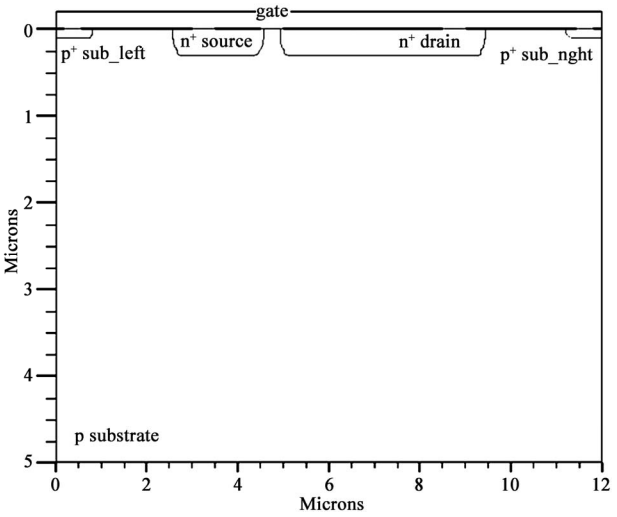

Figure 1. Cross section of the NMOS device.

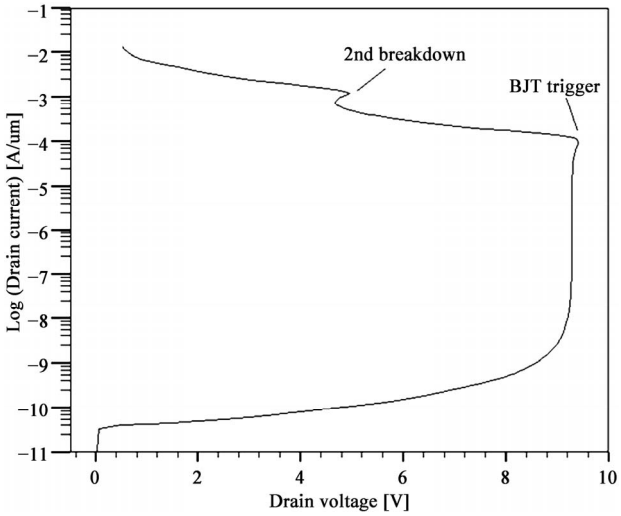

Figure 2. Drain I-V characteristics of the NMOS device.

Figure 3 shows the lvtr_thyristor_down device structure assumed in this work, which is used as a protection device between an input pad and a V_{SS} node. An lvtr_thyristor device is a pnpn-type device suggested to lower the snapback voltage by incorporating an NMOS transistor into it [2]. The drain/gate/source NMOS structure composed of the n^+ well (n^+ region at the right-hand corner of the n well), the gate, and the n^+ cathode is similar to the NMOS structure in **Figure 1**. However, it does not incorporate ESD implant steps, which is implied by the relatively shallow junctions. The structure shown in **Figure 3** is same with the one of the lvtr_thyristor device suggested in [4]. The NMOS gate oxide thickness, the gate length, the effective channel length, and the channel peak doping are same with those in **Figure 1**. A series resistor is also connected at the bottom substrate node as in the NMOS device in **Figure 1**.

The n^+ and p^+ anodes in **Figure 3** are tied together to serve as an anode. The cathode, the gate, and the substrate were grounded, and the anode bias was varied for simulation.

Figure 4 shows the simulated DC anode current vs. voltage characteristics of the lvtr_thyristor_down device in **Figure 3**. The underlying physics relating the characteristics in **Figure 4** are fully explained in [4] previously. The device shows an n^+-drain/p-sub junction breakdown when the anode voltage is increased to above 8.8 V. With a sufficient hole current flowing to the substrate terminal, the p-sub/n^+-cathode junction is forward biased triggering a lateral npn bipolar transistor. The n^+ well, the p substrate, and the cathode act as a collector, a base, and an emitter, respectively. At this situation, a snapback is monitored as shown in **Figure 4**. The collector current from the n^+ anode flows through the n well to decrease the potential of the region under the p^+ anode by an ohmic drop. When the collector current is large enough, the p^+-anode/n-well junction is forward biased to trigger a pnpn (p^+-anode/n-well/p-sub/n^+-cathode) thyristor, which causes another decrease in the anode voltage, as indicated as "pnpn trigger" in **Figure 4**. The resulting holding voltage drops to about 1 V, which is much smaller compared to 4.6 V of the NMOS device in **Figure 2**.

We note here that the device shown in **Figure 3** includes a well conducting thyristor by virtue of the larger n^+–p^+ anode space. This is verified by the fact that the current level for the pnpn trigger is not much higher than that for the bipolar trigger in **Figure 4**. As the anode space decreases, the current level for the pnpn trigger increases [8].

If we want to use the lvtr_thyristor_down device in **Figure 3** as a protection device between a V_{DD} node and a pad in a thyristor-only protection scheme, we should

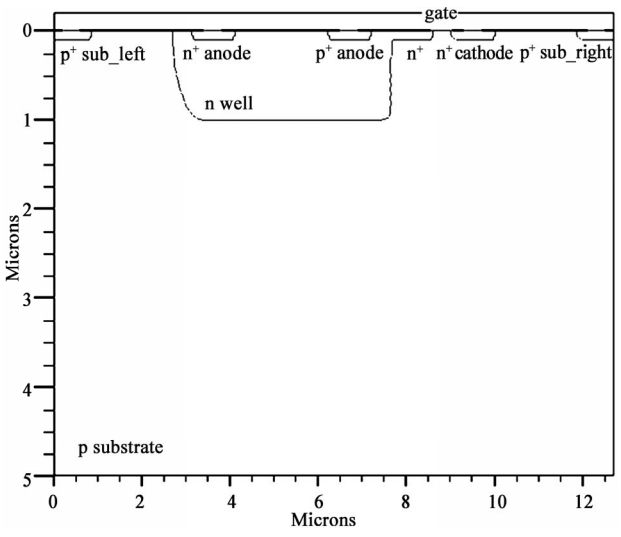

Figure 3. Cross section of the lvtr_thyristor device.

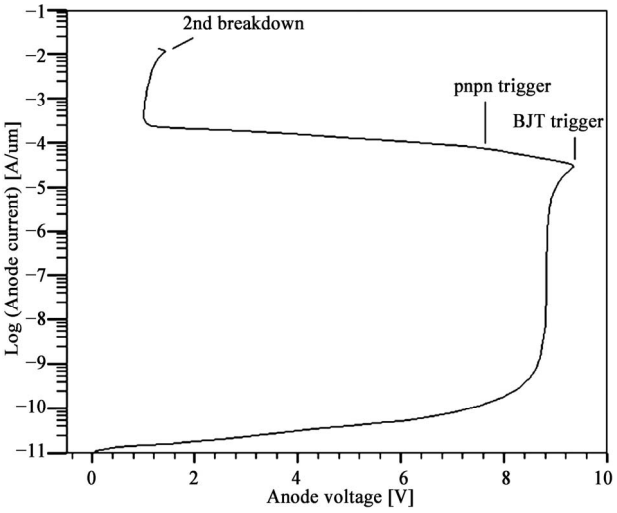

Figure 4. Anode I-V characteristics of the lvtr_thyristor device.

connect the p^+ anode and the n^+ anode to a V_{DD} node, and n^+ cathode to a pad, and the common p substrate to a V_{SS} node. In this case, however, we found that a serious problem occurs in a PD mode (a positive ESD voltage applied to a pad with a V_{DD} pin grounded) since there is no forward diode path from the pad to the V_{DD} node. Without the forward diode path provided, an npn (n^+-cathode/p-sub/n^+-anode) bipolar transistor conducts from the pad to the V_{DD} node to cause a thermal-related problem with a larger holding voltage. **Figure 5** shows the lvtr_thyristor_up device, which is suggested in this work to solve the problem. The device apparently includes a forward diode path from the cathode to the anode.

As we can see in **Figure 5**, the device needs addition of a p base region, which is provided in most of standard CMOS processes below 0.35 μm to allow forming simple bipolar transistors. Depth of the p-base region was assumed as 0.5 μm, and the base is assumed to have a channel peak doping of 2.35×10^{17} cm^{-3}, which is similar to that of the NMOS structure in the lvtr_thyristor_down device. Doping profiles of the n well, the n^+ and p^+ junctions are same with those in the the lvtr_thyristor_down device.

The NMOS transistor, which is incorporated in the device to lower the snapback voltage, is located inside the p base. The n^+ well (n^+ region at the left-hand corner of the p base), the gate, and the n^+ cathode play the role of the drain, the gate, and the source, respectively. The NMOS structure in the device is very similar to that in the lvtr_thyristor_down device except a small difference in the acceptor doping profile in the body region. We note that, in deep n-well processes, a p well separated from a p substrate can replace the p base.

The n^+ and p^+ anodes in **Figure 5** are tied together to serve as an anode. The n^+ and p^+ cathodes, the gate, and the substrate were grounded, and the anode bias was varied for simulation.

Figure 6 shows the simulated DC anode current vs. voltage characteristics of the lvtr_thyristor_up device in **Figure 5**. The characteristics and the underlying physics are very similar to those of the lvtr_thyristor_down device except that an npn bipolar transistor is formed by the n^+-well/p-base/n^+-cathode structure and a pnpn thyristor is formed by the p^+-anode/n-well/p-base/n^+-cathode structure. The breakdown voltage in this device corresponds to that of the n^+-well/p-base junction.

Table 1 summarizes the principal DC characteristics of the three protection devices.

3. ESD Protection Schemes

Since parasitics added to an input pad should be minimized, it is desired to connect fewer number of protection devices to an input pad. An effective way to reduce the number is to use a V_{DD}-V_{SS} clamp device since it provides discharge paths without adding parasitics to an input pad. **Figure 7** shows a popular ESD protection scheme utilizing a thyristor device, which minimizes the added parasitics and is chosen for a comparison study with the thyristor-only protection scheme in this work. A CMOS inverter was assumed as an input buffer.

The lvtr_thyristor_down device in **Figure 3** is used for T_1 in **Figure 7**. The NMOS device in **Figure 1** is used for M_2. In M_2, the drain is connected to V_{DD}, and the gate, the source, and the substrate are connected to V_{SS}. In T_1, the p^+ and n^+ anodes are connected to the pad, and the p substrate and the n^+ cathode are connected to V_{SS}. The NMOS gate (G_1) in T_1 is also connected to V_{SS} to maintain an off state in normal operations.

It is important to locate all the protection devices close to the pad to minimize variation of the gate voltage in the input buffer when an ESD voltage is applied to the pad. Even though same discharge paths can be provided with V_{DD}-V_{SS} clamp devices located in other places, there exists an enhanced danger of oxide failure since the voltage applied to the gate oxide of the input buffer may increase due to added high voltage drops in power bus lines with a large discharge current flowing.

Figure 8 shows the thyristor-only protection scheme suggested in this work. The lvtr_thyristor_down device in **Figure 3** is used for T_1, and the lvtr_thyristor_up device in **Figure 5** is used for T_2. Connection of T_1 is same as that in **Figure** 7. In T_2, the p^+ and n^+ anodes are connected to V_{DD}, and the p^+ and n^+ cathodes are connected to the pad. The NMOS gate (G_2) in T_2 is connected to the pad to maintain an off state in normal operations. Although it is not shown in **Figure 8**, the p substrate in T_2 is connected to V_{SS}.

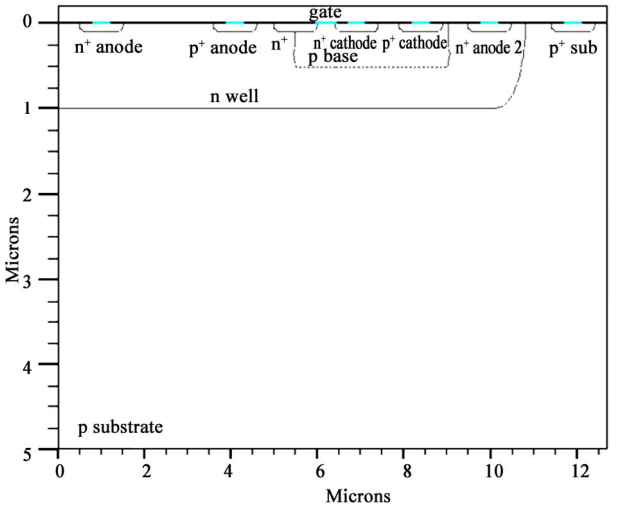

Figure 5. Cross section of the diode device.

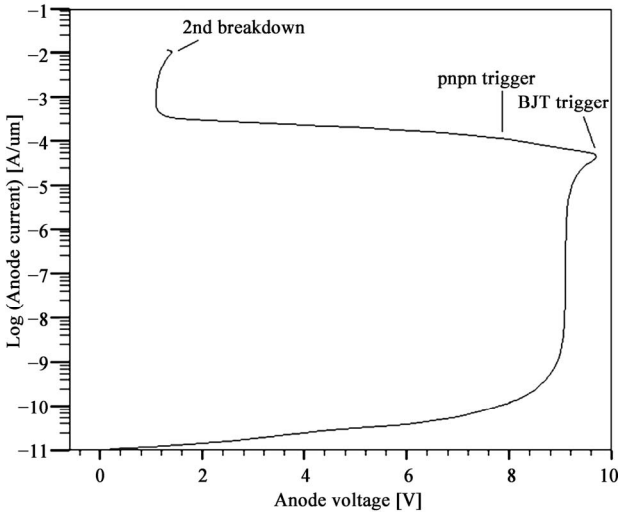

Figure 6. Anode current-voltage characteristics of the lvtr_ thyristor_up device.

Table 1. Principal principal DC characteristics of the protection devices.

Protection device	Holding Voltage	Breakdown voltagee	Snapback voltagee
NMOS	4.6 V	9.3 V	9.4 V
lvtr_thyristor_down	1.0 V	8.8 V	9.4 V
lvtr_thyristor_up	1.1 V	9.1 V	9.7 V

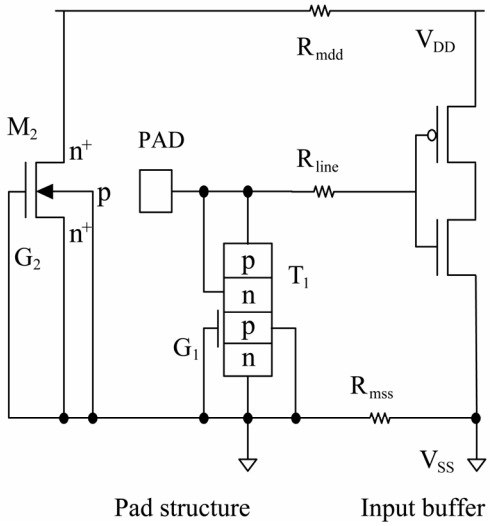

Figure 7. Protection scheme (1) utilizing a thyristor device.

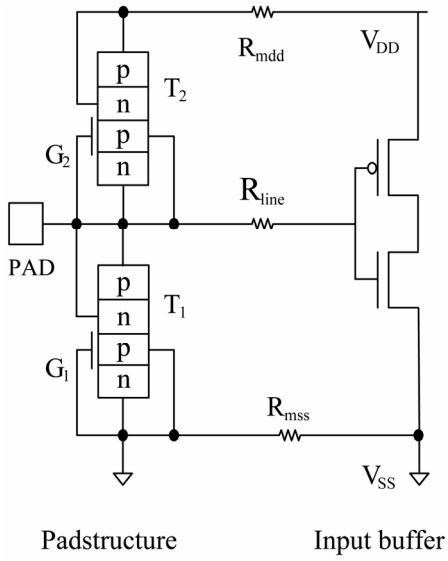

Figure 8. Protection scheme (2) utilizing thyristor devices only.

Input protection schemes utilizing thyristor devices only had been suggested [9,10]; however the trigger voltages of the suggested devices are too high [9] to be used in recent technologies, or the trigger voltages for the two LVTSCR thyristor devices are uneven [10] due to a difference in hole and electron mobilities resulting uneven trigger voltage for different HBM test modes, which is certainly not beneficial, and the PMOS-triggered thyristor structure does not provide a forward diode path from a pad to a V_{DD} node [10] to make the complementary-LVTSCR structure hard to be optimized.

While the amount of added capacitance to an input pad is expected to increase to about twice of that in case of using the protection scheme (1), the area consumed by a pad structure is expected to be reduced a lot by eliminating the clamp NMOS device, and the peak voltages applied to gate oxides of input buffers can be reduced somewhat since the series clamp NMOS device disappears in a discharge path.

Since HBM tests for input pins should include all possible discharge modes, tests are performed for five modes defined as PS, NS, PD, ND, and PTP modes [4].

Main discharge paths for test modes in each protection scheme are shown in **Figures 9** and **10**.

Figure 9 shows main discharge paths for each test mode when using the protection scheme (1). In a PS mode, a pnpn thyristor in T_1 provides a main discharge path, and in an NS mode, a forward-biased pn (p^+-sub/n^+-anode) diode in T_1 provides it. In a PD mode, a pnpn thyristor in T_1 and a forward-biased pn (p^+-sub/n^+-drain) diode in M_2 in series provide a main discharge path, and in an ND mode, a parasitic npn bipolar transistor in M_2 and a forward-biased pn (p^+-sub/n^+-anode) diode in T_1 in series provides it. In a PTP mode, a pnpn thyristor in T_1 and a forward-biased pn (p^+-sub/n^+-anode) diode in T_3, which is located in the other pad, in series provide a main discharge path.

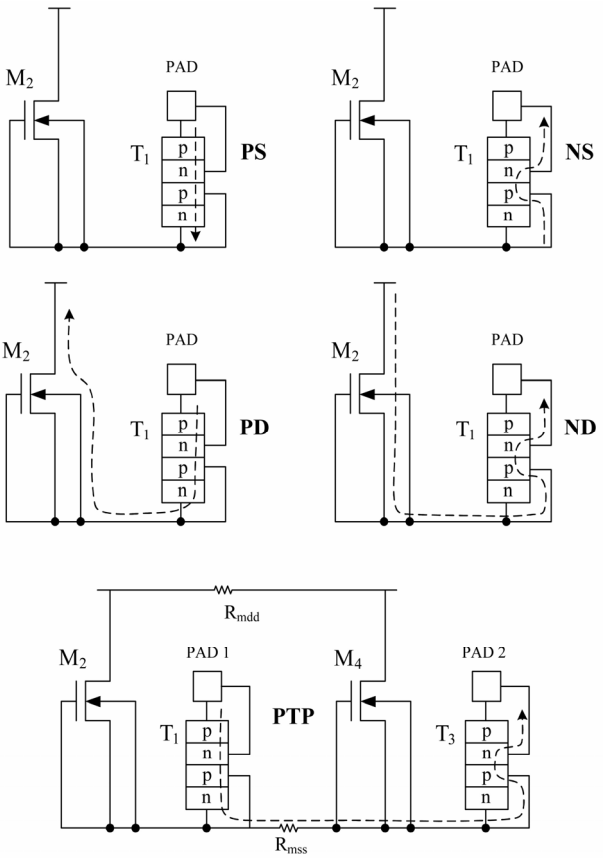

Figure 9. Main discharge paths for each test mode in the protection scheme (1).

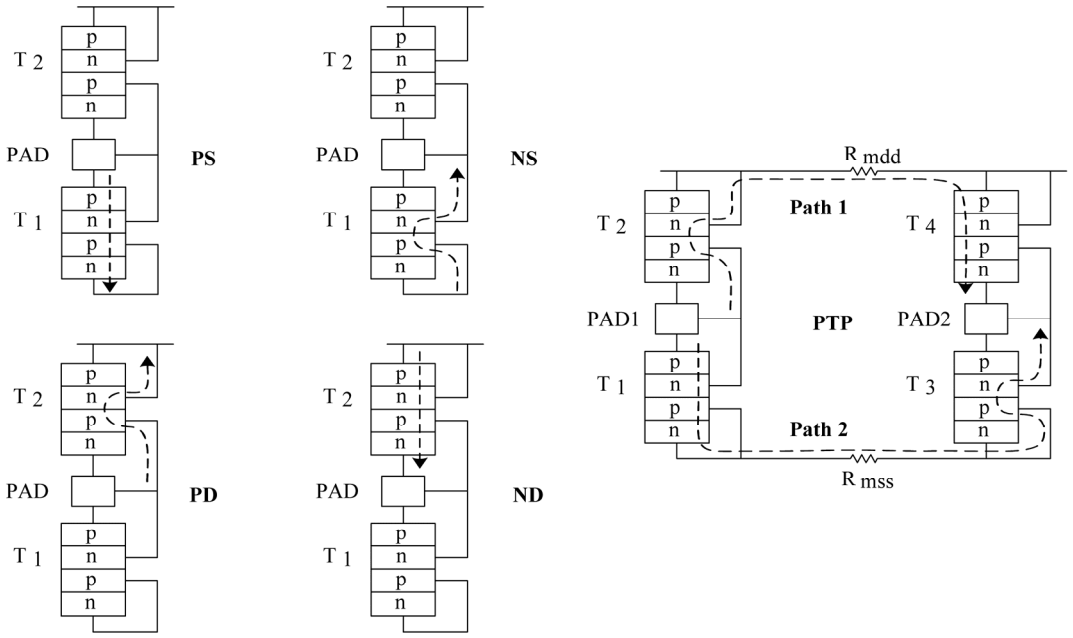

Figure 10. Main discharge paths for each test mode in the protection scheme (2).

Local lattice heating is proportional to a product of current density and electric field intensity, and therefore temperature-related problems in the protection devices can occur in the parasitic npn bipolar transistor rather than in the forward-biased diode or in the pnpn thyristor since the holding voltage of the bipolar transistor is much larger. Therefore the width of the lvtr_thyristor_down device can be small, however, we should assign a sufficient device width to M_2 considering an ND mode.

Figure 10 shows main discharge paths for each test mode when using the protection scheme (2). In a PS mode, a pnpn thyristor in T_1 provides a main discharge path, and in an NS mode, a forward-biased pn (p^+-sub/n^+-anode) diode in T_1 provides it. In a PD mode, a forward-biased pn (p^+-cathode/n^+-anode) diode in T_2 provides a main discharge path, and in an ND mode, a pnpn thyristor in T_2 provides it. In a PTP mode, there exist two main discharge paths. One is a series path composed of a forward-biased pn (p^+-cathode/n^+-anode) diode in T_2 and a pnpn thyristor in T_4, and the other is a series path composed of a pnpn thyristor in T_1 and a forward-biased pn (p^+-sub/n^+-anode) diode in T_3.

Since the holding voltages of the thyristor devices are not large, widths of all the thyristor devices don't need to be large.

4. Mixed-Mode Transient Simulations

Figure 11 shows an equivalent circuit of an input HBM test situation assuming a PS mode, which is fully explained in [4] previously. V_{ESD} is a HBM test voltage, and a switch S_1 charges C_{ESD} and then a switch S_2 initiates discharge. By utilizing time-varying resistors for the switches, the switching times of S_1 and S_2 were set short as 0.15 ns.

In **Figure 11**, a V_{DD}-V_{SS} clamp NMOS protection device M_2 and a protection device T_1 form a representative protection circuit in the input pad, assuming usage of the protection scheme (1). In case of using the protection scheme (2), M_2 is eliminated, and the additional protection device T_2 should be inserted between the V_{DD} node and the pad.

A CMOS inverter is assumed as an input buffer inside a chip, which is modeled by a capacitive network. C_{ngate} and C_{pgate} represent gate-oxide capacitances of an NMOS transistor and a PMOS transistor, respectively. C_{ds} represents an n-well/p-sub junction capacitance. 0.1 pF, 0.1 pF, and 0.01 pF were assumed for C_{ngate}, C_{pgate}, and C_{ds}, respectively.

Using ATLAS, we performed mixed-mode transient simulations utilizing the equivalent circuit in **Figure 11** equipped with two different input protection circuits shown in **Figures 7** and **8**. When a mixed-mode simulation is performed, the active protection devices are solved by device and circuit simulations simultaneously.

For all the mixed-mode transient simulations performed for each test mode, $V_{ESD} = \pm 2000$ V was assumed. To have fair comparison on ESD robustness of the different protection schemes, widths of the protection devices were adjusted to maintain utmost peak lattice temperature inside the protection devices below 500 K in all the mixed-mode simulations, resulting 250 μm, 20 μm, and 20 μm for M_2, T_1, and T_2, respectively.

As an example of the mixed-mode simulation results, **Figure 12** shows variation of the anode current of T_1 as a function of time in a PS mode in case of using the protection circuit (1) in **Figure 7**. The anode current peaks up to 1.37A, and shows decaying characteristics with a time constant of roughly $R_{ESD}C_{ESD}$ = 0.15 μs, which can be expected from the equivalent circuit in **Figure 11**.

Figure 13 shows variations of the voltages developed across C_{ngate} and C_{pgate} in the input buffer from the same simulation result. In **Figure 13**, the pad voltage is not shown since it is almost same with the voltage developed across C_{ngate}.

From the DC simulation result in **Figure 4**, we can estimate transient discharge characteristics of T_1, which lies in the main discharge path in this case. When a positive ESD voltage is applied, the developed voltage across the device will increases at least up to the snapback voltage (9.4 V). As the bipolar transistor and the pnpn thyristor are triggered in order, the developed voltage will drop down to the holding voltage (1 V) and main discharge will proceed. In the later stage of discharge when the discharge current decreases below the holding current for the thyristor action, the developed voltage will increase again at most up to the snapback voltage (9.4 V) and will remain constant around the breakdown voltage (8.8 V) for some duration even though the discharge current decreases. As the discharge current decreases further, the device will go out of the breakdown mode and the developed voltage will decrease towards zero to end the discharge.

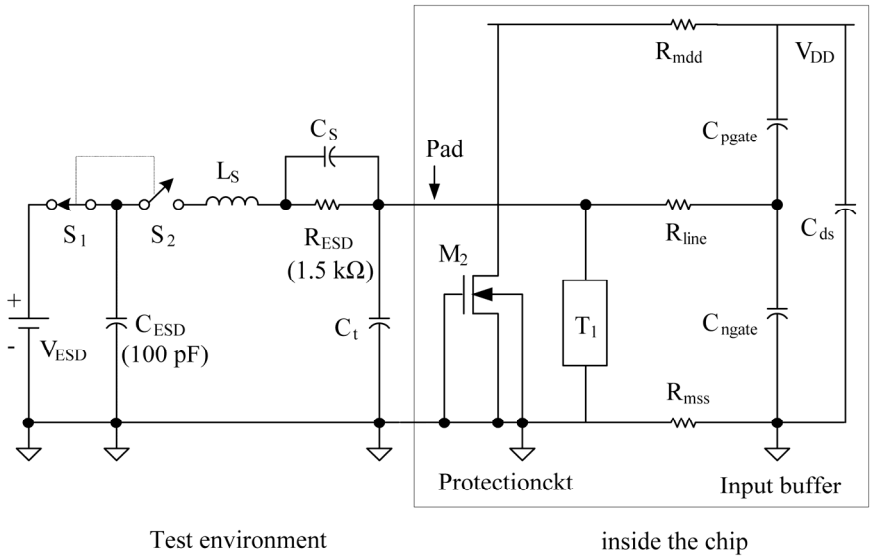

Figure 11. Equivalent circuit of an input-pin HBM test situation.

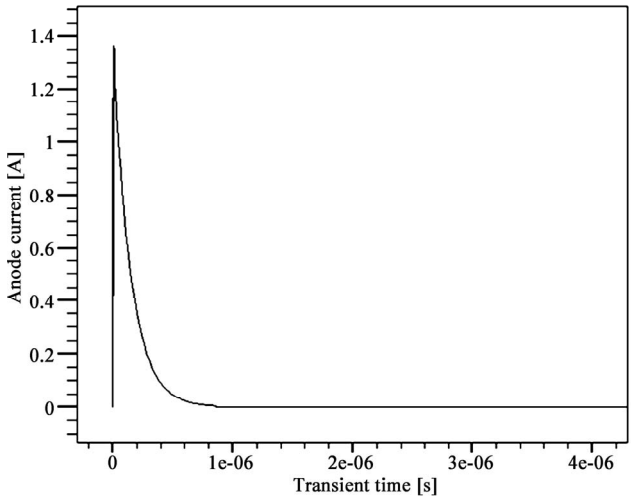

Figure 12. Variation of the anode current of T_1 in a PS mode when using the protection circuit (1).

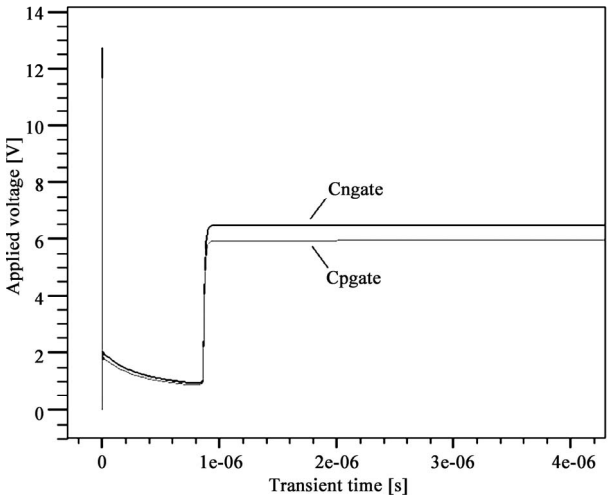

Figure 13. Variations of the voltages developed on C_{ngate} and C_{pgate} in a PS mode when using the protection circuit (1).

With the expectation above in mind, let's examine the results shown in **Figures 12** and **13**. From the results shown in **Figures 12** and **13**, we can see that the parasitic bipolar transistor in T_1 is triggered when the pad voltage in the early stage of discharge increases to about 12.8 V at 0.77 ns after S_2 in **Figure 11** is closed. The trigger voltage is lager than the expected DC value probably due to the time needed for charge redistribution. Main discharge through the pnpn thyristor proceeds as the pad voltage, which is equal to the anode-cathode voltage of T_1, drops to the holding voltage of about 2 V. The pad voltage decreases down to 1 V as the discharge current decreases with time. We can also see that the pad voltage increases again and reaches to 6.5 V at about 0.9 μs, when the anode current is reduced below the holding current for the pnpn thyristor action, and decreases very slowly thereafter. We confirmed from additional simulations that it takes 510 ms for the pad voltage to decrease down to 3 V. We also confirmed that main components of the anode current at 0.9 μs are the leakage current through the n-well/p-sub junction and the weak-inversion MOS current. The developed peak voltage in this later stage of discharge is smaller than the breakdown voltage (8.8 V) of the lvtr_thyristor device shown in **Figure 4**. This seems to be caused by the long duration (0.9 μs) of the main discharge by virtue of the excellent conducting pnpn thyristor. We confirmed that, with the sufficient discharge through the pnpn thyristor, the remaining discharge current level in this stage of discharge is only about 40 nA, which is too low for T_1 to conduct in a breakdown mode. We also confirmed from an additional simulation that, if we decrease the n^+/p^+ anode contact space down to 0.7 μm, the pnpn thyristor turns off earlier at 0.815 μs and the developed peak voltage increases up to 9 V with the remaining discharge current level of about 0.1 mA, which is certainly high enough for the device to conduct in a breakdown mode.

Figure 13 shows that, in overall, a lower voltage by about 1 V is developed on C_{pgate} since the V_{DD} node does not lie in the main discharge path.

Figure 14 shows variations of the voltages developed on C_{ngate} and C_{pgate} in a PS mode in case of using the protection circuit (2) in **Figure 8**. We confirmed that the variation of the anode current of T_1 is similar to that in **Figure 12**.

As we can see from **Figure 14**, the variation of the pad voltage, which is again almost same with the voltage developed on C_{ngate}, is similar to that in case of using the protection circuits (1). The parasitic bipolar transistor in T_1 is triggered when the pad voltage in the early stage of discharge increases to about 12.8 V at 0.77 ns after S_2 is closed. Main discharge through the pnpn thyristor proceeds as the pad voltage drops to the holding voltage of about 2 V.

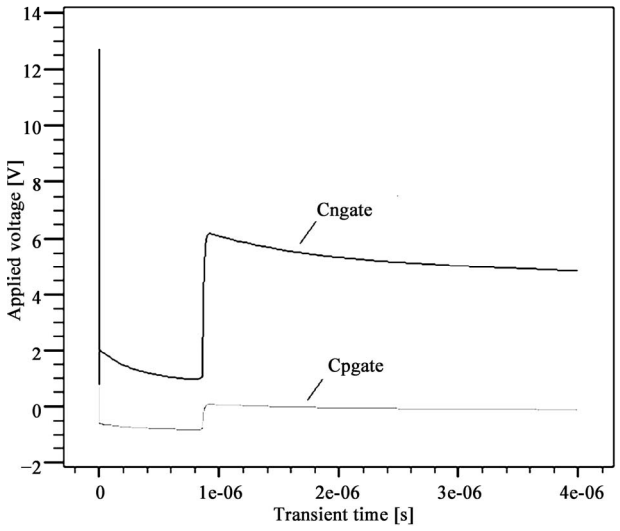

Figure 14. Variations of the voltages developed on C_{ngate} and C_{pgate} in a PS mode when using the protection circuit (2).

The pad voltage increases again and reaches to 6.2 V at about 0.9 μs, and decreases very slowly thereafter. We confirmed that the pad voltage (6.2 V) in this case is slightly lower than that in case of using the protection circuit (1) due to a difference in the current components. We confirmed that, when the pad voltage increases to 6.2 V, a pnp (p^+-cathode/n-well/p^+-sub) bipolar transistor in T_2 is triggered and the pad voltage is limited by the pnp bipolar holding voltage. Since the holding voltage is somewhat large, thermal heating may cause a problem. However, we confirmed that the bipolar current level at this moment is too low to cause thermal heating. The components of the anode current in T_1 in this later stage of discharge also include the leakage current through the n-well/p-sub junction and the weak-inversion MOS current, however the bipolar current through T_2 is a major discharge current for some duration. Due to this current component, the pad voltage in this later stage of discharge decreases faster, compared to the case using the protection circuit (1). We confirmed that it takes 23 ms for the pad voltage to decrease down to 3 V.

In **Figure 14**, we can see that the voltage developed across C_{pgate} remains low all the time. This is because the p^+-cathode/n^+-anode diode is conducting if the V_{DD}-pad voltage becomes larger than the forward diode drop. In the later stage, there is almost no conduction through T_2, and the voltage stays close to zero.

4.1. Voltages across the Gate Oxides in the Early Stage of Discharge

For the two PS modes analyzed above, the trigger time for T_1 is 0.77 ns. Due to this trigger time, the voltage

(12.8 V) larger than the DC snapback voltage is developed across T_1 right after S_2 is closed, resulting the high voltage developed on C_{ngate} in the early stage of discharge in **Figures 13** and **14**.

Depending on test modes, larger peak voltages across the gate oxides in the input buffer appear at C_{ngate} or C_{pgate}. If we define the test modes, which produce larger peak voltages in the mixed-mode transient simulations performed for 5 test modes, as weak modes, the results can be summarized as shown in **Table 2**.

In **Table 2**, 13.3 V on C_{pgate} in the PD mode in case of using the protection scheme (1) corresponds to a sum of the voltages applied on the pnpn structure in T_1 and the forward diode in M_2, which can be easily expected from **Figures 7** and **9**. The voltage applied on the pnpn structure peaks up to 12 V in this case. 13.5 V on C_{pgate} in the ND mode in case of using the protection scheme (1) corresponds to a sum of the voltages applied on the npn structure in M_2 and the forward diode in T_1. The voltage applied on the npn structure peaks up to 10.8 V. 12.3 V on C_{pgate} in the ND mode in case of using the protection scheme (2) corresponds to the voltage applied on the pnpn structure in T_2, which can be easily expected from **Figures 8** and **10**.

The peak voltages in **Table 2** can be regarded as excessive; however, durations of the peak voltages applied are very short. We confirmed that, for example, the durations for which the voltages exceed 10 V are at most 0.2 ns. Therefore it may be inferred that the gate oxides in the input buffer won't be damaged in the early stage of discharge [11].

Notice that the peak voltages can be suppressed by reducing the bipolar trigger voltage of the NMOS transistor in the NMOS protection device or the thyristor protection devices. To make the bipolar trigger voltage of the NMOS transistor even lower than the off-state DC breakdown voltage, the gate-coupled NMOS (gcNMOS) structure [12] can be adopted.

It is possible to obtain a similar result by simply inserting a series resistor between the gate (G_2) and V_{SS} nodes of M_2 in **Figure 7** since the gate-drain overlap capacitance (C_{gd}) already exists in the NMOS structure [4]. For the lvtr_thyristor_down device, the same technique can be applied since it includes the same NMOS structure in it [4]. For the lvtr_thyristor_up device, the same technique can be also applied. A series resistor inserted between the gate (G_2) and the input node in **Figure 8** will do the role.

We performed addition simulations to confirm that the early peaking can be suppressed by adding the series resistor to the gate node. The results are summarized in **Table 3**. For the 250 μm M_2, a 10 kΩ resistor was inserted between the gate and V_{SS} nodes. For the 20 μm T_1, a 125 kΩ resistor was inserted between the gate and V_{SS} nodes. For the 20 μm T_2, a 125 kΩ resistor was inserted between the gate and the input pad nodes. It is certain that the early peaking can be suppressed if needed.

4.2. Voltages across the Gate Oxides in the Later Stage of Discharge

Depending on test modes, larger peak voltages across the gate oxides also appears at C_{ngate} or C_{pgate} in the later stage of discharge. If we define the test modes, which produce larger peak voltages, as weak modes, the results can be summarized as shown in **Table 4**. We confirmed that use of the gate-coupling techniques does not affect the peak voltages in the later stage of discharge at all.

Table 2. Peak voltages developed across the gate oxides in the early stage of discharge.

Protection scheme	Weak mode	Peak voltage [V]		Time [ns]
		C_{ngate}	C_{pgate}	
(1)	PS	12.8		0.77
	PD		13.3	0.66
	ND		13.5	0.82
(2)	PS	12.8		0.77
	ND		12.3	0.80

Table 3. Peak voltages developed across the gate oxides in the early stage of discharge when adopting the gate-coupling technique.

Protection scheme	Weak mode	Peak voltage [V]		Time [ns]
		C_{ngate}	C_{pgate}	
(1)	PS	8.7		0.65
	PD		9.7	0.57
	ND		10.4	0.79
(2)	PS	8.7		0.65
	ND		8.8	0.69

Table 4. Peak voltage developed across the gate oxides in the later stage of discharge.

Protection scheme	Weak mode	Peak voltage [V]		Time [μs]
		C_{ngate}	C_{pgate}	
(1)	PD	7.6		0.92
	ND		10.7	0.50
(2)	PS	6.2		0.92
	ND		8.8	0.89
	PTP	7.4	7.9	0.89

From **Table 4**, we can see that, in case of using the protection scheme (1), the ND mode is the weakest one. 10.7V developed on C_{pgate} corresponds to a sum of the breakdown voltage of M_2 (9.6 V) and the forward diode drop in T_1 (1.1 V) right after the main discharge through M_2 and T_1 is finished, which can be easily expected from **Figures 9** and **7**. Differently from the results of the thyristor devices in **Figures 13** and **14**, the peak voltage developed across M_2 in this case is about same with the DC breakdown voltage (9.3 V). This is because the bipolar transistor in M_2 is not as excellent conducting as the pnpn thyristor, and the main discharge through the bipolar transistor ends earlier (at 0.5 μs) compared to that through the pnpn thyristor as shown in **Table 4**.

In case of using the protection scheme (2), the ND mode is also the weakest one. 8.8 V developed on C_{pgate} corresponds to the voltage developed across T_2, which is somewhat smaller than the DC breakdown voltage (9.1 V) of T_2. In a PTP mode, 7.4 V and 7.9 V are developed on C_{ngate} and C_{pgate}, respectively, which correspond to the voltages developed across T_1 and T_4 in **Figure 10**.

We note that high voltages in the later stage of discharge can damage gate oxides in input buffers since they last for long time. When judging from the peak voltages developed across the gate oxides in the later stage of discharge in **Table 4**, the weakest modes in case of using the protection scheme (1) is an ND mode, and the PMOS gate oxide is more vulnerable to HBM ESD damages if the gate-oxide thicknesses of the NMOS and the PMOS are same. In case of using the protection scheme (2), the weakest mode is also an ND mode and the PMOS gate oxide is also more vulnerable.

When judging from the peak voltages developed, the advantage of the protection scheme (2) over the protection scheme (1) is expected to stand out more as the gate oxide thickness shrinks with advanced process technology used.

4.3. Location of Peak Temperature and Weak Modes

In case of using the protection scheme (1), the utmost peak temperature in a PS mode appears at T_1, and **Figure 15** shows the variation of peak temperature inside T_1. Peak temperature increases up to 473 K at about 0.9 ns just before the pnpn thryristor trigger, but decreases down to 330 K as soon as the pnpn thryristor is triggered since the holding voltage decreases. It peaks again up to 421 K at about 45 ns with increasing discharge current, and decreases slowly with the discharge current decreasing. By examining 2-dimensional temperature distributions, we confirmed that peak temperature at 0.9 ns appears at the n^+ well junction, where the electric field intensity is highest, and that at 45 ns appears at the n^+ cathode junction, where the current density is highest.

If we define the test modes, which produce larger temperature increase inside any protection device, as weak modes, the results can be summarized as shown in **Table 5**.

In case of using the protection scheme (1) incorporateing the 250 μm NMOS device and 20 μm lvtr_thyristor_down device, the weakest mode is the ND mode, and peak temperature appears in M_2, which conducts as an npn bipolar transistor. Peak temperature inside M_2 appears at the gate-side n^+ drain junction. This is the reason for assigning a large spacing between the gate and the drain contact in **Figure 1** to avoid drain contact melting. The second weakest mode is the PS mode, and the 1st peak temperature appears in T_1, which happens just before the pnpn thyristor is triggered. At this point, peak temperature inside T_1 appears at the n^+ well junction

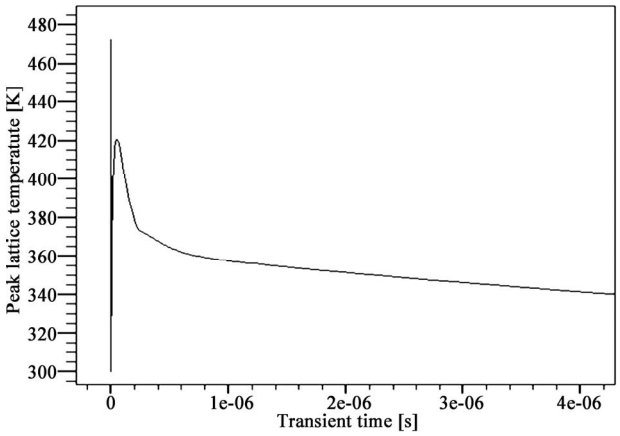

Figure 15. Peak temperature variation inside T_1 in a PS mode when using the protection scheme (1).

Table 5. Peak temperature locations and times.

Protection scheme	Weak mode	Peak temp.[°K]	Peak temperature	
			Location	Time [ns]
(1)	PS	473	n^+ well junction in T_1	0.9
		421	n^+ cathode junction in T_1	45
	ND	495	gate-side drain junction in M_2	33
(2)	PS	471	n^+ well junction in T_1	0.8
		421	n^+ cathode junction in T_1	52
	ND	471	n^+ well junction in T_2	0.9
		473	n^+ cathode junction in T_2	44

at the right-hand corner of the n well. However, a problem with contact melting will not occur in this junction since there is no contact on it. The 2nd peak temperature in T_1 appears at the n^+ cathode junction when it conducts as a pnpn thyristor. Junction engineering such as increasing the junction area or adopting ESD ion implantation may be required to restrain temperature increase. However, it will not add parasitics to the input pad since the junction is not connected to it.

In case of using the protection scheme (2) incorporating the 20 μm lvtr_thyristor devices, the weakest mode is the ND mode, and the 1st peak temperature appears in T_2, which happens just before the pnpn thyristor is triggered. Peak temperature inside T_2 appears at the n^+ well junction at the left-hand corner of the p base. However, a problem with contact melting will not occur in this junction since there is no contact on it. The 2nd peak temperature in T_2 appears at the n^+ cathode junction when it conducts as a pnpn thyristor. Junction engineering such as increasing the junction area or adopting ESD ion implantation may be required to restrain temperature increase. This will not add parasitics to the input pad as long as the p-base region is not widened since the n^+ cathode is located inside the p base. As shown in **Table 5**, lattice heating characteristics in a PS mode are very similar to those in case of using the protection scheme (1).

We confirmed from additional simulations incorporating the gate-coupling technique that all the temperature peaking prior to 1ns in **Table 5** are suppressed below 380 K by virtue of the reduced bipolar trigger voltages. This can be easily expected from the results shown in **Table 3**.

From the result shown in **Table 5**, we can see that the 20 μm lvtr_thyristor devices are superior to the 250 μm NMOS device in ESD robustness in terms of thermal heating. Therefore we can save a lot of area consumed by a pad structure by eliminating the large clamp NMOS device.

5. Discussions

5.1. Considerations in Designing the Lvtr_Thyristor_Down Device

By performing additional simulations, we figured out that a serious problem could occur if the p-type substrate contacts are not located close to the lvtr_thyristor_down device as shown in **Figure 3**. When the p^+-sub/n^+-anode forward diodes in T_1 and T_3 in **Figure 10** turn on in the early stage of discharge in the NS and PTP modes, respectively, the parasitic npn (n^+-cath-ode/p-sub/n^+-anode) bipolar transistor inside this small-sized device can be triggered to increase temperature around the n^+ cathode junction a lot, where electric field intensity is high. Therefore it is very important to locate the p^+-sub contacts close as shown in **Figure 3**.

5.2. Considerations in Designing the Lvtr_Thyristor_Up Device

By performing additional simulations, we also figured out that a similar problem could occur if the n^+ anode2 contact at the right-hand side of the p base is not located in the lvtr_thyristor_up device as shown in **Figure 5**. When the p^+-cathode/n^+-anode forward diode in T_2 in **Figure 10** gets on in the early stage of discharge in PD and PTP modes, a parasitic npn (n^+-cathode/p-base/n^+-anode) bipolar transistor inside this small-sized device can be triggered to increase temperature around the n^+ cathode junction a lot. This can be completely solved by providing an additional p^+-cathode/n^+-anode2 forward diode path with the n^+ anode2 contact as shown in **Figure 5**.

We also figured out that there is an important consideration to take care in connecting the gate node (G_2) in T_2 in **Figure 8**. Even though G_2 can be connected to the V_{SS} node without increasing an off-state leakage in normal operations, this may cause a problem by making the pnpn thyristor in T_1 never triggered in the PTP mode shown in **Figure 10**. This is because the voltage developed between the pad (connected to the n^+/p^+ cathodes of T_2) and the V_{SS} node is restrained below 9 V, which is much smaller than the pnpn trigger voltage of 12.8 V, as a result of capacitive coupling between G_2 (connected to the V_{SS} node) and the n^+/p^+ cathodes of T_2. As a result, the discharge current flows mainly through the upper discharge path (Path 1) consisting of T_2 and T_4 in **Figure 10**. At the same time, the pnp (p^+-cathode/n-well/p^+-sub) bipolar transistor in T_2 is triggered to provide another discharge path by way of the forward biased pn (p^+-cathode/n^+-anode) diode in T_3. This causes a thermal heating problem by increasing lattice temperature near the p^+ sub junction at the right-hand corner of T_2 a lot. This pnp (p^+-cathode/n-well/p^+-sub) bipolar transistor is easily triggered since the p^+-cathode/n-well diode is already forward biased due to the conduction through Path 1 in **Figure 10**. This problem is completely solved by making the pnpn thyristor in T_1 easy to be triggered by connecting G_2 to the input pad as shown in **Figure 8**.

5.3. Providing Discharge Paths for VDD-VSS HBM Discharge

We have to check that a chip adopting the thyristor-only protection scheme can provide safe discharge paths when V_{DD}-V_{SS} HBM tests are performed. We note that large

clamp devices such as the NMOS device shown in **Figure 1** should be located between V_{DD} and VSS buses in V_{DD} and V_{SS} pad structures and also anywhere a space is available to provide discharge paths for V_{DD}-V_{SS} ESD events and also to reduce a V_{DD} bounce during normal operation by increasing the capacitance between the two buses. We note that the bipolar trigger voltage of the clamp NMOS device without the gate-coupling technique was confirmed as less than 11 V relating the result shown in **Table 3**.

Using a single lvtr_thyristor protection device formed by assuming the lvtr_thyristor_down device in **Figure 3** (T_1) and the lvtr_thyristor_up device in **Figure 5** (T_2) located side by side on a same substrate, we confirmed by a mixed-mode simulation that the V_{DD}-V_{SS} peak voltage of the protection scheme (2) in a V_{DD}-V_{SS} HBM test is 17.6 V. The V_{DD}-V_{SS} voltage decreases down to 4 V (2 V each across T_1 and T_2) with both of the pnpn thyristors in T_1 and T_2 being triggered. Therefore, in a V_{DD}-V_{SS} HBM ESD test, it is certain that the clamp NMOS devices will provide discharge paths before the pnpn path through T_1 and T_2 in any of input pad structures is triggered.

Also when a surge voltage appears between V_{DD} and V_{SS} buses, the clamp NMOS device will constrain the rail voltage below 11 V to suppress the possibility of latch-up through T_1 and T_2. Also the latchup cannot persist since the conduction through T_1 and T_2 in series can be maintained only if the V_{DD}-V_{SS} voltage is higher than 4 V, which is higher than the normal supply voltage in recent technologies.

6. Summary

We proposed an input protection scheme composed of thyristor devices only to minimize the size of an input pad structure. For this purpose, we suggested the low-voltage triggering thyristor protection device structures assuming usage of standard CMOS processes, and attempted an in-depth comparison study with a conventional thyristor protection scheme incorporating a clamp NMOS device based on DC and mixed-mode transient analyses utilizing a 2-dimensional device simulator.

We analyzed in detail the problems which can occur in real HBM tests to provide useful findings regarding the proposed protection scheme as follows.

1) We figured out weak modes in terms of peak voltages developed across gate oxides in input buffers.

2) We figured out weak modes in terms of temperature increase inside the protection devices, and also figured out locations of peak temperature inside the protection devices.

3) We suggested design guidelines for each protection device to minimize temperature increase inside it and to minimize voltages developed across gate oxides in input buffers.

4) We showed how we can incorporate the gate coupling technique into the suggested protection devices.

5) We showed that the suggested thyristor-only protection scheme can be made free from CMOS latch-up.

7. References

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