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A Review of PVT Compensation Circuits for Advanced CMOS Technologies

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Abstract

The recent high-performance interfaces like DDR2, DDR3, USB and Serial ATA require their output drivers to provide a minimum variation of rise and fall times over Process, Voltage, and Temperature (PVT) and output load variations. As the interface speed grows up, the output drivers have been important component for high quality signal integrity, because the output voltage levels and slew rate are mainly determined by the output drivers. The output driver impedance compliance with the transmission line is a key factor in noise minimization due to the signal reflections. In this paper, the different implementations of PVT compensation circuits are analyzed for cmos45 nm and cmos65 nm technology processes. One of the considered PVT compensation circuits uses the analog compensation approach. This circuit was designed in cmos45 nm technology. Other two PVT compensation circuits use the digital compensation method. These circuits were designed in cmos65 nm technology. Their electrical characteristics are matched with the requirements for I/O drivers with respect to DDR2 and DDR3 standards. DDR2 I/O design was done by the Freescale wireless design team for mobile phones and later was re-used for other high speed interface designs. In conclusion, the advantages and disadvantages of considered PVT control circuits are analyzed.

Keywords: PVT Compensation, PVT Control Circuit, Process Variation, DDR Interface, I/O Driver

1. Introduction

In any manufacturing step during the fabrication process of ICs, there are target specifications and there are manufacturing tolerances around each specification. For example, the gate oxide thickness specification translates to slower devices (higher threshold voltage) for thicker oxides and faster devices for thinner oxides (lower threshold voltage). If such devices were used as a driver element, large variations in driver strengths and slew rates from the pre-driver should be expected. This is turn affects the timing of the outgoing signals.

Providing the higher data processing rate and interface speed are becoming more important to the evolution of multimedia environment. For example, the speed of modern storage interfaces (ATA/ATAPI-6 standard) has rapidly increased up to 100 MB/s [1]. The recent high-performance interfaces like DDR2, DDR3, USB and Serial ATA require their output drivers to provide a minimum variation of rise and fall times over process, voltage, and temperature (PVT) and output load variations. As the interface speed grows up, the output drivers have been important component for high quality signal integrity, because the output voltage levels and slew rate are mainly determined by the output drivers. Any decrease in the skews variation depending on the PVT variations can usually be translated into better timing budgets and signal integrity, resulting in the increase of system I/O speed. To achieve good signal integrity, slew rate also must be kept constant over PVT variations. Large slew rate induces significant switching noise (Ldi/dt noise) and small slew rate decrease the signal timing margin. One method to improve system speed is to provide circuit compensation. The compensation allows the designer to speed up the slower I/O driver and receiver speeds and increase the driver strength for the slow part. At the same time, the fast part is slowed down to match the slow part in speed and drive strength. Various compensation architectures have been previously reported for PVT variation [2-5] and most of them use external resistors to generate a bias current. Generally, the PVT control circuits can be classified on two types with (1) analog and (2) digital compensation methods, as it shown in **Figure 1**. In this paper, the different imple-

mentations of PVT compensation circuits are analyzed for cmos45 nm and cmos65 nm technology processes. These new PVT circuits are used for compensation of output resistance variation of high speed DDR I/O drivers implemented in sub-100 nm bulk and SOI technologies. In deep submicron technologies, the PVT control is extremely important due to the higher process variations and process instability. One of the considered PVT compensation circuits uses the analog compensation approach.

This circuit was designed in the cmos45nm SOI technology. The second PVT compensation circuit uses the digital compensation method. This circuit was designed in the cmos65nm bulk technology and its electrical characteristics are matched with the requirements for I/O driver with respect to DDR3 standard. In conclusion, the advantages and disadvantages of considered PVT control circuits are analyzed.

2. Scope of the Problem

One practical method of communication between chips is the transmission lines on a printed circuit boards (PCB). These transmission lines are fast and very economical, which explains their popularity. Generally, these transmission lines are thick metal wires (~1 mil) with a polymer dielectric surrounding it. The driver, the transmission line and termination matching are key factors to clean signaling. Transmission lines that are not well terminated suffer from reflecting. These reflections interfere with signaling as a new data will be affected by the remnants of the previous data that have not settled down. It is very well known that the good impedance matching of I/O driver and transmission line reduces the signal reflection in a transmission line. In this paper, the presented PVT compensation circuits are used for impedance matching of I/O driver and transmission line under the process, voltage and temperature variations.

3. Analog Compensation: General Background

There are different implementations of analog PVT compensation circuits. Some of them are presented in **Figure 2**, where in option (a) transistor stacks reflects the stack up in a pre-driver and option (b) reflects a normal output buffer structure, which directly compensates the output impedance under PVT variations. These schemes are based on equalizing the voltage drop across a resistor and transistor. The compensating device (NMOS or PMOS) is compared to a known external resistor (R3 or R6) and the voltage is fed back to an operational amplifier (OA1 or OA2). The operational amplifier compares this voltage to a known reference voltage. Independing on the chip processing (fast or slow), the correct voltage is generated to make the device drains match the reference voltage. Using this compensation voltage, the I/O buffers can be biased. The strengths of drivers and pre-drivers can be adjusted by rationing the gate widths with respect to the compensated N and P devices. Before the compensating voltage can be used, it has to be distributed on the chip to each buffer. Since the distributed interconnection can couple noise from other digital signal lines and be lengthy, it should be closely shielded. An effective shield is the addition of power interconnects in parallel with the compensation voltage interconnect. For example, the analog voltage delivery scheme using Vss wires to shield and charge share the injected noise. The digital signals should not run in parallel to the analog signals.

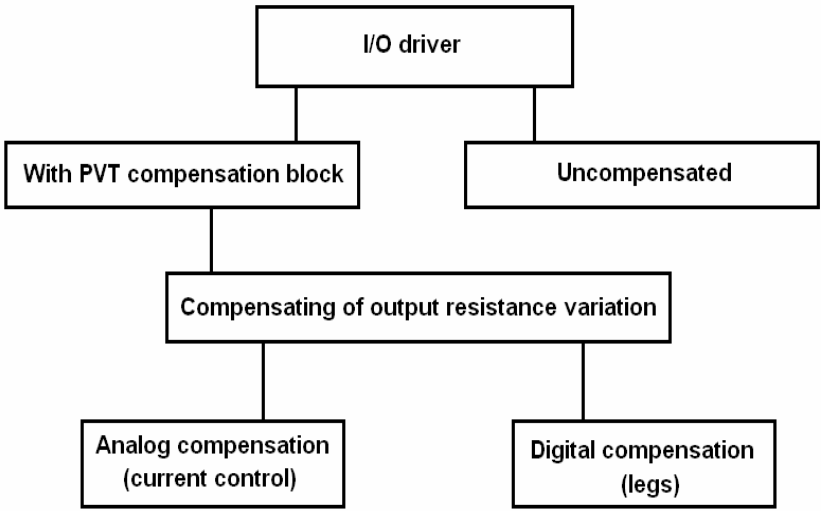

Figure 1. Compensation schemes used for control of output resistance compensation of I/O drivers.

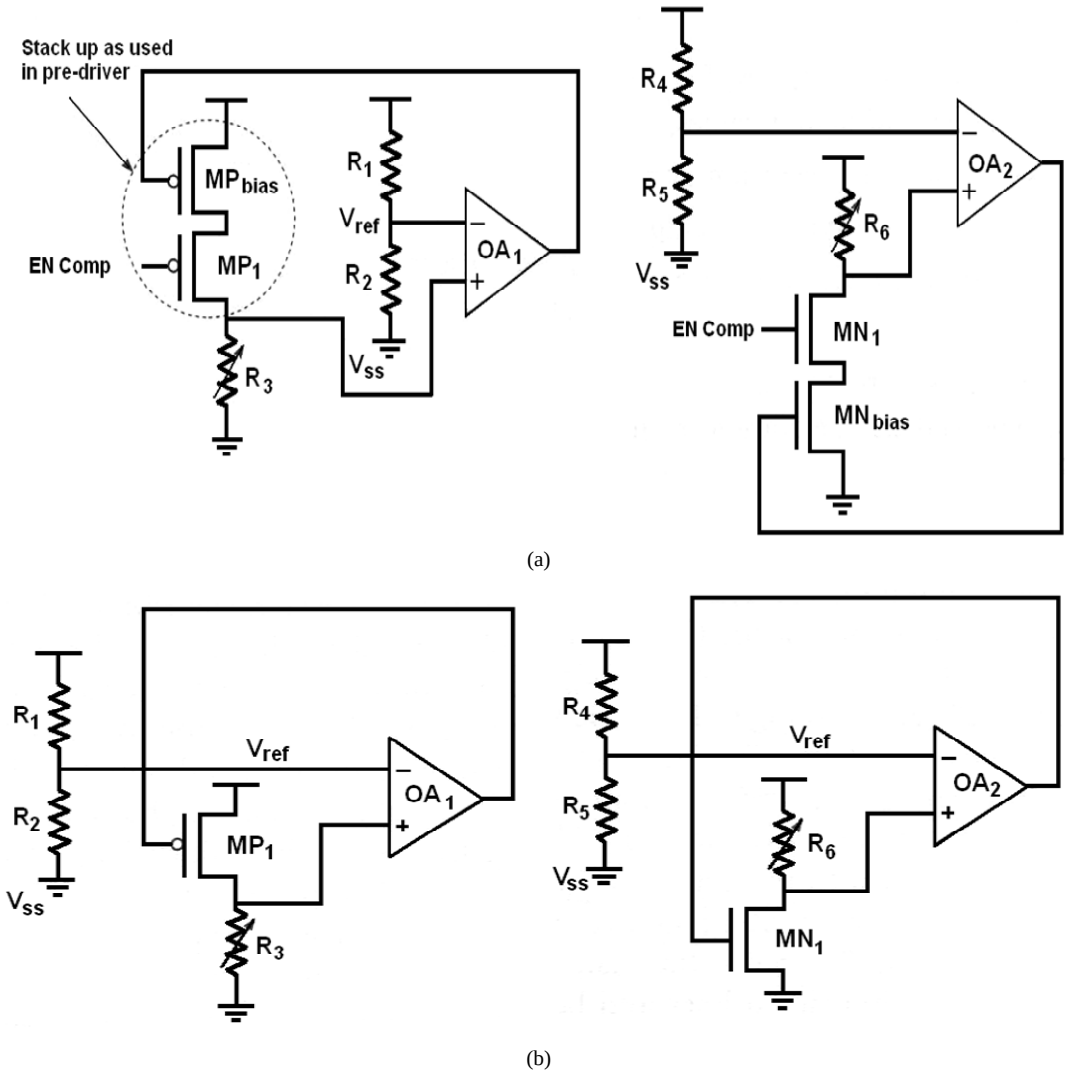

Figure 2. (a) Analog bias generation scheme that can be used to compensate I/O buffers: transistor stack reflects the stack up in a pre-driver (adopted from [6]); (b) Analog bias generation scheme that can be used to compensate I/O buffers: this option is convenient since it reflects a normal output buffer structure (adopted from [6]).

4. Digital Compensation: General Background

The analog techniques are sensitive to noise, as all other analog schemes. This is true in the generation of the compensation voltage and its distribution. An option is to use digital compensation techniques. On of such methods is given in **Figure 3**. Here a circuit similar to the analog case may be used to generate the compensation factor (a series of bits). The calibration transistor is broken into sections. Each leg is then controlled by a control bit. All the "on" legs together represent the driver strength. The control bits are derived from a counter that is fed by a comparator. The comparator senses the voltage division between the resistor and transistor legs and compares it to a reference voltage. A key difference between analog and digital compensation is that in the digital scheme when a leg is turned on it is fully on (Vcc at the gate of an NMOS device), unlike the analog case where all the legs are partially on.

The digital comparator can change states as the feedback loop time permits. The distribution of digital compensated signals is easier because they are all at normal CMOS voltage levels and not at an intermediate analog level, and thus they are less noise sensitive.

One of the implementation of digitally-impedance-controlled output buffer circuit was developed by T. Takahashi *et al*. [5]. This circuit is suitable for chips with a high I/O count due to its stable impedance against various kinds of noise. Impedance of the pull-up NMOS and pull-down NMOS are set to transmission line impedance for obtaining an accurate midpoint level and for avoiding

reflection. The schematic of digitally-impedance-controlled output buffer circuit is shown in **Figure 4**. In this circuit, the input buffer judges 0.6 V as a "High", when the output of its output buffer is "Low" and "Low" when the output is "High". This is accomplished by the adjustable voltage divider which is controlled by the core input signal (Din).

5. Digital Compensation: Implementation in CMOS065 nm Bulk Technology

In this section, two practical implementations of digital PVT compensation technique are analyzed for DDR2 and DDR3 I/O circuits.

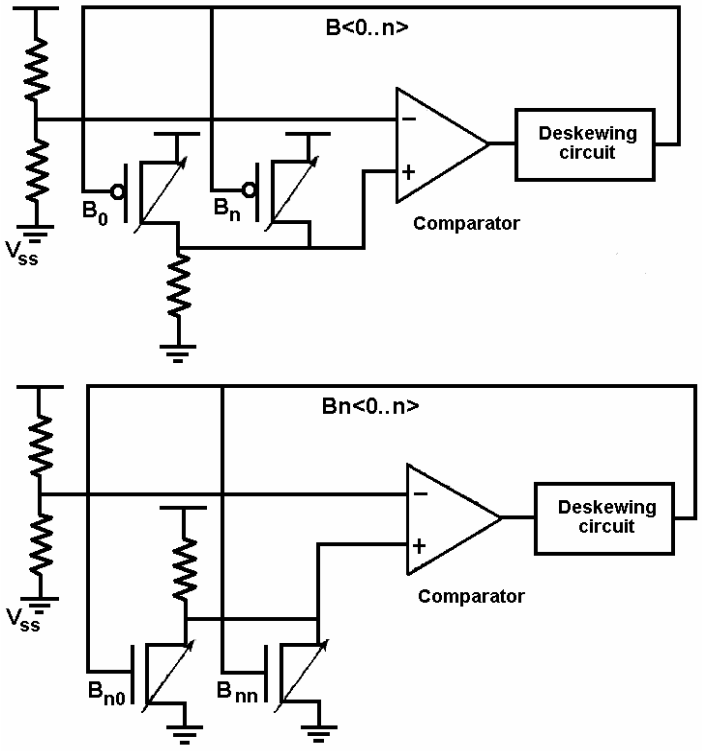

Figure 3. Concept of digital bias generation scheme. It may be similar to analog scheme except that the transistors are not one device but a number of parallel bits capable of being switched on and off independently (adopted from [6]).

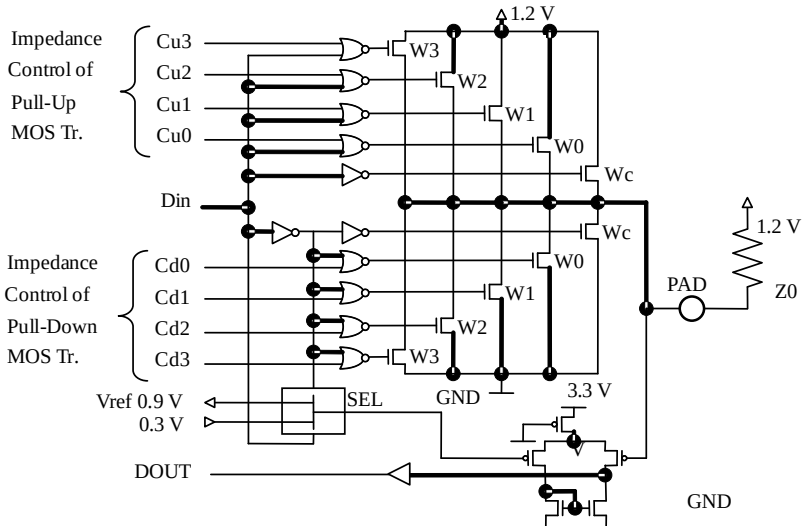

Figure 4. Digitally-impedance-controlled bidirectional I/O circuit [7].

In DDR2 I/O cell, the PVT control circuit consists on PVT sensor block, which is used to track the PVT conditions, and output driver block, which is split on several Legs that are used for the adjustment of output driver impedance according to the detected PVT condition [8]. The schematic of PVT control block is presented in **Figure 5**. The PVT sensor block includes ring oscillator, digital frequency decoder and level shifter. The ring oscillator uses the same OVDD power supply as the DDR drivers in the pad ring. The changing of junction temperature, operating voltage and process variation can be sensed as a changing of oscillation frequency. This oscillation frequency is correlated to the time constant of RC network within of ring oscillator. In the RC network, "R" is determined by the transistor impedance which is a scaled down replica of the output driver. And C represents the metal routing capacitance that has a very low temperature coefficient and has a weak process variation dependency. The ring oscillator output is divided by 256 times prior to the frequency decoder, as shown in **Figure 5**.

Figure 6 shows how the ring oscillator frequency depends on the PVT conditions. "Wcs" corresponds to the lowest frequency, "typ" case corresponds to the medium frequency and "bcs" corresponds to the max frequency. The frequency of ring oscillator is compared to the external reference clock signal (32 KHz CKIL clock). The PVT decoder analysis the difference and generates the 6 bits control signals (s0-s5) to switch ON or OFF the legs in output driver (see **Figure 7**).

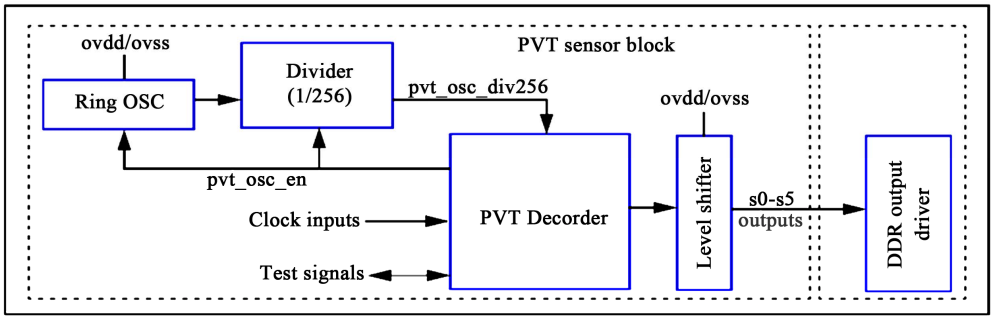

Figure 5. A PVT control circuit used in DDR2 I/O bank [this figure is courtesy of Kiyoshi Kase and Dzung T. Tran from Freescale Semiconductor].

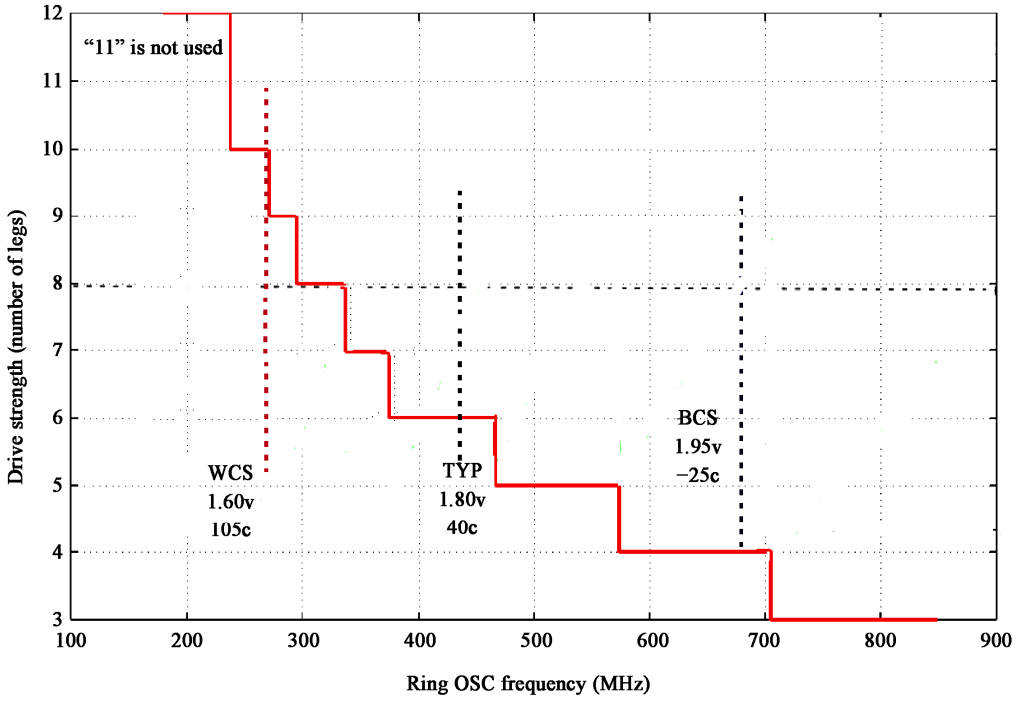

Figure 6. Ring oscillator frequency with respect to the number of output legs that should be connected to keep constant the impedance of output driver [this figure is courtesy of Kiyoshi Kase and Dzung T. Tran from Freescale Semiconductor].

Another digital PVT calibration approach was developed for CMOS065 DDR3 I/O cells set. It uses the external resistor for accurate adjustment of output driver impedance. The schematic of calibration circuit is presented in **Figure 8**. The calibration circuit consists on PMOS and NMOS output drivers that are connected to external resistor, comparator, reference voltage generator, and logical state machine for the generation of calibration signals.

The output NMOS and PMOS drivers have a major transistor, which has a slightly bigger resistance in "bcs" than the external reference resistor, and a number of legs. These are the additional transistors placed in parallel to the major transistor. These legs are used to reduce the total impedance of output driver and match it to the external resistor. In the calibration circuit, the combination of PMOS, NMOS transistors in output drivers and the external reference resistor forms the voltage divider. To monitor the voltage drop on the Xres pin, the comparator is used. It compares the voltage drop on the pin Xres and the reference voltage (OVDD/2) which is generated within of calibration circuit. During the calibration process, the logical state machine activates one by one the additional transistors (Legs) in output PMOS driver using the voh<4:0> signals. As a result, the effective resistance of output PMOS driver is reduced and the voltage drop on the Xres pin is increased. When the voltage drop on the Xres pin is increased to OVDD/2 (the switching

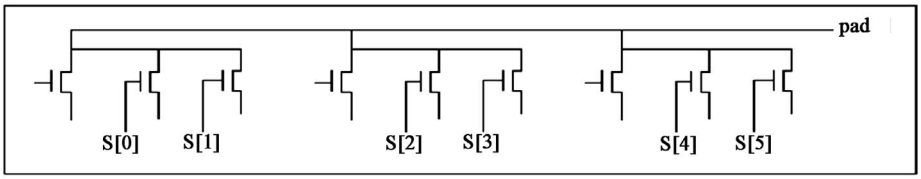

Figure 7. Example of output NMOS driver with additional legs for PVT adjustment [this figure is courtesy of Kiyoshi Kase and Dzung T. Tran from Freescale Semiconductor].

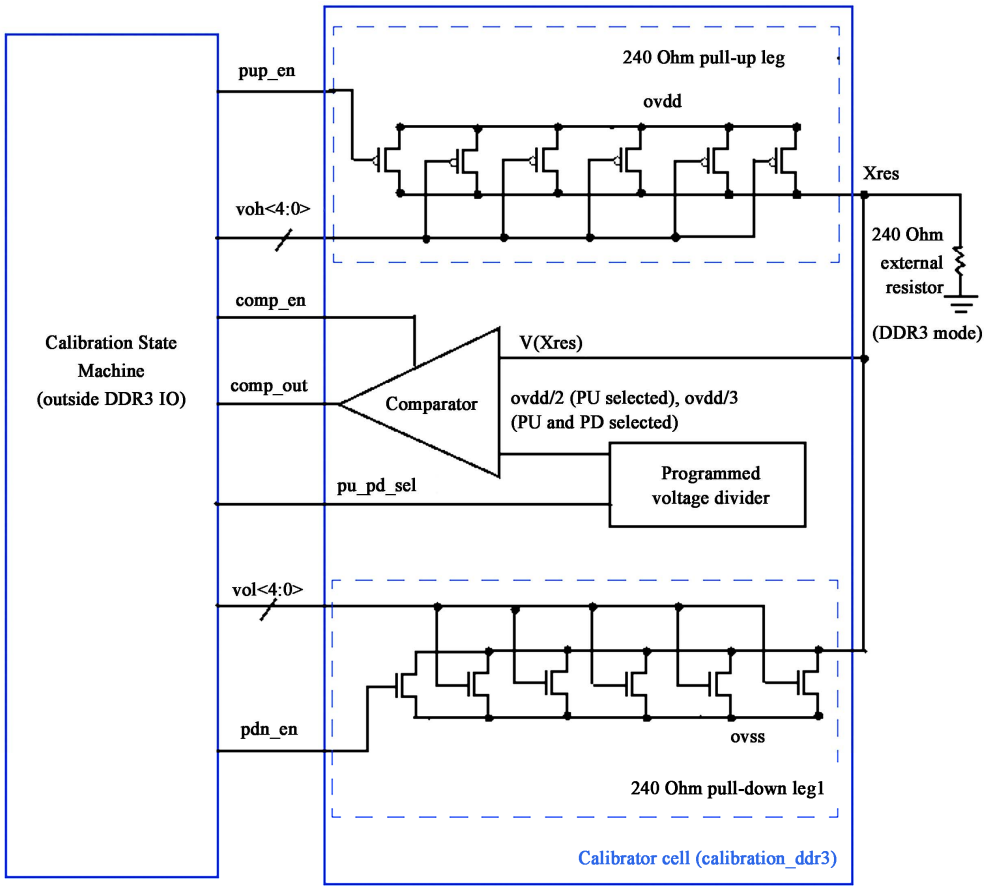

Figure 8. PVT calibration circuit developed for DDR3 I/O banks.

voltage for comparator), the output signal from comparator is changed from 0 to 1. It means that the calibration process of PMOS output driver is completed and the output driver impedance is equaled to the external reference resistor. The calibration codes are stored in the internal register. The next step is the calibration of NMOS output driver. To do this, the previously calibrated PMOS output driver is kept in ON mode and NMOS driver is also switched ON by the vol<4:0> signals. It is necessary because the reference resistor is connected between Xref and VSS. The calibration procedure of NMOS output driver is similar to the calibration process of PMOS output driver, except that the Xref voltage should be compared to OVDD/3 instead of OVDD/2 as it was for PMOS driver. This is because for the NMOS output driver calibration the voltage divider based on PMOS transistor and NMOS transistor with Rext resistor connected in parallel is used.

6. Analog Compensation: Implementation in CMOS045nm SOI Technology

The idea of analog compensation method is based on the control of output driver transconductance. In this method, the output driver of I/O buffer has stacked NMOS and PMOS transistors. One of the stacked transistors is managed by P-pre-driver and N-pre-driver, respectively, as it shown in **Figure 9**, and these transistors are operating in a switch ON/OFF mode. On the gate terminals of second transistors in the stacked transistor pairs are applied the Vbias_n and Vbias_p voltages that keep constant transconductance of stacked transistors under different PVT conditions.

Generally, the analog PVT compensation circuit consists on two major blocks: 1) PVT control block (**Figure 9**) and 2) Reference current block (**Figure 10**). The reference current block has the "OVDD/2" voltage divider, external resistor, operational amplifier and a couple current mirrors. The external resistor is used to specify the reference currents Iref_p and Iref_n that are not dependent on process corners and temperature, and are directly proportional to the OVDD/2 voltage.

The PVT control block consists on two stacked NMOS and PMOS devises and two operational amplifiers. The principle of PVT block operation is the same as the functionality of previously mentioned analog bias generation circuit shown in **Figure 2(a)**. The advantage of analog PVT compensation circuit developed for CMOS045 nm SOI technology is that it requires just one external reference resistor. Most of other implementations of analog PVT compensation circuits given in literature require two external resistors, for example circuit presented in **Figure 2(a)** or circuit developed by Seok-Woo Choi *et al*. [9].

7. Conclusions

In this paper several different implementations of PVT compensation circuits are analyzed for cmos45 nm and cmos65 nm technology processes. One of the considered PVT compensation circuits uses the analog compensation approach. This circuit was designed in cmos045 nm SOI technology. Other two PVT compensation circuits use the digital compensation method. Theses circuits were designed in cmos065 nm technology and their electrical characteristics were matched with the requirements for I/O driver with respect to DDR2 and DDR3 standards.

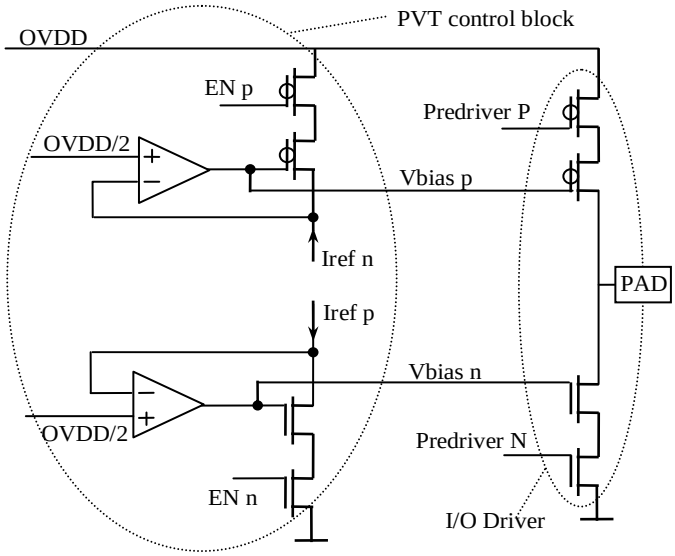

Figure 9. Implementation of PVT control block.

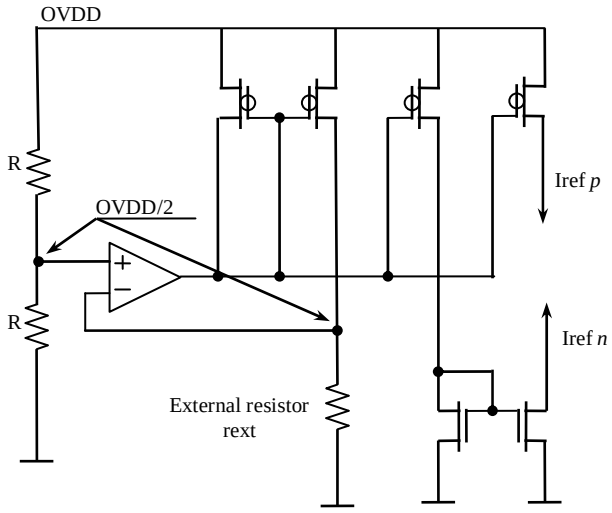

Figure 10. Reference current block.

The advantage of analog-based PVT compensation circuit is that its layout area is typically smaller than the layout area consumed by the digital-based PVT compensation circuit. However, the digital-based PVT compensation circuit is recommended for chips with high I/O count due to its stable impedance against various kinds of noise. Finally, in case of uncompensated I/O drivers, the effect of PVT variations can be reduced by the placement of poly-silicon resistor in series to the transistor of output driver. Typically, poly-silicon resistor has low dependency on PVT variations and it is designed to have significantly higher resistance than the output driver transistor.

8. Acknowledgements

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9. References

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