Circuits and Systems, **2011, 2, 145-150**
doi:10.4236/cs.2011.23022 Published Online July 2011 (http://www.SciRP.org/journal/cs)

New Analysis to Measure the Capacitance and Conductance of MOS Structure toward Small Size of VLSI Circuits

Wagah Farman Mohammad
Communications & Electronics Department, *Faculty of Engineering*, *Philadelphia University*, *Amman*, *Jordan*
E-mail: *wagahfaljubori@yahoo.com*
Received February 16, 2011; *revised April* 15, 2011; *accepted April* 22, 2011

Abstract

In this research thin film layers have been prepared at alternate layers of resistive and dielectric deposited on appropriate substrates to form four - terminal R-Y-NR network. If the gate of the MOS structures deposited as a strip of resistor film like NiCr, the MOS structure can be analyzed as R-Y-NR network. A method of analysis has been proposed to measure the shunt capacitance and the shunt conductance of certain MOS samples. Mat lab program has been used to compute shunt capacitance and shunt conductance at different frequencies. The results computed by this method have been compared with the results obtained by LCR meter method and showed perfect coincident with each other.

Keywords: Thin Film R-Y-NR Network, MOS R-Y-NR Network, MOS-VLSI Circuits, MOS Capacitance

1. Introduction

In recent years, there have been rapidly growing interest and activity in thin film integrated circuits as an approach to microelectronics. Electronic circuits have been fabricated on the basis of replacing conventional lumped elements with their thin film equivalents. Essentially the VLSI memory devices are Electronic structures. The Metal-Oxide-Silicon (MOS) structures are an important type of the VLSI memory devises. MOS capacitance is one of the key test structures for VLSI technology characterization. It permits the determination of the electrical characteristics of a given technology such as oxide thickness, substrate doping, the switching speed and the driving capability of VLSI circuits [1].

The MOS capacitor is a Metal-Oxide-Semiconductor structure. **Figure 1** show the MOS capacitor which consists of few layers: semiconductor substrate with a thin oxide layer and a top metal contact also referred to as the gate. A second metal layer forms an ohmic contact to the back of the semiconductor, also referred to as the bulk. The electrical characteristics of MOS structures determine the switching speed of VLSI circuits. The electrical characteristics of MOS structures may be estimated using few simple formulas, such [2]:

The gate capacitance: $C_G = C_{ox}WL$

The channel resistance: $R_C = R_s\ (L/W)$. Where R_s is the sheet resistance, C_{ox} is the oxide capacitance, L is the channel length and W is the channel width. Unfortunately MOS is not simple and computing the channel resistance and gate capacitance is more complicated.

As MOS feature size is getting smaller and smaller, the thickness of layers becomes more and more significant. The correct extraction of parasitic capacitance and resistance in deep submicron VLSI design is getting a major research area. The MOS different modes of operation, namely accumulation, flat band, depletion and inversion [3] are introduced here. The MOS structure has a

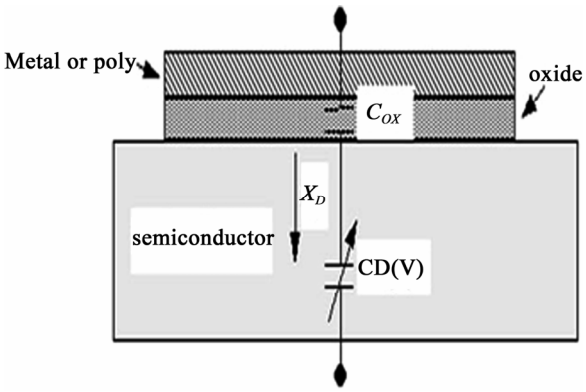

Figure1. Schematic cross section of the MOS.

p-type substrate. The structure will be referred as an n-type MOS capacitor since the inversion layer as discussed below contains electrons.

To understand the different bias modes of an MOS capacitor three different bias voltages were considered. The first one is below the flat band voltage, V_{FB}, a second between the flat band voltage and the threshold voltage V_T, and finally one larger than the threshold voltage.

These bias regimes are called the accumulation, depletion and inversion mode of operation. These three modes as well as the charge distributions associated with each of them are shown in **Figure 2**.

Accumulation occurs typically for negative voltages where the negative charge on the gate attracts holes from the substrate to the oxide-semiconductor interface. Depletion occurs for positive voltages. The positive charge on the gate pushes the mobile holes into the substrate. Therefore, the semiconductor is depleted of mobile carriers at the interface and a negative charge, due to the ionized acceptor ions, is left in the space charge region. The voltage separating the accumulation and depletion regime is referred to as the flat band voltage, V_{FB}. Inversion occurs at voltages beyond the threshold voltage. In inversion, there exists a negatively charged inversion layer at the oxide-semiconductor interface in addition to the depletion-layer. This inversion layer is due to minority carriers, which are attracted to the interface by the positive gate voltage. **Figure 3** represents a typical C(V) behavior for a MOS capacitance test structure, measured at high frequency (1 MHz). The operation ranges are also indicated on this figure: strong inversion, depletion, and accumulation.

The majority of the up-dated work however has been concerned with the investigation of sandwiched three layer rectangular and exponential shaped structures. In these structures, alternate layers of resistive and dielectric films are deposited on appropriate substrates to form four terminal R-Y-NR networks [4], which is a special type of MOS structure. In this research a new method to measure the capacitance and conductance of MOS structures was derived and discussed. The method of analysis that was used to obtain the steady state ac response and the response to a unit step is rather straightforward. It is shown that the partial differential equation relating voltage, position, and time is of second order homogeneous ordinary linear differential equation [5]. If the MOS gate deposited as a strip of resistor film like NiCr, MOS structure can be analyzed as R-Y-NR network [6].

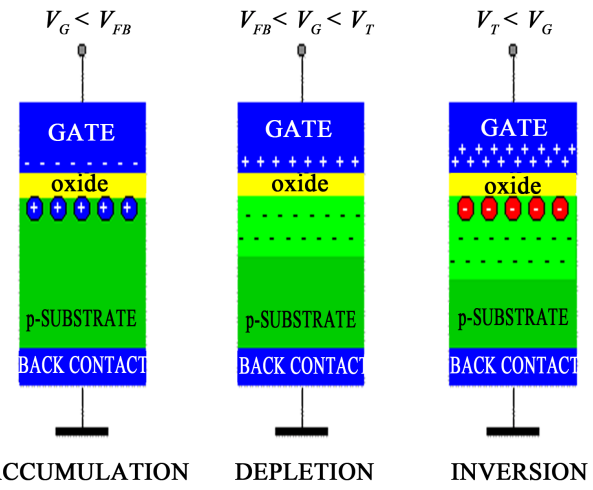

Figure 2. The three bias regimes of MOS structures.

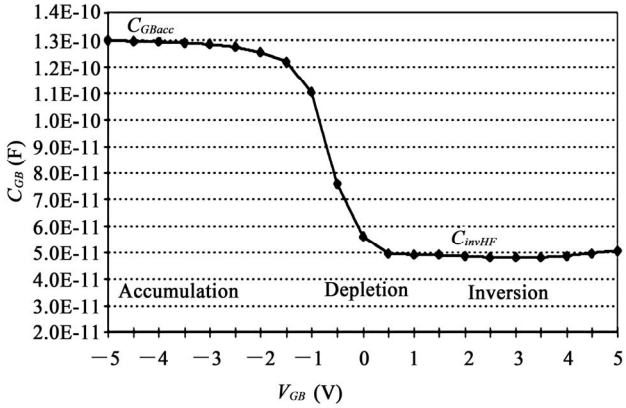

Figure3. *C*(V) behavior for a MOS capacitance test structure measured at high frequency (1 MHz).

2. Open Circuit Voltage Transfer Function

The matrix parameter functions (MPFs) of a solvable DP R-Y-NR network are defined with the following symbols [5]:

$$r = \begin{vmatrix} M_0' & F_0' \\ M_L' & F_L' \end{vmatrix} \tag{1}$$

$$g = (1+N) R_o \begin{vmatrix} M_0' & F_0' \\ M_L' & F_L' \end{vmatrix} \tag{2}$$

$$b = (1+N) R_L \begin{vmatrix} M_0' & F_0' \\ M_0 & F_0 \end{vmatrix} \tag{3}$$

$$a = (1+N) R_o \begin{vmatrix} M_L' & F_L' \\ M_L & F_L \end{vmatrix} \tag{4}$$

$$h = (1+N) R_L \begin{vmatrix} M_0' & F_0 \\ M_L & F_L \end{vmatrix} \tag{5}$$

$$y = (1+N)^2 R_o R_L \begin{vmatrix} M_L & F_L \\ M_0 & F_0 \end{vmatrix} \tag{6}$$

Employing the technique of sub network generation

[7,8], the open circuit voltage transfer function T_{vo} of the exponential distributed parameter two-port three Layer sub networks of **Figure 4** is obtainable in terms of the matrix parameter functions (MPFs). The exponential distributed parameter R-Y-NR structure consists of two resistive layers with per unit length (PUL) series resistance $R = R_o\exp(Kx)$ and $NR = NR_o\exp(Kx)$ for first and second resistive layers respectively. These two resistive layers are separated from each other by an intermediate dielectric layer for which the per unit length (PUL) shunt capacitance is $C = C_o\exp(-Kx)$ and shunt conductance is $G = G_o\exp(-Kx)$ where N is a dimensionless constant representing the ratio of the two resistive layers, R_o is a PUL resistive constant, C_o is a PUL capacitive constant, G_o is a PUL conductive constant and K is a PUL exponential taper constant.

The open circuit voltage transfer function [7] for the Sub network in **Figure 4(a)** is:

$$T_{V_o} = \frac{V_o}{V_i} = \frac{a + N_g}{(1+N)g} \tag{7}$$

And that for the sub network in **Figure 4(b)** is:

$$T_{V_o} = \frac{V_o}{V_i} = \frac{g - a}{(1+N)g} \tag{8}$$

where g and a are (MPFs) for the exponential distributed parameter (DP) R-Y-NR structure. For structure of length L and ac signal, they are identified as [8]:

$$g = \cosh(mL) + \frac{K}{2}\sinh(mL) \tag{9}$$

ω = angular frequency = $2\pi f$

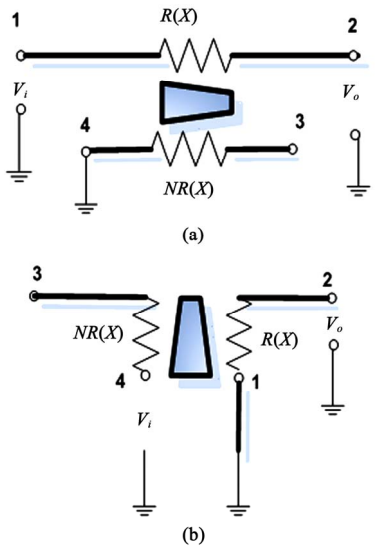

Figure 4. (a) IOFG configuration: 1-input, 2-output, 3-floating and 4-Ground. (b) GOFI configuration: 1-ground, 2-output, 3-floating and 4-input.

For $N = 0$ which means that the second resistive layer is perfect conductive film, Equations (7) and (8) will respectively be abbreviated to:

$$a = m\exp\left(\frac{KL}{2}\right)$$
$$m = \sqrt{(K/2)^2 + (j\omega C_o + G_o)R_o(1+N)} \tag{10}$$
ω = angular frequency = $2\pi f$

For $N = 0$ which means that the second resistive layer is perfect conductive film, Equations (7) and (8) will respectively be abbreviated to:

From **Figure 4(a)**:

$$\frac{V_o}{V_i} = \frac{a}{g} \tag{11}$$

From **Figure 4(b)**:

$$\frac{V_o}{V_i} = \frac{g-a}{g} = 1 - \frac{a}{g} \tag{12}$$

Substituting the matrix parameter functions in the Equations (11) and (12) will respectively give:

From **Figure 4(a)**:

$$\frac{V_o}{V_i} = \frac{m\exp\left(\frac{KL}{2}\right)}{m\cosh(mL) + \frac{K}{2}\sinh(mL)} \tag{13}$$

From **Figure 4(b)**:

$$\frac{V_o}{V_i} = 1 - \frac{m\exp\left(\frac{KL}{2}\right)}{m\cosh(mL) + \frac{K}{2}\sinh(mL)} \tag{14}$$

Considering the uniform distributed thin film R-Y-NR network; that means the constant of exponential taper is zero ($K = 0$), and substituting in the Equations (13) and (14) leads respectively to get:

From **Figure 4(a)**:

$$\frac{V_o}{V_i} = \frac{m}{m\cosh(mL)} = \frac{1}{\cos h(mL)} = \mathrm{Sech}(mL) \tag{15}$$

From **Figure 4(b)**:

$$\frac{V_o}{V_i} = 1 - \mathrm{Sech}(mL) \tag{16}$$

where m is a complex angle per unit length and

$$m = \sqrt{j\omega C_o R_o + R_o G_o} \tag{17}$$

Then the complex angle is $mL = m \times L$ and

$$mL = \sqrt{j\omega C_o R_o L^2 + R_o G_o L^2} \tag{18}$$

Let $\frac{V_o}{V_i} = T_{v1}$ and $\frac{V_o}{V_i} = T_{v2}$ for circuit connection in **Figures 4(a)** and **(b)** respectfully.

Then:

$$T_{v1} = \text{Sech}\left(mL\right) \tag{19}$$

And:

$$T_{v2} = 1 - \text{Sech}\left(mL\right) \tag{20}$$

Subtracting (20) from (19) and manipulating the results lead to:

$$mL = \text{Sech}^{-1}\left(\frac{T_{v1} + 1 - T_{v2}}{2}\right)$$

And hence:

$$\left(mL\right)^2 = \left[\text{Sech}^{-1}\left(\frac{T_{v1} + 1 - T_{v2}}{2}\right)\right]^2 \tag{21}$$

From Equation (18):

$$\left(mL\right)^2 = j\omega C_o R_o L^2 + R_o G_o L^2 \tag{22}$$

Joining Equations (21) and (22) gives:

$$C = C_o L = \frac{\text{Im}\left[\text{Sech}^{-1}\left(\frac{T_{v1} + 1 - T_{v2}}{2}\right)\right]^2}{\omega R_o L} \tag{23}$$

$$G = G_o L = \frac{\text{Re}\left[\text{Sech}^{-1}\left(\frac{T_{v1} + 1 - T_{v2}}{2}\right)\right]^2}{R_o L} \tag{24}$$

3. Experimental Results

For sake of showing accuracy of the proposed method, shunt capacitance and shunt conductance measurements have been carried out on a certain MOS samples. These samples are accomplished by depositing a strip of NiCr resistor thin film as a gate contact and then depositing two dot aluminum points at the two ends of the strip for measurement purposes.

At the beginning, transfer function of the device has been measured for both configurations shown in **Figure 4**. Response of transfer function magnitude and its phase with respect to frequency have been plotted as shown in **Figures 5** and **6** respectively for positive gate biasing. For negative biasing, transfer function magnitude and phase responses have been plotted as shown in **Figures 7** and **8** respectively. Mat lab program has been used to compute shunt capacitance and shunt conductance for strip gate MOS structure at different frequencies. For a zero bias, shunt capacitance and shunt conductance of the MOS structure at different frequencies have been computed. The computed results and the results obtained using LCR meter method [9] have been plotted, as shown in **Figures 9** and **10**. It is clear that the results obtained from the two methods coincided with each other.

4. Conclusions

In this research the high frequency C-V and G-V device measurements were fulfilled using MOS structure as a

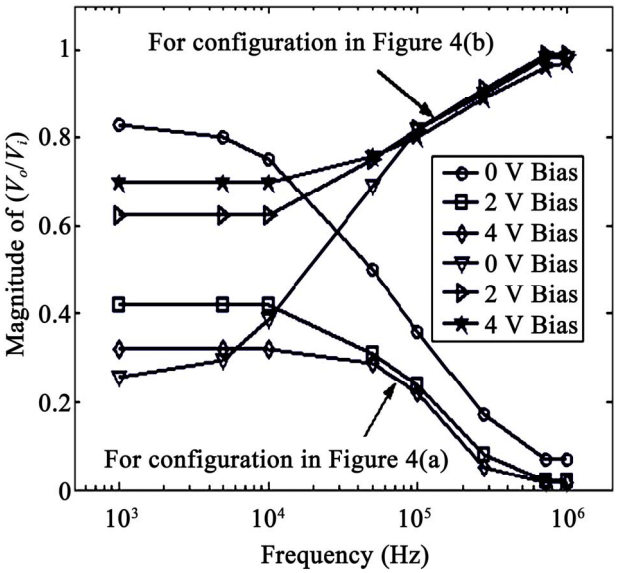

Figure 5. Transfer function magnitude frequency response of a strip gate MOS device for different positive biases.

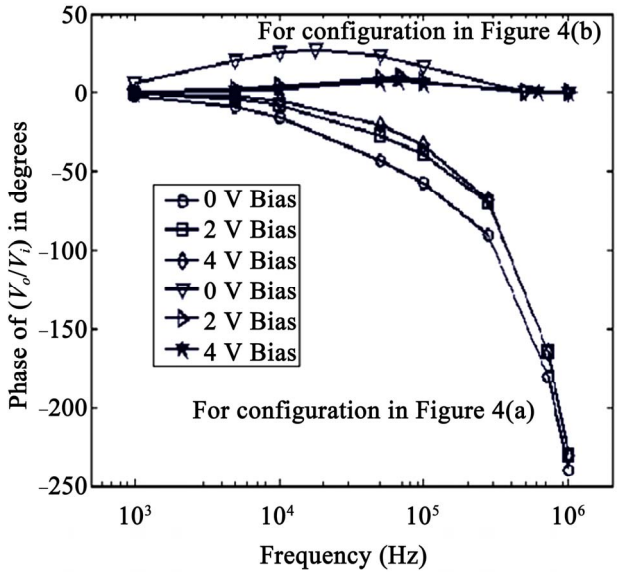

Figure 6. Transfer function phase frequency response of a strip gate MOS device for different positive biases.

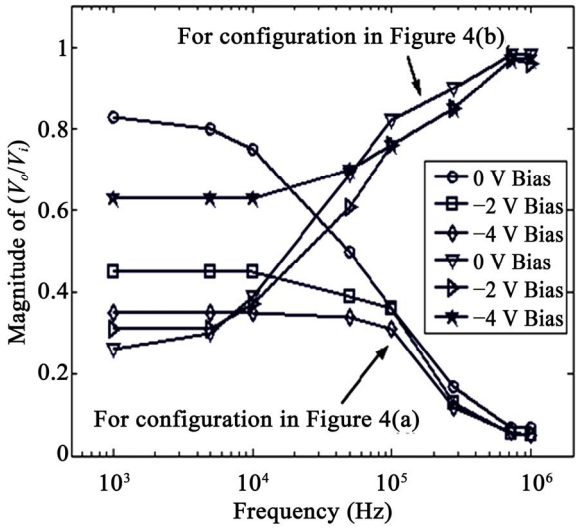

Figure 7. Transfer function magnitude frequency response of a strip gate MOS device for different negative biases.

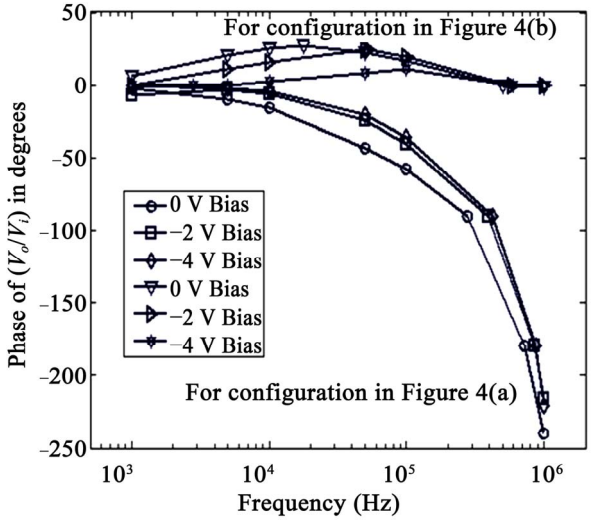

Figure 8. Transfer function phase frequency response of a strip gate MOS device for different negative biases.

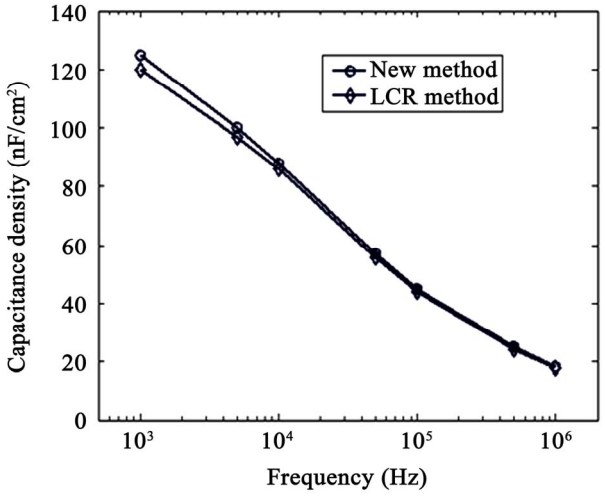

Figure 9. Comparison between capacitance determined by the two methods for zero bias.

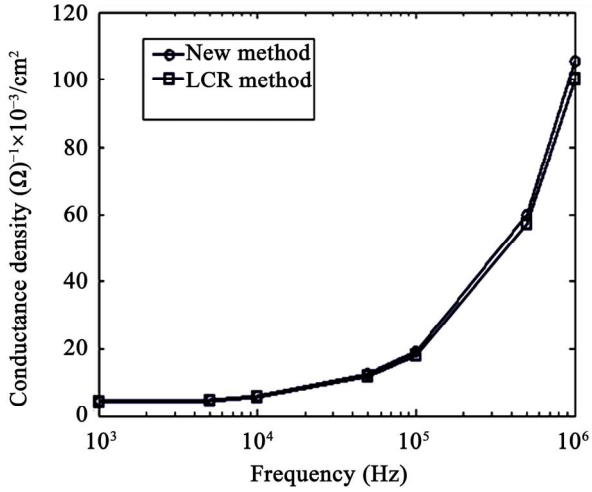

Figure 10. Comparison between leakage conductance dede-termined by the two methods for zero bias.

thin film distributed R-Y-NR structure with four terminal two port network. This conclusion encourage using the proposed method as a tool for C-V and G-V plots at any frequency.

5. References

[1] A. Meinertzhgen, C. Petit, M. Jourdain and F. Mondon, "Anode Hole Injection and Stress Induced Leakage Current Decay in Metal-Oxide-Semiconductor Capacitors," *Solid-State Electronics*, Vol. 44, No. 4, 2000, pp. 623-630. doi:10.1016/S0038-1101(99)00309-3

[2] J. Singh, "Semiconductor Optoelectronics, Physics & Technology," McGraw-Hill, New York, 1995.

[3] W. Monch, "Electronic Properties of Ideal and Interface-Modified Metal-Semiconductor Interface," *Journal of Vacuum Science & Technology B*, Vol. 14, No. 4, 1996, p. 2985. doi:10.1116/1.588947

[4] B. B. Woo and J. M. Bartlemay, "Characteristics and Applications of a Tapered, Thin Film Distributed Parameter Structure," *IEEE International Convention Record*, Vol. 11, No. 2, 1963, pp. 56-75.

[5] K. U. Ahmed, "The Two Port Four Terminal Matrix Parameter Functions of Solvable Distributed Parameter Z--Y-KZ Network," *IEEE Transactions on Circuit Theory*, Vol. 19, No. 5, 1972, pp. 506-508. doi:10.1109/TCT.1972.1083528

[6] P. L. Swart and C. K. Campbell, "Effect of Losses and Parasitic on a Voltage-Controlled Tunable Distributed RC Notch Filter," *IEEE Journal of Solid-State Circuits*, Vol. 8, No. 1, 1973, pp. 35-36.

[7] K. U. Ahmed, "Two Port Sub-networks of Exponential

Distributed Parameter Z-Y-KZ and Y-Z-KY Micro-circuits with Similar Transfer Functions," *Micro Electron Reliable*, Vol. 21, No. 2, 1981, pp. 235-239.

[8] K. U. Ahmed, "A New Band-Reject Filter Configuration of Three-Layer Thin-Film Exponential R-C-KR," *Micro Electron Reliable*, Vol. 21, No. 2, 1981, pp. 241-242.

[9] P. Olivo, T. N. Nguyen and B. Ricco, "High-Field Induced Degradation in Ultra-thin SiO_2 Films," *IEEE Transactions on Electron Devices*, Vol. 35, No. 12, 1988, pp. 2259-2267. doi:10.1109/16.8801

