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High Frequency Oscillator Design Using a Single 45 nm CMOS Current Controlled Current Conveyor (CCCII+) with Minimum Passive Components

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Abstract

In the field of analog VLSI design, current conveyors have reasonably established their identity as an important circuit design element. In the literature published during the past few years, numerous application have been reported which are based on a variety of current conveyors. In this paper, an oscillator circuit has been proposed. This oscillator is designed using a single positive type second generation current controlled current conveyor (CCCII+). A CCCII has parasitic input resistance on it's current input node. This resistance could be exploited to reduce circuit complexities. Thus in this accord, a novel oscillator circuit is proposed which utilizes the parasitic resistance of the CCCII+ along with a few more passive components.

Keywords: Current Mode (CM) Circuit Applications, Current Conveyor (CC), Current Controlled Current Conveyor (CCC) Applications, CCCII Oscillator Circuit; Single CCCII+ Oscillator Circuit, Low Power Oscillator Circuit

1. Introduction

In the recent past, the analog VLSI has emerged as a promising technology for the future demands of low power and high bandwidth requirements. Current mode (CM) design approach is fast gaining in and establishing a trend setting reputation in the design of the modern day VLSI. It proves to be a viable technique that can help applying various design considerations which are ineffective or hard to apply otherwise. Because of it's superiority over the voltage mode approach, [1], the CM design approach appears to be a fit candidate for the next generation of analog VLSI.

Current mode design approach is one where circuits are operated on current stimuli and also the states of the circuits are represented in terms of currents rather than in terms of voltages. Current mode approach has numerous remarkable features, like, superior bandwidth, higher speed and better operational accuracy. It does not require highly sophisticated designs as demanded by the good performance VM amplifiers. Further, this approach can also manage with comparatively low precision design components. The CM design approach has been successfully applied to a variety of circuit applications. For example, several important CM applications are proposed in [2]. These applications are based on various CM devices like CCII, CCIII, CFA, OFC.

Current conveyor (CC) is an important and versatile current mode active building block, which has been considered superior to operational amplifiers [3], and can offer higher design flexibility than conventional operational amplifiers. It can be elegantly applied to a variety of analog circuit design problems. CC versions of various standard applications are found simpler and more elaborate than their voltage mode counterparts. In a CC, the voltage follower action between the input nodes and the current conveyance between input output nodes are the principal actions [1], and are controllable over a wide range [3]. A CC facilitates the use of both positive and negative feedbacks with equal ease, and can be used to simulate negative resistance. Current controlled current conveyor (CCC) is yet another CM active building block, where considerable parasitic resistance appears at the current input node and is controllable by the controlling (biasing) current. Both of these devices also offer the features of current duplication and current negation without any deterioration in the operation of the principal

circuit. A brief review of the well known characteristics of an ideal CCCII+ are given in Equation (1) and **Figure 1** [4,5].

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_X & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1)$$

In a type CCCII+, both I_X and I_Z may flow into or out of the device simultaneously. For the other two possible combinations of these currents, the device is typed as CCCII-. The R_X is input resistance at the node X and depends upon the circuit structure.

In this work, an oscillator is realized using CMOS version of the CCCII+ shown in **Figure 1**. Resistance R_X of the CCCII+ is exploited and is treated like any other passive resistor with the aim of reducing the demand of external passive resistors.

2. Oscillator Circuit Scheme

Several oscillator circuits have been published recently [4,6-10]. These circuits have invariably been proposed on the basis of the multiple use of CC/CCC along with two or more passive components, incorporating both inverting and non inverting outputs, and, in some cases, a few more design building blocks, etc. A number of oscillator topologies are presented in [11]. ICCII is the active device used in all these topologies. However, the minimum passive component count is irredundantly four, along with at least one ICCII.

Here in this work, a novel scheme is proposed as depicted in **Figure 2**. This scheme is quite simple and employs only one single output CCCII+ with a possible minimum passive component count. Here the basic circuit structure is proposed with four passive components, however, the subsequent analysis helps in reducing the external component count to three. The circuit also has the added features like, very low power requirement,

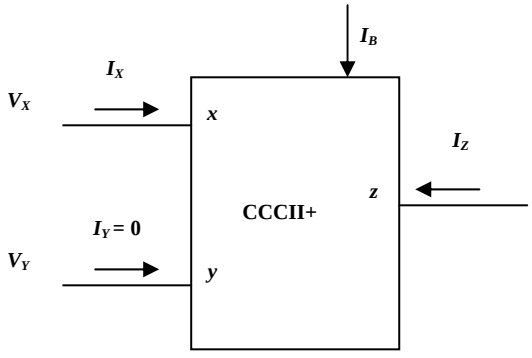

Figure 1. Block Diagram representation of the 2nd generation CCCII+.

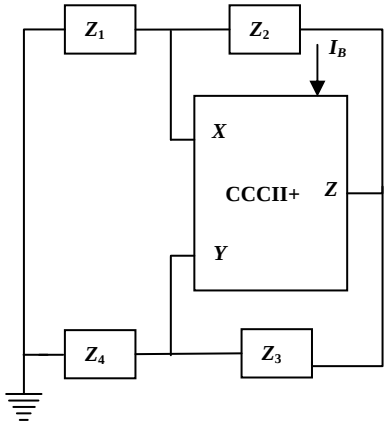

Figure 2. Generalized scheme for the proposed Oscillator. All Z_i's are impedances.

capability of generating high oscillation frequency, low turn-on time [6], and electronically tunable frequency through I_B.

Routine analysis of the scheme of **Figure 2**, gives the following characteristic equation:

$$\begin{aligned} Z_2 Z_4 &= Z_4 R_X + Z_1 Z_2 + 2 Z_1 Z_3 \\ &+ R_X \left(Z_1 + Z_2 + Z_3 \right) \end{aligned} \quad (2)$$

For a real frequency of oscillation, and the gain adjustment, a suitable second order polynomial is required, so that the real and imaginary components yield. This requirement of Equation (2) can be fulfilled for the following specific choice of external components as given in Equation (3). Arrows in Equation (3) indicate the operation of replacing the impedances by the corresponding passive components (for example, impedance Z_1 is replaced by the capacitor C_1).

$$Z_1 \to C_1; Z_2 \to C_2; Z_3 \to R_3; Z_4 \to R_4 \quad (3)$$

The choice of Equation (3) is incorporated in the scheme of **Figure 2** and the following s-domain characteristic polynomial is obtained.

$$\begin{aligned} &s^2 C_1 C_2 R_X \left(R_3 + R_4 \right) + \\ &s\left(C_1 R_X + C_2 R_X + 2 C_2 R_3 - C_1 R_4 \right) + 1 = 0 \end{aligned} \quad (4)$$

Equation (4) gives the necessary gain condition and the frequency of oscillations.

$$C_1 R_X + C_2 R_X + 2 C_2 R_3 = C_1 R_4 \quad (5)$$

$$\omega_O = \frac{1}{\sqrt{C_1 C_2 R_X \left(R_4 + R_3 \right)}} \quad (6)$$

Equations (5) and (6) clearly show the insignificance of R_3. If it is shorted, ($R_3 = 0$), both the Equations (5) and (6) are further simplified.

$$R_4 = 2 R_X \quad (7)$$

$$\omega_O = \frac{1}{\sqrt{2}CR_X} \quad (8)$$

Thus it is possible to realize the oscillator using a single CCCII+, one Resistor and two equal capacitors. The final complete circuit is presented in **Figure 3**.

On the basis of **Figure 3** and the Equations (7) and (8), a few observations are worth noting. Equation (7) depicts ideal condition, and thus Equation (8) remains a valid equation when expressed in terms of R_4. Further, from **Figure 3**, the feedback signal with respect to node *Y* is $V_2 = \frac{R_X - R_4 - sCR_XR_4}{R_4(1+2sCR_X)}V_3$. For large values of R_4 and ω, $\frac{V_2}{V_3} \to -\frac{1}{2}$. It clearly indicates that a larger value of R_4 is necessary to build up the required level of the *Y* node feed back signal and 180° phase shift so that the circuit sustains oscillations. Therefore the oscillation frequency should better be defined using Equation (8) instead of using the suggestion of Equation (7), as it predicts only the ideal condition for oscillations. Simulation results also suggest the independence of the frequency of oscillations of R_4.

Ignoring the body effect, the estimate of resistance R_X of the above circuit, is given by $R_X \approx \frac{1}{g_{m10}+g_{m9}}$. For matched transistors M9 and M10, $R_X \approx \frac{1}{\sqrt{8\beta I_B}}$, β being the device transconductance of M9 [5].

3. Circuit of the CCCII+

For realization of the above oscillator, the class AB CCCII+ circuit adopted is shown in **Figure 4**, and is readily available in literature. It's bipolar version is

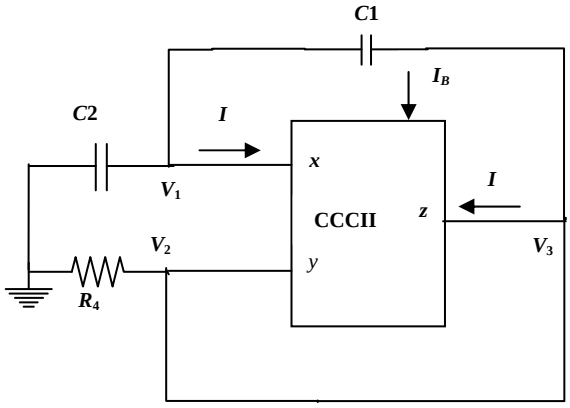

Figure 3. Simplified circuit schematic of the CCCII+ based oscillator.

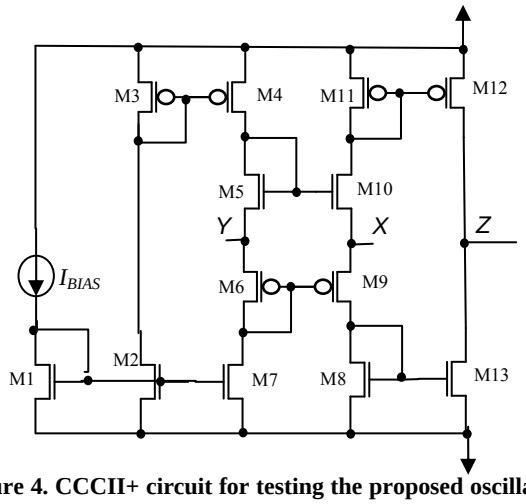

Figure 4. CCCII+ circuit for testing the proposed oscillator. Upward arrow is to V_{DD} and the downward arrow is to V_{SS}.

studied by many authors, [12,13]. It's CMOS version can be found in references [5,10]. In the present work, this circuit is redesigned in 45 nm CMOS and is simulated using the "Predictive Technology Model Beta Version 45 nm MOS Parameters" compatible with HSPICE [14]. The design details of this circuit are presented in **Table 1**.

4. Verification and Results

CCCII+ of **Figure 4** is designed in 45 nm CMOS, and is applied to the realization of the proposed oscillator.

The application is then simulated on HSPICE and the performance of the oscillator (node *Z* voltage signal) is presented in **Figure 5**. For clarity of the necessary details, **Figure 5** is windowed between 600 ns and 800 ns; and is presented in **Figure 6**. However, the simulation is done for the entire 0.1 ms interval.

Fourier analysis, with respect to the principal frequency (38.48 MHz), is performed on the node *Z* signal to ascertain the quality of the oscillations. Result of this analysis is presented in **Figure 7**. Peaks in **Figure 7** correspond to the principal frequency of the oscillator and it's harmonic frequencies. Third harmonic component is significant (–27 dB) compared to the second harmonic component (–30 dB). Estimates of the total harmonic distortion (THD) and the DC component of the node *Z* signal are important quality matrices. Both these parameters are found reasonably very low. The simulation results are summarized in **Table 2.**

It is noteworthy that the sustainable oscillations are established without requiring a trigger signal. Further, the value of resistor R_4 estimated by Equation (6) above, would theoretically establish oscillations. It is observed that higher values of R_4 enhance the voltage buildup

Table 1. Design details of the circuits of Figure 3 & Figure 4.

Design Parameter	Value
R_4	15 kΩ
$C_1 = C_2$	1 pF
Supply Voltage	± 1.0V
I_{BIAS}	3 μA
W/*L*	0.98 μm/0.2 μm (all NMOS)
W/*L*	8.3 μm/0.36 μm (all PMOS)
Parameters	45 nm (β version), HSPICE

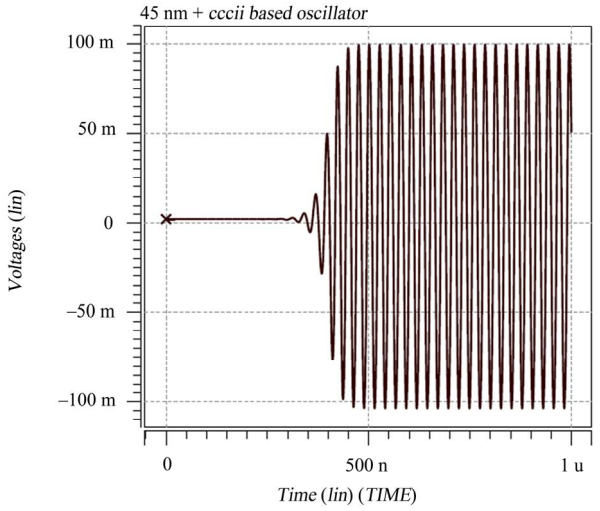

Figure 5. Output of the proposed oscillator (node *Z*). I_B = 3 μA, *C* = 10 pF. Figure shows startup time ≈ 400 ns.

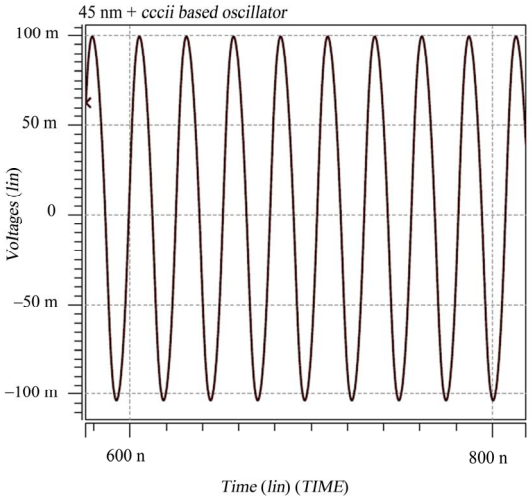

Figure 6. Expanded view of the output signal (node *Z*) in Figure 5.

quicker and hence the oscillations start up earlier. It is also observed that R_4 do not affect the oscillation frequency though Equation (8) can be expressed in terms of R_4. This is merely because of Equation (7).

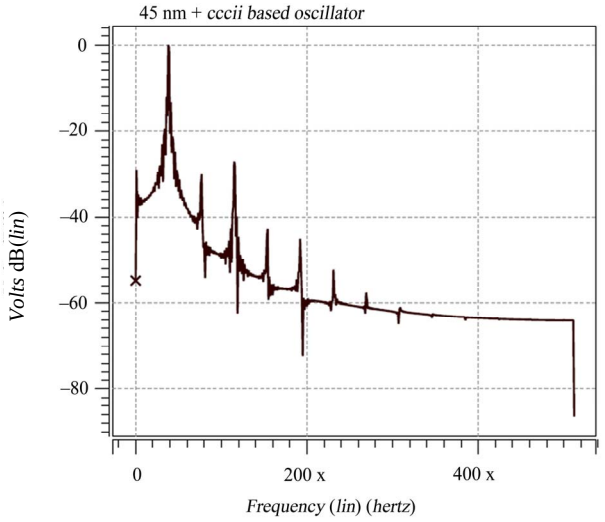

Figure 7. Fourier analysis of the signal at node z of Figure 5. First peak appears at 38.5 MHz. Subsequent peaks occur at harmonic frequencies.

Table 2. Performance results of the proposed oscillator.

Performance Parameters	Detail
Frequency	38.5 MHz
THD	–31.4 dB,(2.7%)
DC Component	–1.8 mV
Peak Average Magnitude	–104 mV to 99.4 mV
Total Power Dissipation(biasing source)	257 μW
Oscillations start-up Time	~400 ns
SNR at output node	–0.75 dB

Authors of reference [4] reported frequency of operation in kHz range for their proposed oscillators with a THD of 0.5% using CC/CCC based upon bipolar technology.

Authors of reference [11] use 1.2 μm CMOS based ICCII using ±2.5 V supply voltages. The total active area for the proposed ICCII was 2096 μm^2. Also the proposed oscillators gradually build up to final peak to peak amplitude of oscillations in about 400 μs. Test results in [11] are presented for 39.78 kHz.

The circuit scheme proposed here in this work is a low voltage, low power scheme, based on CCCII designed in 45 nm CMOS technology, biased at ±1 V and simulation results are summarized in **Table 2**. In addition, the proposed circuit can generate frequencies up to 100 MHz(at I_B= 2.79 μA, C_1= C_2= 0.225 pf), and requires only 19.6 μm^2 active area, which is quite small [11].

Figure 8 shows a logarithmic plot for frequency variation with respect to capacitance. The graph shows a natural trend of as frequency drops with increasing capacitance.

In **Figures 9** a plot for frequency variation with biasing current of the CCCII+ is presented on logarithmic scale. Simulation results show that a variation in the bias current, ΔI_B = 2.9 μA (0.4 μA to 3.3 μA), cause the oscillator frequency to vary as Δf = 25.78 MHz (15.2 MHz to 40.98 MHz). For the sake of analysis, a figure of merit could be defined as the current to frequency transfer coefficient, K_{fi}, [15]. Thus for $C_1 = C_2 = 1$ pf, K_{fiN} = 25.78 MHz /2.9 μA = 8.9 MHz/μA. $K_{f\text{-}I}$ depends on capacitances and the biasing current. It varies directly with the I_B and inversely with the capacitances.

5. Non Idealities of CCCII+ and Their Impact on Circuit Performance

In the above analysis, the CCCII+ is considered ideal. However, a number of non-idealities are present in a practical CCCII+. Considering some of these non-idealities, the device model of the CCCII+ of **Figure 1** can be described as below:

$$I_Z = \pm \alpha I_X \tag{9}$$

$$V_X = I_X R_X + \beta V_Y \tag{10}$$

$$I_Y = I_\delta \tag{11}$$

where α in Equation (9), is the current conveyance coefficient between nodes X and Z; β in Equation (10), is the voltage gain from node Y to node X and is usuall $y < 1$. I_δ in Equation (11) is the input current at node Y. For analytical simplicity in the proposed oscillator scheme, it is assumed that this current is a function of the voltage at node Z. Therefore, $I_\delta = V_Z/R_\delta$, where R_δ is the corresponding resistance at the Y node. Also, as usual, $C_1 = C_2 = C$. Using these assumptions, analysis of circuit in **Figure 3**, gives the following modified characteristic equation:

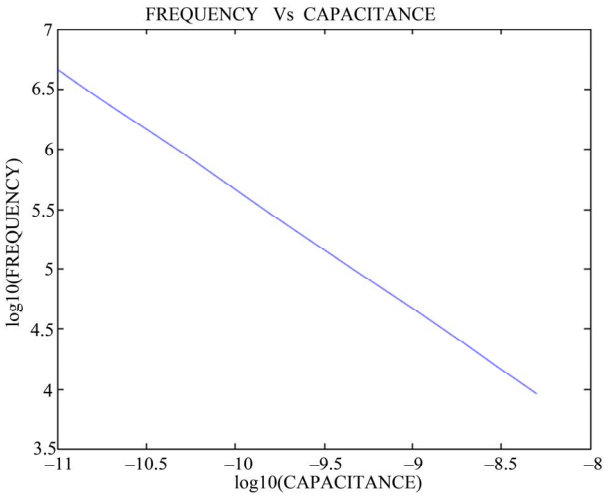

Figure 8. Frequency variation with Capacitor ($C_1 = C_2 = C$).

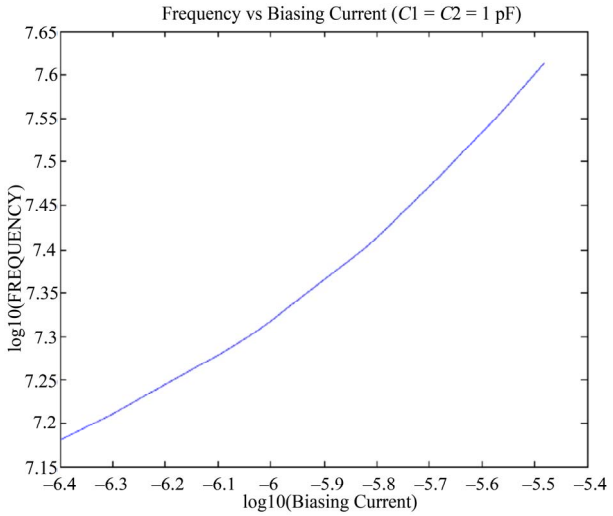

Figure 9. Frequency variation with biasing current. Case 2 : C = 1 pF.

$$s^2 C^2 R_4 R_X + sC\left(2R_X - 2\alpha\beta R_4 + R_4 + \beta R_4 - \alpha R_4 R_X + 2\frac{R_4}{R_X}\right) + \left(1 + \frac{R_4}{R_\delta}\right) = 0 \tag{12}$$

On solving Equation (12), the results are:

$$\frac{1}{R_4} + \frac{1}{R_\delta} = \frac{\alpha(1+2\beta) - (1+\beta)}{2R_X} = \frac{K}{2R_X} \tag{13}$$

$$\omega^2 = \frac{\frac{1}{R_\delta} + \frac{1}{R_4}}{C^2 R_X} = \frac{K}{2C^2 R_X^2} \tag{14}$$

$$\omega = \sqrt{K}\frac{1}{\sqrt{2}CR_X} = \sqrt{K}\omega_O \tag{15}$$

$$\frac{\omega}{\omega_O} = \sqrt{K} < 1 \tag{16}$$

Equation (13) relates R_4, R_X, and R_δ. Equation (15) shows a possible elimination of R_δ. Hence either of R_4 and R_X or both may get modified on account of the voltage and current tracking errors of the CCCII. Here it is assumed that the circuit non-idealities do not cause significant change in the value of R_X. Equation (16) shows that the oscillation frequency ω under non-ideal conditions is lesser than the ideal oscillation frequency ω_o . Further more,

$$K = \alpha(1+2\beta) - (1+\beta) \tag{17}$$

Equation (17) indicates that the variation in the oscillator frequency depends on the current and voltage tracking errors, and shows no effect of the current existing at node *Y* of the CCCII+. Percent decrease in the frequency can be described as:

$$\frac{\omega_O - \omega}{\omega_O} = 1 - \sqrt{K} \tag{18}$$

For an ideal situation, $\alpha \to 1$, $\beta \to 1$, $I_\delta = 0$ and $R_\delta \to \infty$; hence Equation (13) reduces to $\frac{1}{R_4} = \frac{1}{2R_X}$, and Equation (14) reduces to Equation (8), and hence from Equations (16) and (18), $\omega = \omega_O$. But for a 5% tracking error in the values of α, and β, e.g. $\alpha = 0.95$, $\beta = 0.95$, using Equation (18), the deviation in the oscillation frequency is observed to be $\frac{\omega_O - \omega}{\omega_O} = 0.1028$, or 10.3%.

6. Time Domain and Stabilty Considerations

The time domain analysis may be significant in giving better insight in the functioning and performance of the oscillator circuit. Assuming the circuit of **Figure 3** relaxed, it can be described by the following system of equations for $v_1(t)$ and $v_3(t)$ voltages of nodes 1 and 3 respectively

$$(CR_X)^2 R_4 \frac{d^2 v_1}{dt^2} + CR_X (2R_X - R_4) \frac{dv_1}{dt} + R_X v_1 = 0 \tag{19}$$

$$(CR_X)^2 R_4 \frac{d^2 v_3(t)}{dt^2} + CR_X (2R_X - R_4) \frac{dv_3(t)}{dt} - R_X v_3(t) = 0 \tag{20}$$

Equation (19) predicts oscillatory behaviour for the option $R_4 = 2R_x$ as has already been indicated above. Using this option, and defining $\omega'_o = \frac{1}{CR_4}$, general solutions of Equations (19) and (20) are as follows

$$v_1(t) = c_1 e^{j\omega_o' t} + c_2 e^{-j\omega_o' t} \tag{21}$$

$$v_3(t) = c_3 e^{\sqrt{2}\omega_o' t} + c_4 e^{-\sqrt{2}\omega_o' t} \tag{22}$$

In the above Equations (21) and (22), the coefficients C_1, C_2, C_3, and C_4, are arbitrary constants. Equation (21) is oscillatory in nature. In Equation (22), one of the terms rises exponentially to saturation while the other term sharply decays out for large ω'_o and hence oscillations attain their amplitude. $\omega_o = \sqrt{2}\,\omega'_o$

Again one can consider the gain limits of the circuit. For this purpose, feedback signal from node *Z* to node *X* is through C_1 and C_2 ($C_1 = C_2$), while to node *Y* is through R_4. Thus the gain function corresponding to the capacitive feedback arm is:

$$\frac{v_1(s)}{v_3(s)} = \frac{sCR_X + 1}{s2CR_X + 1} = \tfrac{1}{2}\frac{s + \frac{2}{CR_4}}{s + \frac{1}{CR_4}} = \tfrac{1}{2}\frac{s + 2\omega'_o}{s + \omega'_o} \tag{23}$$

$$\left|\frac{v_1(s)}{v_3(s)}\right| = \tfrac{1}{2}\frac{\sqrt{\omega^2 + 4\omega'^2_o}}{\sqrt{\omega^2 + \omega'^2_o}} = \tfrac{1}{2}\frac{\sqrt{\omega_n^2 + 4}}{\sqrt{\omega_n^2 + 1}} \tag{24}$$

Similarly the gain function corresponding to the resistive arm is

$$\frac{v_3(s)}{v_1(s)} = \frac{(sCR_X - 1)R}{sCRR_X + R_X - R} = \frac{s - \frac{2}{CR_4}}{s - \frac{1}{CR_4}} = \frac{s - 2\omega'_o}{s - \omega'_o} \tag{25}$$

$$\left|\frac{v_3(s)}{v_1(s)}\right| = \frac{\sqrt{\omega^2 + 4\omega'^2_o}}{\sqrt{\omega^2 + \omega'^2_o}} = \frac{\sqrt{\omega_n^2 + 4}}{\sqrt{\omega_n^2 + 1}} \tag{26}$$

Equations (24) and (26) are described as a function of normalized frequency, $\omega_n = \omega/\omega'_o$. From Equation (24), the gain limits are: for $\omega_n \to 0$, $\left|\frac{v_1(s)}{v_3(s)}\right| \to 1$ and $\omega_n \to \infty$, $\left|\frac{v_1(s)}{v_3(s)}\right| \to \frac{1}{2}$. Similarly from Equation (26), $\omega_n \to 0$, $\left|\frac{v_3(s)}{v_1(s)}\right| \to 2$ and $\omega_n \to \infty$, $\left|\frac{v_3(s)}{v_1(s)}\right| \to 1$. In both cases, the gain transitions occur between $1 < \omega_n < 2$. However, the phases for Equations (23) and (25), being opposite to one another, start at 0° phase angle, both attain a peak ($\omega_n \approx 1.4$, $\varphi(\omega) \approx \pm 19.47^\circ$ and then gradually die towards zero individually. It is thus concluded that the system is quite stable [16].

7. Conclusions

In this work, a novel oscillator is designed using a single CCCII+, two passive capacitors to control frequency and one passive resistor to sustain the necessary gain. The simulation results of the oscillator verify the circuit capability to generate megahertz oscillations. Quality of oscillations is also reasonable as per the simulation results presented in **Figures 5** and **6**, summarized in **Table 2**. The DC component of the output is observed about –1.8 mV and the total harmonic distortion in the output

node Z signal is about 2.7% (–31.4 dB) at 38.5 MHz frequency (see **Table 2**). The peak to peak amplitude of the output voltage is 203 mV. Also, the simulation shows the average power dissipation low, 257 μW when biased through ±1.0 V and a 3 μA source. The oscillator is also investigated for higher frequencies and found capable of generating 100 MHz at I_B = 2.79 μA, $C_1 = C_2$ = 0.225 pf satisfactorily. It is also supported by the **Figures 8** and **9** that smaller capacitance and larger bias current results higher frequency oscillations.

Further more, it is noticeable that a higher value of R_4 is required to set in the oscillations. The reasons may include

1) Requirement of the feedback loop gain to satisfy the criterion of oscillations.

2) Current, and voltage follow up errors at the relative node pairs (Z, X) and (Y, X) respectively. If R_X assumed unchanged, critical value R_4 requires an upward modification on account of $\alpha \neq 1$, $\beta \neq 1$.

In presence of such non-idealities, however, the model of CCCII described in Equation (1) may be modified to accommodate the tracking errors and the voltage node input current.

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \beta & R_X & 0 \\ 0 & \pm\alpha & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} I_\delta \end{bmatrix} \qquad (27)$$

It is also noticeable that it is the deviations (the absolute values of the coefficients α and β) that affect the results much more than the input current or impedance of the node Y as is clearly indicated by Equation (15). It is further noteworthy that the definition of the parasitic resistance in Equation (1) includes both gate transconductance and body transconductance of M9 and M10. Body transconductnace of the MOSFETs, was ignored in the analysis. Inclusion of the body transconductance of the MOSFETs, however, shows a favorable impact on decreasing R_X, and thus improves the oscillator performance.

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