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Influence of Temperature and Pentacene Thickness on the Electrical Parameters in Top Gate Organic Thin Film Transistor

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Abstract

In this contribution, we report on the effect of pentacene thickness and temperature on the performance of top gate transistors. We first investigated the temperature dependence of the transport properties in the temperature range of 258 K - 353 K. The electrical characteristics showed that the threshold voltage (V_T) and the onset voltage (V_{on}) remain unchanged. However, the subthreshold current (I_{off}), the on-current (I_{on}) and the field effect mobility (μ) are highly affected with a slight deterioration of subthreshold slope. We observed Arrhenius-like behavior suggesting a thermally activated mobility with an activation energy E_A = 68 meV. Moreover the dependence of the charge carrier mobility on the organic semiconductor thickness has also been studied. The mobility decreased as the pentacene thickness increases whereas the threshold voltage and I_{off} current remain minimally affected. In order to understand the transport properties and in view to put in light morphology peculiarities of pentacene, AFM images were performed. It turns out that the pentacene grain sizes are smaller and disorganized as the film thickness increases, and charge carriers are more prone to be trapped, leading to decrease the field effect mobility and the I_{on} current. The devices were also tested under bias stress and the transistors with low thicknesses exhibited a relatively good electrical stability compared to those with high pentacene thicknesses. This work points out the influence of temperature, semiconductor thickness and bias stress effect on the device performance and stability of transistor using top gate configuration.

Keywords

Pentacene, Organic Transistor, Top Gate, Thin Film Transistor, Bias Stress,

Parylene

1. Introduction

In the last decades, organic electronic devices have received increasing interests. This is because they can be manufactured in large area, flexible substrates and low cost processing techniques. Thereby, a wide variety of related devices, like sensors, memories, flat display driving and RFIDs [1]-[6] based on organic semiconductor, have been experimentally demonstrated. The performance of organic field-effect transistors (OFETs) is becoming comparable to that of conventional amorphous silicon (Si) thin-film transistors so that they are currently being seriously considered for practical applications. In spite of the discovery of large number of organic semiconductor materials, pentacene is a prominent candidate for the active semiconducting layer in organic thin film transistors and it is one of the most promising candidates for industrial applications since Field-effect mobilities greater than 1 $cm^2 \cdot V^{-1} \cdot s^{-1}$ have been reported by many research groups [7] [8] [9].

Most applications using OFET are based on bottom gate devices in which the organic semiconductor is classically deposited onto the gate dielectric. So far, top gated devices are much less developed although some applications require this configuration. For instance, top gate device is more suitable for biosensor working in liquid media where the (bio) chemical species in solution to be detected interact directly with the gate dielectric of the transistor. The realization of top gate OTFT faces a technological challenge, *i.e.*, a noninvasive deposition of the gate dielectric. As organic transistors work in the accumulation regime, the conducting channel is very thin and the quality of the interface between the dielectric and the organic semiconductor needs to be controlled. On one side, depositions of inorganic dielectrics, usually including plasma, high temperatures or oxygen atmosphere, are detrimental to the organic active layer; while on the other side, polymeric dielectrics are often deposited via a liquid process where the solvent degrades the organic active layer in number of cases. Thus a specific care must be taken to avoid any damage to the sensitive underlying organic semiconductor and subsequent devices degradation. Several studies using top gate configuration have been reported such as dielectric lamination [10], parylene dielectric [11] [12] and inorganic material depositions [13], and CYTOP dielectric [14] [15], and so on.

An important factor influencing the transistor performances is probably the organic semiconductor growth. The quality of the layer and semiconductor growth enables to understand charge transport mainly expressed by the charge carrier mobility. Semiconductor active layer thickness is highly related to transistor performances as observed in several studies [16]-[23]. However most of these studies are based on Bottom gate configuration and very few investigations were performed in the so-called top gate configuration [24] [25] in which the

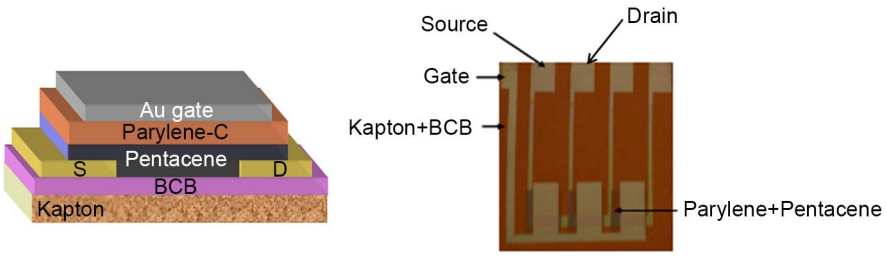
channel is located on the top of the semiconductor. In this configuration the last pentacene monolayers are playing an important role for charge transport as the channel conduction is close to the interface pentacene (the last monolayers)/ dielectric.

Besides, temperature is one of the fundamental physical parameters affecting several electronic devices. Variable-temperature studies of field effect transistor have been used to characterize charge transport mechanisms, and generally reveal thermally activated charge transport, with activation energies on the order of tens to hundreds of millielectronvolts [26]. The charge transport in OTFTs is still not well understood, even though there have recently been several models reported to explain the mechanism such as the multiple trapping and release [27] and variable range hopping [28].

In this work we investigate the effects of temperature dependence of electrical parameters as well the influence of pentacene thickness including gate bias stress in organic transistor using parylene-C as gate dielectric in top gate configuration.

2. Experimental Procedure

Nearly all plastic devices were processed on 125 μm thick kapton substrate which has been planarized by 3 μm thick benzocyclobutene photoresist layer (Cyclotene from Dow Chemical). **Figure 1** shows a schematic view of our top gate device. Gold source and drain contacts (50 nm Au) were deposited by joule evaporation through a shadow mask. Then pentacene was evaporated at different thicknesses (30, 60 and 100 nm unless otherwise stated) at a rate and a temperature of 0.02 nm/s and 70˚C respectively. Both substrate temperature and evaporation rate are of utmost importance for the organization of pentacene molecules on the surface and they must be carefully controlled for reproducible results. Pentacene was purchased from Sigma Aldrich without further purification. The gate dielectric was a 540 nm thick Parylene-C (DiX-C, Kishimoto Sangyo GmbH) layer deposited in a Specialty Coating Systems PDS 2010 labcoter 2 reactor. The deposition rate was 3 - 4 Å/s. Finally, a 100 nm thick Au gate was deposited onto parylene layer. The conduction channel was then localized on the top of the pentacene layer at the parylene/pentacene interface. Current-voltage characteristics were obtained in the dark with a probe station Keithley



(a) (b)

Figure 1. Schematic illustration of transistor in top gate configuration (a) and picture of the device (b).

2612 double source-meter under LABVIEW® environment. The devices were characterized in a closed cell at different temperatures in the range of 258 K - 353 K. The mobility was μ_{sat} extracted from the saturation region of the transfer curves with the equation:

$$I_{D,sat} = \frac{W}{2L}\mu_{sat}C\left(V_G - V_T\right)^2 \quad (1)$$

where $I_{D,sat}$ is drain current in the saturation regime, W/L is the width to length ratio, C is the capacitance per unit area, V_G the gate voltage and V_T the threshold voltage.

The morphology of the pentacene thin films was studied in an Amplitude Modulation mode Atomic Force Microscopy (AM-AFM) using the AFM Solver P-7, "stand alone" Smena-B (NT-MDT, Russia), with typical spring constant k of 22 N/m and tip radius of 10 nm. This mode was shown to be more appropriate than the contact mode to image soft materials such as polymers, functionalized surface and biological objects, in air.

3. Results and Discussion

Figure 1(a) and Figure 1(b) show respectively the schematic and the picture of top gate pentacene transistor fabricated on kapton substrate. As we can see the channel conduction is close to the interface between pentacene and Parylene-C. Figure 2(a) represents the output characteristics for 70 nm thick of pentacene; we clearly see a field effect transistor behavior with well-defined linear and saturation regimes with limited contact resistance although the transistor has a bottom contact configuration (Source and drain deposited before pentacene evaporation). The characteristics were also recorded with first increasing then decreasing of the drain voltage to assess the stability (not shown here). No hysteresis phenomenon between forward and reverse was observed. The transfer characteristics in saturation regime were shown in Figure 2(b) on a double scale, logarithmic and square root as function of gate voltage. We can determine the I_{on}/I_{off} ratio, the onset voltage and the subthreshold slope to be respectively 10^5, +8 V and 2.2 V/decade. The I_{on}/I_{off} ratio could be improved through a decrease of the I_{off} current by using pentacene purified and also by improved control of the interface. This latter point could be addressed by a better control of parylene deposition. In order to determine unambiguously the threshold voltage we use the second derivative method (SD) initially proposed for silicon MOSFETs and later adapted to OFETs [29] and we obtained a threshold value V_T = 0 V. Extracted field effect mobility (μ) in saturation regime was 1.5×10^{-2} $cm^2 \cdot V^{-1} \cdot s^{-1}$.

3.1. Temperature Dependence

The temperature dependence of the transport properties was investigated in the range of 258 K - 353 K. The transfer characteristics in logarithmic scale for device with 70 nm thick pentacene at different temperatures are plotted in Figure 3(a). When increasing T, the onset voltage remains constant and we record an increase of subthreshold slope, from 1.2 V/decade to 2.4 V/decade respectively

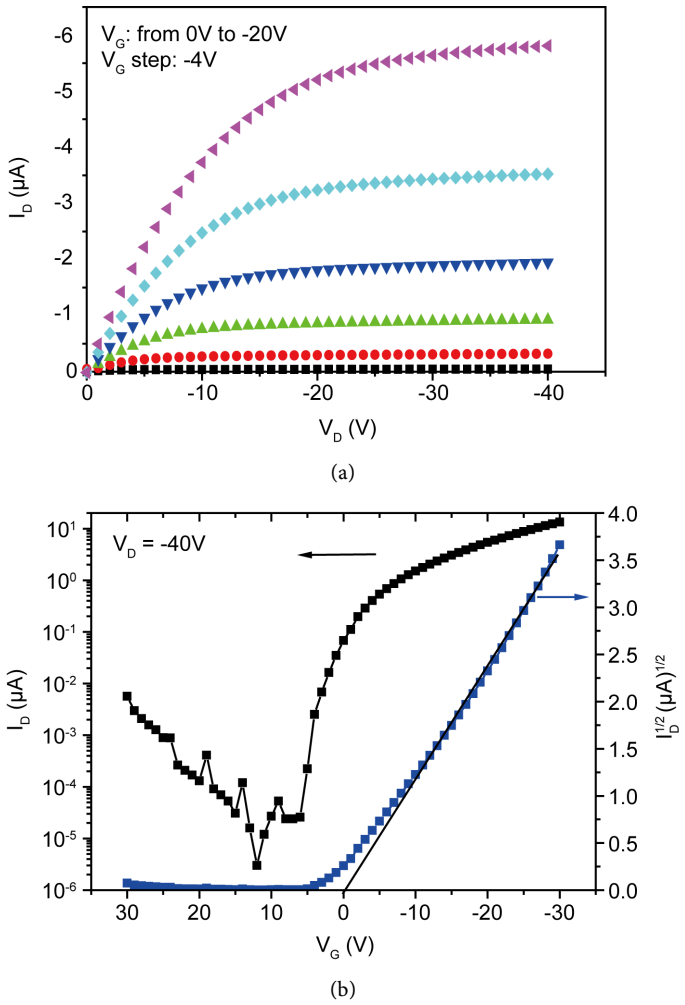
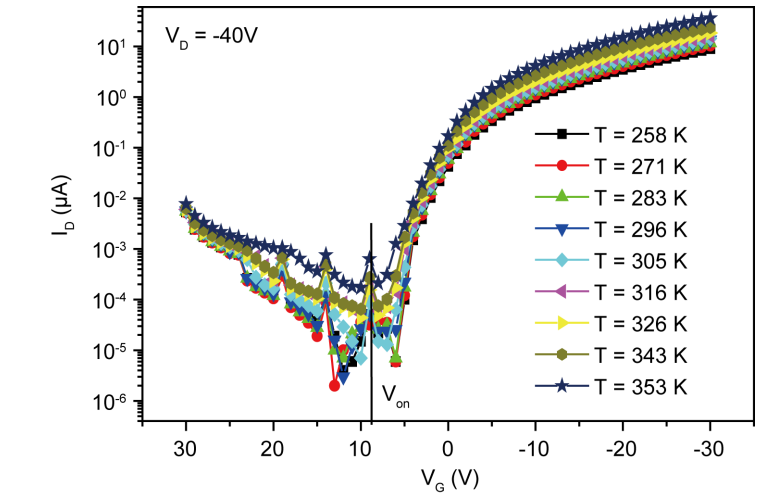
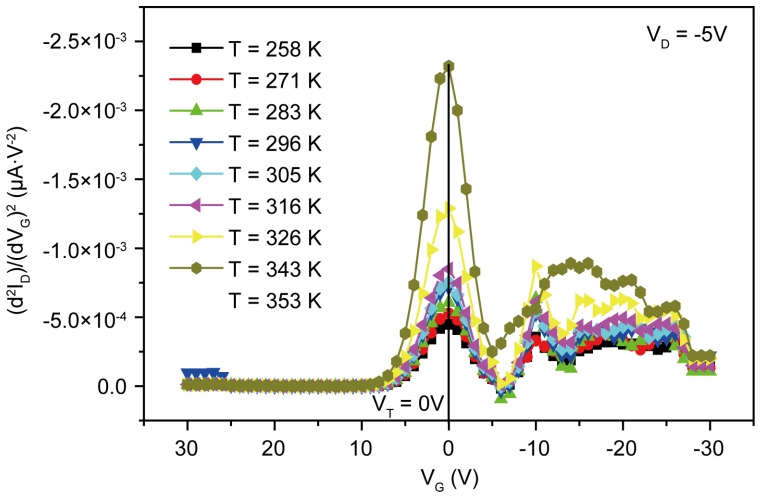


Figure 2. Output characteristics at different gate voltage (a), transfer characteristics in saturation regime at $V_D = -40$ V with 70 nm thick pentacene.

for 258 K and 353 K. The increase of the I_{off} current is only partially compensated by the increase of the I_{on} current and we also observe a slight decrease of the I_{on}/I_{off} ratio as T increases. The I_{on} current at final temperature measurement was found to be four times higher than that at initial temperature. The drain current increase with temperature was expected in polycrystalline material where conduction is based on variable range hopping. Similarly, the I_{off} current increase by nearly one order of magnitude from 258 K to 353 K. Structural changes in pentacene consecutive to annealing at a temperature higher than the deposition temperature could be suspected. A similar behavior was observed by Jung *et al.* [30]; the temperature increase enhances pentacene oxidation. The high electronegativity of oxygen compared to carbon and hydrogen atoms leads to modify the molecular chain and organic semiconductor doping, as consequence we observe an increase of conductivity. Infrared spectroscopy measurements showed that the pentacene layer was strongly oxidized since the temperature increased, giving rise to aldehyde and carboxylic acid formation [31]. The threshold voltage (**Figure 3(b)**) was determined in the linear regime for each



(a)



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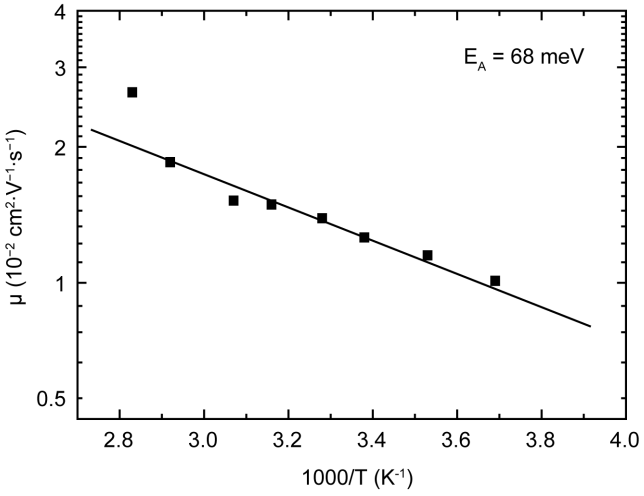


(c)

Figure 3. Transfer characteristics, in logarithmic scale and in saturation regime at V_D = −40 V (a), second derivative method to extract the threshold voltage V_T (b) in linear regime V_D = −5 V, the Arrhenius plot of the mobility in the saturation regime showing activation energy (c) with 70 nm thick pentacene.

measurement temperature from the SD method as reported above, and $V_T = 0$ V was found perfectly constant in the whole temperature range. Once the threshold voltage was unambiguously determined, the mobility in the saturation regime could be deduced according to (1). In order to gain more understand the transport property in the saturation regime, we have characterized the saturation carrier mobility as a function of temperature as shown in **Figure 3(c)**. In the temperature range of 258 K - 353 K, the field effect mobility increases from 1×10^{-2} $cm^2 \cdot V^{-1} \cdot s^{-1}$ to 3×10^{-2} $cm^2 \cdot V^{-1} \cdot s^{-1}$. We observed Arrhenius-like behavior with negligible deviations from linearity suggesting a thermally activated mobility and the activation energy is $E_A = 68$ meV close to the previous reported works [32] [33].

3.2. Thickness Dependence

It is well known in the OFET devices, the conductive active channel is located close to the gate insulator-semiconductor interface. Almost all charge carriers have been found within the 4 - 5 molecular layers. In the case of pentacene, it corresponds to a thickness of about 6 - 8 nm. Hence, channel formation in bottom gate transistors, is definitively related to organic semiconductor initial growth. The questioning is to know the situation in OFET with a top gate configuration for which the channel is located on top of the semiconductor beneath the dielectric layer and not in the first monolayers. **Figure 4(a)** and **Figure 4(b)** show the output and transfer characteristics respectively at $V_G = -40$ V and $V_D = -80$ V for 30, 60 and 100 nm thick pentacene. The electrical performance parameters are summarized in **Table 1**. As can be seen the I_{on} current increases as the pentacene thickness decreases in both output and transfer curves, while the I_{off} currents (inset in **Figure 4(b)**) remain quite unaffected as well as the threshold voltage (with a small shift around 2 V). Extracted mobilities are 0.035 $cm^2 \cdot V^{-1} \cdot s^{-1}$, 0.0150 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and 0.0058 $cm^2 \cdot V^{-1} \cdot s^{-1}$ for 30 nm, 60 nm and 100 nm of pentacene respectively. To explain this performance decrease in our transistors, two phenomena could be taken into account, 1) the charge injection carriers from the source and 2) the charge transport in the channel conduction. It is well known and reported that whenever the work function of the metal does not coincide with the valence band (or highest occupied molecular orbital) for *p*-channel devices or with the conduction band (or lowest unoccupied molecular orbital) for *n*-channel devices, an injection barrier with non-ohmic electrical behavior is formed at the metal-semiconductor interface [34] [35]. The charge

Table 1. Summary of the electrical parameter performances of top gate transistor at $V_D = -80$ V.

Pentacene thickness (nm)	μ ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	V_T (V)	I_{on} (μA)	I_{off} (μA)
30	3.2×10^{-2}	+7	−67.4	-5.5×10^{-4}
60	1.5×10^{-2}	+5	−30.9	-3.1×10^{-4}
100	5.8×10^{-3}	+6	−13.1	-3.1×10^{-4}

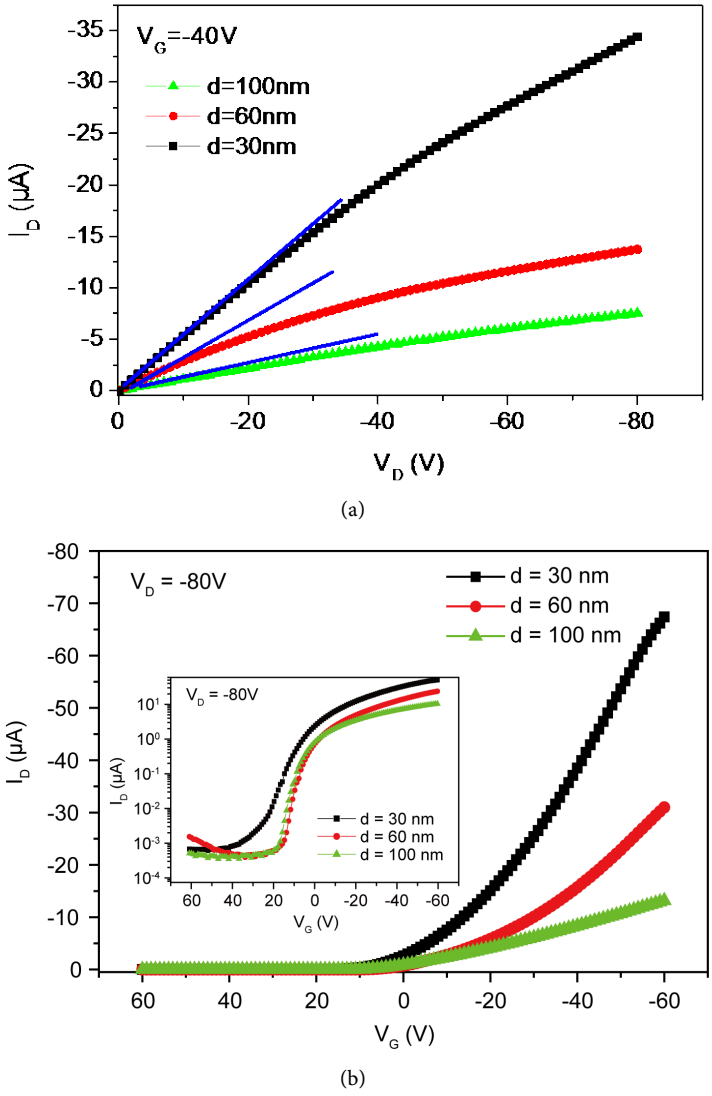
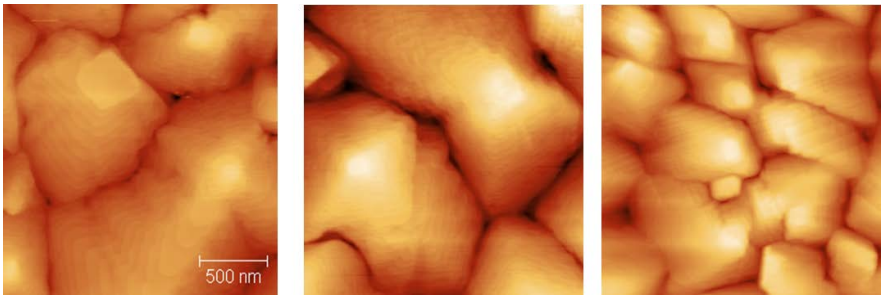


Figure 4. Electrical characteristics of transistor devices for different thicknesses, output characteristic for V_G = −40 V (a) and transfer characteristics and inset shows the logarithmic scale for V_D = −80V (b).

injection involves barrier height between gold work function and the HOMO level of pentacene. Although the structure is in top gate configuration, the source and drain electrodes are in bottom contact structure. When we look at the slopes ($\frac{\partial I_D}{\partial V_D}$ in blue lines) in I_D-V_D characteristics (**Figure 4(a)**), they are more tilted in thicker pentacene layers; this is especially a drawback for charges to be injected and transported into the channel with high contact resistance. Addi- tionally it has been reported [36] in bottom contact transistor; the pentacene growth in the channel and on the source/drain contacts was noticeably different. Therefore, compared to the organic semiconductor deposited in the channel region (on BCB) of a bottom contact device, the grain size on and near the source/drain electrodes tends to be smaller. Growth on the source/drain electrodes exhibited many grain boundaries which are a suitable environment for charge

trapping. The authors suggested that the presence of water molecules close to the contacts reduced the charge injection by a slight increase of barrier height between the HOMO level and gold source/drain work function. Additionally the polar water molecules residing in the grain boundaries of the channel transistor modified the pi stacking, and also changed the intermolecular interactions increasing subsequently energy barrier for charge carrier intergrain transport. All of these contributions lead to decrease the I_{on} current.

In view to put in light morphology peculiarities of pentacene, AFM images were performed to explain the thickness dependent morphology. Several works reported some correlations between surface morphology of pentacene and transport properties of bottom gate transistors [37] [38] [39]. **Figure 5(a)**, **Figure 5(b)** and **Figure 5(c)** show 2 × 2 μm^2 AFM pictures for 30, 60, and 100 nm of pentacene respectively. A Stranski-Krastanov mode can be inferred to the growth mechanism of pentacene on BCB, like what was observed in an earlier work, pentacene growth on PMMA [40] for instance. For all thicknesses, grains show a compact pyramidal shape as observed by Iazkov *et al.* [41]. Grain sizes are 1.56 μm, 1.03 μm and around 0.35 μm for 30 nm, 60 nm and 100 nm respectively. For 30 nm pentacene, we note 4.8 nm of root mean square and a peak-to-valley value up to 39 nm, while for 60 nm thick pentacene film we obtained 7.3 nm, 46 nm for peak-to-valley value respectively. For 100 nm of pentacene, the values are 10.2 nm of root mean square and a peak-to-valley up to 62 nm. As we can see the root mean square and peak-to-values increase as the pentacene thickness increases. The best electrical performances were obtained for pentacene thickness 30 nm, which corresponds to the thickness of the film with the largest grain size. The field effect mobility of the carriers decreases with the presence of traps and grain boundaries. The size of the islands is crucial for device performance and mostly depends on the deposition process, the substrate nature and the growth mode. The largest grain sizes reduce the number of grain boundaries acting as charge traps during the transport. Since the carrier mobility is very sensitive to the molecular ordering and grain boundaries, the larger grain size of pentacene will result in higher field-effect mobility [42]. This is confirmed by our experimental results which show that the highest mobility corresponds to films with the largest grains (30 nm pentacene thick in our case).



(a) (b) (c)

Figure 5. Pentacene morphologies obtained by AFM images for 30 nm (a), 60 nm (b) and 100 nm (c).

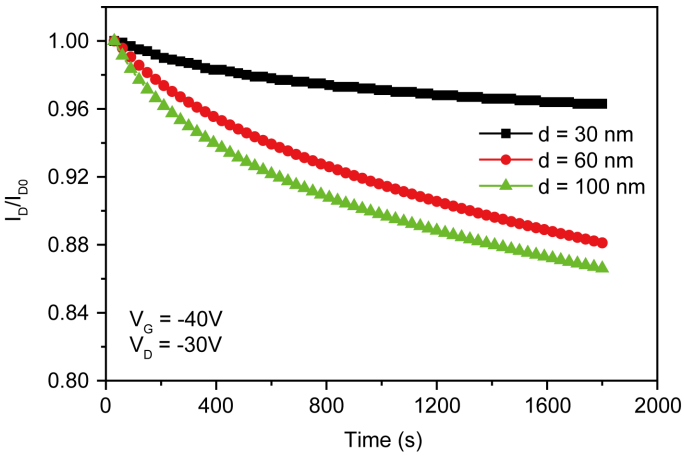


Figure 6. Decay of drain current under gate bias stress conditions ($V_G = -40$) at $V_D = -30$ V and $V_G = -40$ V for different pentacene thicknesses.

To study the electrical stability of our devices, a prolonged polarization during 1800 s was applied on the gate electrode (at $V_G = -40$ V by keeping $V_D = 0$ V) and the current recorded at $V_D = -30$ V and $V_G = -40$ V. The drain current (I_D) was used to monitor bias stress effect kinetic as it can be measured directly and continuously during bias stress and requires no extraction. **Figure 6** presents the time-dependent decay of drain current (I_D/I_{D0}) under bias stress conditions over 30 min for OFET with 30 nm, 60 nm and 100 nm thick pentacene. The current decay exhibited typical bias stress instability with an exponential decay function. While OFET based on 100 nm and 60 nm lost 15% and 12%, respectively, of their initial drain current, transistor with 30 nm of pentacene have reduced their performance only by 4%. The bias stress instability is not well understood and remains unclear regarding the physical origin, however few mechanisms have been proposed as defect generation, the formation of bond hole pairs, charge trapping and migration of mobile ions [43] [44] [45] [46] [47]. In the present study, the presence of numerous grain boundaries in 100 nm and 60 nm thin films are suitable to water molecules diffusion until the interface with the dielectric layer could be responsible to the high current decrease. The orientation of water dipoles after electric field application changes the local polarization of the organic semiconductor monolayers, creating trap states in the band gap [48]. These traps may be attributed to states above the HOMO level (donor-like) which decrease the mobile charge density. On the contrary, transistor with 30 nm thick pentacene beneficiates of large grains sizes which reduce the impurity penetration and their diffusion through the pentacene active layer to the interface with the parylene dielectric.

4. Conclusion

Our studies bring light on the role of temperature and pentacene microstructure in top gate transistor. We have investigated the influence of temperature and organic semiconductor thickness on the electrical parameters. Our findings revealed that in the temperature range of 258 K - 353 K the field effect mobility is

thermally activated with activation energy close to 68 meV. No threshold voltage change has been recorded, however, in the subthreshold regime the I_{off} current increased and the subthreshold slopes are slightly degraded, a sign of interface deterioration. Thickness dependent studies on pentacene top gate transistor exhibited that the best electrical performances are obtained with low pentacene thickness in the range of 30 nm - 100 nm. These results were correlated to AFM images which revealed large grain sizes and well-organized structure at lower thicknesses, moreover the associated device remains relatively stable under gate bias stress compared to that using thicker pentacene confirming less charge trapping for a low pentacene thickness.

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