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Effect of Temperature Dependence on Electrical Characterization of *p-n* GaN Diode Fabricated by RF Magnetron Sputtering

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Abstract

The *p-n* junction GaN diodes were all fabricated by sputtering technique with cermet targets for *p*- and *n*-type GaN and metal targets for electrodes. The interface of these *p-n* junction GaN diodes examined by high-resolution transition electron microscopy was clear and distinguishable. Lattice images identified the complete dissolution of Mg into the Ga site. At the room temperature, the diode had the turn-on voltage of 2.2 V, the leakage current of 2.2×10^{-7} A, the breakdown voltage of −6 V, the barrier height of 0.56 eV, ideality factor of 5.0 by *I* (current)-*V* (voltage) test and 5.2 derived from the Cheungs' method, and series resistance of 560 Ω. These electrical properties were investigated at different testing temperatures from room temperature to 200˚C. The temperature dependence in the *I-V* characteristics of the *p-n* diodes can be successfully explained on the basis of thermionic-emission mode.

Keywords

***p-n* GaN Diode, *I-V* Measurement, Barrier Height, Leakage Current, Cheungs' Method**

1. Introduction

GaN material is one of the important semiconductors for high-power electronics due to its wide band gap characteristics. The nitride-based materials have brought promising future for the application of electronic devices such as metal-oxide-semiconductor field effect transistor (MOSFET) and hetero junction field-effect transistor

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(HJ-FET), Schottky diodes, *p*-*n* junction diodes, laser diodes, and light emitting diodes (LEDs). Many researchers have investigated onidentifying carrier recombination centers, defects and impurities, to improve the GaN devices performance [1]-[3]. Such a development from *n*-GaN to *p*-GaN is very important for the investigation of Schottky and *p*-*n* junction diodes based on GaN films. Generally, the *p*-*n* junction diodes will have larger turn-on voltages, lower leakage currents, larger breakdown voltages, and slower switching speeds as compared to Schottky diodes [3]. In the fabrication of *p*-*n* junction LED using nitride semiconductor materials, high efficiency and prevention of thermal degradation to get low turn-on voltages of the device are necessary. So, using nitride semiconductor materials to investigate the *p*-*n* diodes, the control on the turn-on voltage is the important issue [4]. Moreover, another important requirement for *p*-*n* diodes is to have a highly conductive *p*-type layer with a high holes concentration [5]-[8].

Several groups have put many efforts to explore *p*-*n* junction diodes with different approaches. Cao *et al*. reported the fabrication of n^+-*p* junction in GaN by implantation of $^{29}Si^+$. They determined that the breakdown voltage was 13 V at the reverse bias and ideality factor *n* was ~2 [1]. Lee *et al*. studied the effect of *p*-GaN layers on the turn-on voltage of LED. They found that the turn-on voltages at forward bias were in the range of 5.5 - 6.5 V with the incorporation of various amount Mg during growth in *p*-GaN layer [4]. Gupta *et al*. investigated the *p*-*n* junction based on ZnO and copper phthalocyanineusing pulsed laser deposition and thermal evaporator techniques. After *I*-*V* measurement at the room temperature, they reported that the barrier height and ideality factor were 0.63 ± 0.02 eV and 4.0 ± 0.3, respectively [5]. They also applied Cheungs' and Norde methods to compare the junction parameters. Hwang *et al*. examined the characteristics of light-emitting diode comprised of *p*-ZnO/*n*-GaN hetero junction. The threshold voltage and leakage current were found at 5.4 V and 2×10^{-4} A, respectively [6]. Liu *et al*. investigated the In GaN-based light-emitting diode with a *p*-*n* GaN homojunction. The ideality factor was estimated to be 2.11 at voltage regime of 2 V and barrier height was determined to be 0.77 eV at the room temperature [7]. Park *et al*. studied the electrical characteristics of a GaN nanorod *p*-*n* junction diode patterned on the SiO_2 substrate using e-beamlithography [8]. It was observed that the ideality factor varied from 2460 at 6 K to 13 at 298 K, with a large deviation for the ideal unit. The resistance linearly decreased from 0.05 to 0.0034 MΩ with the increasing temperature from 100 to 296 K. In the other paper, they reported the electron trapin the GaN nanorod *p*-*n* junction grown by molecular-beamepitaxy [9]. Data from the *I*-*V* curve showed the turn-on voltage of 7.2 V and breakdown voltage of −9 V at low temperature of 6 K. By increasing the temperature up to 300 K, the turn-on and break down voltages reduced to 0.4 and −0.8 V, respectively. Mohd Yusoff *et al*. described the growth and characterization of *p*-*n* junction diode based on GaN grown on Si (111). Using *I*-*V* measurement for the 700˚C-annealed GaN grown on AlN/Si (111) substrate, they determined that the extractedideality factors had the range of 15.14 - 19.68, decreasing with an increase in testing temperature (30˚C - 104˚C) [10]. Zhang *et al*. fabricated the *n*-ZnO/*p*-GaN hetero junction on GaN single crystal substrate with RF magnetron sputtering for ZnO. The threshold voltage was found to be 2.5 V from the *I*-*V* data. The current increased rapidly when forward bias was above 2.5 V and it was strongly blocked under reverse bias. Their series resistance (R_s) of the device was determined to be 102 Ω from the slope of the curve $I/(\mathrm{d}I/\mathrm{d}V)$ versus *I* [11]. All the above-mentioned reports have their GaN films grown by the techniques of metal-organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE). Some of their excellent performances are established on the GaN layers with the epitaxial quality for LEDs [1] [4] [7].

Radio-frequency (RF) reactive sputtering technique has been chosen as a method to grow the *p*- and *n*-type GaN layers for the *p*-*n* junction GaN diodes. The advantages of using the sputtering technique include lower deposition temperature, low equipment cost, and secure working atmosphere without using the toxic metal-organic precursors and ammonia [12]-[15]. In this study, the electrical *I*-*V* characteristics of *p*-*n* GaN diodes were determined by the thermionic emission (TE) modeat a wide testing temperature range of 25˚C - 200˚C.

2. Experimental Procedures

Mg-doped GaN (Mg-GaN) films have been deposited on Si (100) and Pt/TiO_2/Si substrates at 400˚C for 40 min by RF reactive sputtering. The Mg content of (Mg-GaN) cermet targets was 10% [13]. The RF power was kept at 150 W under the mixture of Ar and N_2 gases at a flow rate of 5 sccm for each. The working pressure during sputtering was kept at 9×10^{-3} torr. After depositing *p*-GaN films, the *n*-GaN layers were also grown on Si (100) and *p*-GaN/Pt/TiO_2/Si substrates at 200˚C for 40 min with a Ga/GaN cermet target (**Figure 1**). The process was kept at RF power of 120 W under the similar Ar and N_2 flow rates. Pt and Al deposited by direct-current sputtering were used for the electrodes of *p*-*n* GaN diode. Aluminum layer was sputtered at 200˚C for 30 min with

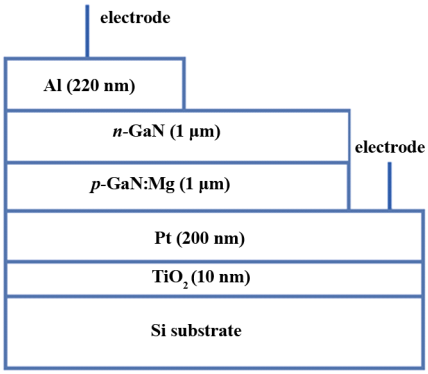


Figure 1. Layers structure of a *p-n* GaN homo junction diode.

a pure Al target. During Al deposition, only Ar gas was used at a flow rate of 5 sccm meanwhile the RF power was kept at 80 W. The detailed experimental procedure for depositing the GaN films can be referred to our previous work [12] [13].

Surface root-mean-square (rms) roughness of Mg-GaN and GaN films was evaluated by atomic force microscopy (AFM, Dimension Icon, Bruker). Before testing TEM images, the FIB system was used to cut samples in *p-n* GaN device. High-resolution transmission electron microscopy (HR-TEM, Tecnai G^2 F20, Philips), operating at 200 keV was used to the determine the SEAD pattern, lattice images of films, and the cross-sectional image of devices. The electrical *I-V* characteristics of *p-n* GaN diodes were determined by using Semiconductor Device Analyzer (Agilent, B1500A) in the temperature range of 25˚C - 200˚C.

3. Results and Discussion

3.1. Structural and Surface Morphological Characteristics

Hall effect measurement (HMS-2000, Ecopia) was conducted for the electron concentration (N_d), hole concentration (N_p), and carrier mobility (μ) of *n*- and *p*-GaN films at the room temperature. As a result, they were found to be $N_d = 5.8 \times 10^{17}$ cm^{-3} and $\mu = 11$ cm^2/Vs for *n*-GaN film and $N_p = 2.1 \times 10^{17}$ cm^{-3} and $\mu = 26$ cm^2/Vs for *p*-GaN films. In our previous study on materials development, the band gap E_g values of *n*-GaN deposited at 200˚C and *p*-GaN deposited at 400˚C were found to be 2.99 and 2.96 eV, respectively [12] [13].

The layers structure of *p-n* GaN homo junction diode is shown in the **Figure 1**. The cross-sectional TEM image of the *p-n* GaN diode structure is shown in **Figure 2(a)**. Each layer of the diode exhibited good adhesion. The interface between *p*- and *n*-GaN layers was crack- and pore-free. The interface between *n*- and *p*-GaN is clearly distinguished, which indicates interfacial diffusion is minimized because of depositing firstly *p*-GaN at higher temperature of 400˚C followed by *n*-GaN at lower temperature of 200˚C. The thicknesses of Al and Pt electrodes were 200 and 220 nm, respectively. The $Pt/TiO_2/Si$ combination has been popularly used for the study of non-volatile memory. The thicknessof *n*- and *p*-GaN layers was found to be 1 µm. As an original work, the thickness effect on the diode performance needs further investigations.

The high-resolution (HR) TEM lattice images of films are presented in **Figure 2(b)** for *n*-GaN and **Figure 2(c)** for *p*-GaN. The insets show the selected area electron diffraction (SAED) patterns. The *n*- and *p*-GaN phases were clean and had no second phases. The lattice images provide important evidence to support the homogeneity of the *n*- and *p*-GaN deposited by reactive sputtering. It is especially important for *p*-GaN, because this information can guarantee the complete dissolution of Mg dopant into the Ga lattice site to form the complete solid solution without phase segregation. The Mg solubility in GaN is well known for using the MOCVD technique. Our lattice images indicate that the sputtering kinetic energy is strong enough to dissolve Mg into the Ga lattice. For the *n*-GaN layer, the measured *d*-space value was 2.76 Å, which corresponded to the $(10\bar{1}0)$ crystalline plane. Other crystalline plane such as $(10\bar{1}1)$ and $(11\bar{2}0)$ could also be observed from the SAED pattern. For the *p*-GaN layer, the measured *d*-space value had a bigger value of 2.77 Å due to the lattice expansion by using the bigger Mg dopant of 0.66 Å to substitute the smaller Ga of 0.62 Å. The HR lattice image of *p*-GaN exhibited similar crystalline $(10\bar{1}0)$ plane. However, the $(10\bar{1}1)$ plane still showed in SAED pattern. Both of *n*- and *p*-GaN films show the polycrystalline nature. The *n*-GaN has a ring diffraction pattern contributed from different

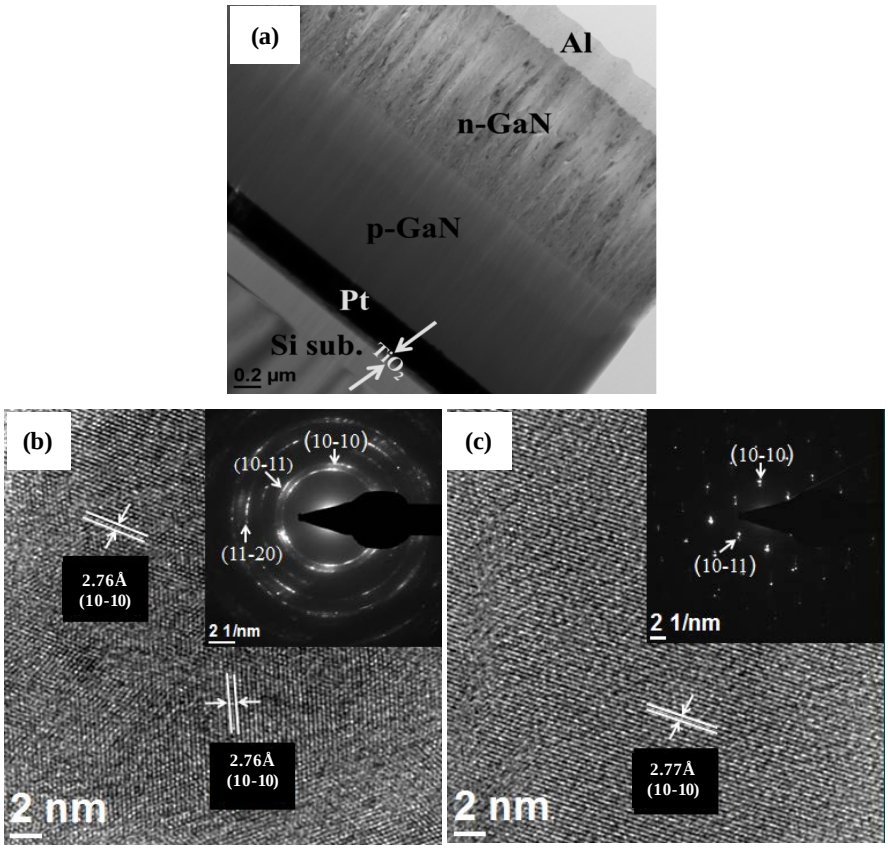


Figure 2. TEM micrographs of (a) *p-n* GaN diode structure, (b) *n*-GaN layer, and (c) *p*-GaN layer.

crystalline planes. The *p*-GaN shows the dotted pattern, which indicates the *p*-GaN has the tendency to become single crystal-like. In addition, the XRD results from our previous indicate that full-width at half-maximum (FWHM) at $(10\bar{1}1)$ is 0.30 for pure *n*-GaN and 0.25 for *p*-Mg-doped GaN at 10% [13]. The addtion of 10% Mg improved slightly the structure of GaN. The instead of excess (~15%) and less (~5%) Mg-doped GaN films, the FWHM of $(10\bar{1}1)$ was increased to 0.30 and 0.34, respectively. The TEM characterization supports with the evidence that Mg doping can improve the crystallinity of the growing *p*-GaN films.

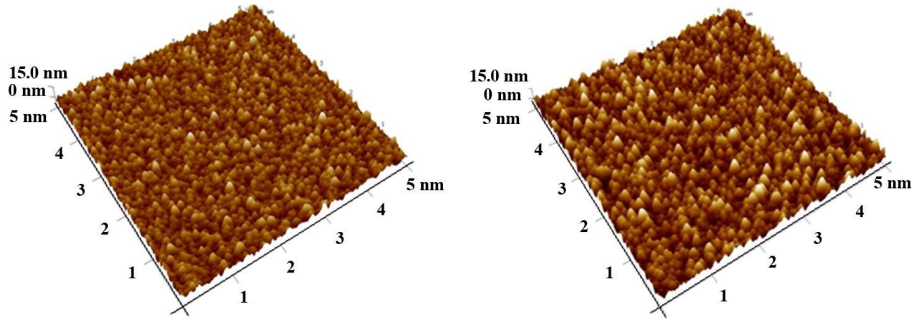
Surface topographies of both GaN films were analyzed by AFM, as shown in **Figure 3(a)** and **Figure 3(b)**, respectively. The root-mean-square (rms) roughness values of *n*- and *p*-GaN were found to be 2.42 and 3.12 nm, respectively. The grains become larger and the surface rougher due to the Mg doping into the GaN films. The surface roughness of *p*-GaN can be attributed to the disturbance of growth kinetics by the Mg dopant or a difference in atomic size between Ga and Mg, which made the lattice distortion and dislocation generation.

3.2. Current-Voltage (*I-V*) Characteristics

Figure 4 shows the plot of the *I-V* characteristics of *p-n* GaN diode at the room temperature. The leakage current of *p-n* GaN diode was 2.2×10^{-7} A at −1 V. The turn-on voltage was found at ~2.2 V for the forward bias, and the breakdown voltage was determined above −6 V.

The forward and reverse *I-V* characteristicofa *p-n* GaN diode was also determined at the different testing temperatures. The electricalcharacteristics can be generally evaluated by using an equation based on a well-known standard thermionic-emission (TE) relation for electron transport from a metal-semiconductor contact (for $qV > 3$ kT) [5] [14] [16]. It can be given as below

$$I = I_0\left[\exp\frac{qV}{nkT}V - 1\right] \quad (1)$$



(a) (b)

Figure 3. AFM topographies of (a) *n*-GaN filmdeposited at 200˚C and (b) *p*-GaN filmdeposited at 400˚C.

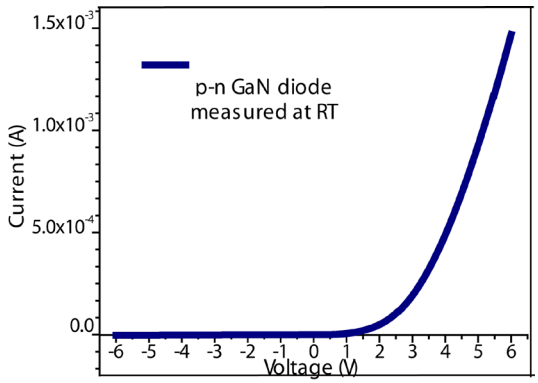


Figure 4. Electrical properties of *p-n* GaN homo junction diode measured at the room temperature (RT).

where V is applied voltage, T the experiment temperature in Kelvin, n ideality factor, I_0 saturation current, q the electronic charge, and k the Boltzmann constant. The saturation current is expressed by

$$I_0 = AA^*T^2 \exp\left(-\frac{q\phi_B}{kT}\right) \tag{2}$$

where A^* is the effective Richardson constant, A the diode area, and ϕ_B the barrier height. In the present work, the *p-n* GaN diode has a square shape and its area was measured to be 1 mm^2. The theoretical value of A^* was found to be 26.4 Acm^{-2}/K^{-2}, based on the effective electron mass ($m^* = 0.22\ m_e$) for GaN [16]-[19]. The plot of ln I versus V, based upon Equation (1), can beused to derive the saturation current, which can be obtained by extrapolated the straight line of the linear region of the semilog plot to zero applied voltage. The barrier height of the *p-n* GaN diode is defined as

$$\phi_B = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_0}\right) \tag{3}$$

In addition, the calculation of the ideality factor n is based upon the pure TE mode. It can be obtained from the slope of the linear region of ln I-V characteristics under the forward bias. It is given by [5] [16]-[19]

$$n = \frac{q}{kT}\left(\frac{\mathrm{d}V}{\mathrm{d}\ln I}\right) \tag{4}$$

Figure 5 shows that the logarithmic plot of I-V characteristics as a function of testing temperature (25˚C - 200˚C). It is noted that the leakage current at the reverse bias of −1 V goes up from 2.2×10^{-7} A at RT to 1.7×10^{-5} A at 200˚C. The barrier heights, based on equation (2) and (3), were found to increase from 0.56 eV at 25˚C

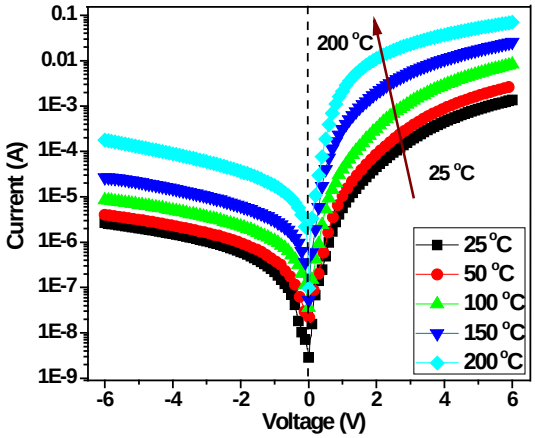


Figure 5. The forward and reverse current-voltage characteristics of a *p-n* GaN diodein the testing temperature range of 25˚C - 200˚C.

to 0.69 eV at 200˚C. By using Equation (4), the ideality factor *n* decreased with the increase in the testing temperature, dropped from 5.0 at 25˚C to 2.5 at 200˚C. These achieved parameters for the diode with all layers made by sputtering are consistent with the reported values in some previous papers for *p-n* junction diodes with GaN made by MOCVD [5] [9].

3.3. Calculations the Series Resistance R_s and Ideality Factor *n*

The series resistance R_s and the ideality factor *n* are very important parameters. The *I-V* characteristics deviate considerably with the change in ideality factor *n* due to the effect of series resistance R_s. The series resistance R_s and ideality factor *n* of a *p-n* diodes can be determined by using the Cheungs' method [20], which is defined as below

$$\frac{\mathrm{d}V}{\mathrm{d}(\ln I)} = \frac{nkT}{q} + IR_S \tag{5}$$

As can be seen **Figure 6**, the plot of d*V*/d (ln*I*) versus *I* will be linear (based on Equation (5)). The slopes will give the values of series resistance R_s and the intercepts will give the values of ideality factor *n* [5] [15] [18] [20]. **Table 1** also provides the results from a detailed calculation of the series resistances R_s and ideality factor *n* by the Cheungs' method.

3.4. Discussion

Table 1 shows a comparison of data derived from the *I-V* data for the all sputtering-made *p-n* GaN diode. It is noted that the ideality factor *n* decreases whereas the barrier increases with the increase in the testing temperature. This result can be attributed to the combination of the low and high barrier heights of diodes with the *I-V* behavior in the standard TE mode. At the room temperature, the flow of the electron transport across the metal-semiconductor interface of devices is able to overcome the lower barriers. Therefore, the current transport will be determined by electrons flowing through the path of lower barrier height and a larger ideality factor. When the testing temperature increases, more and more electrons will have sufficient energy to transcend the higher barrier. As a result, the dominant barrier height will increase with increasing the testing temperature [17]. Other reasons are the inhomogeneous thickness of films and non-uniformity of the interfacial charges to lead to the increase in ideality factor and the decrease in the barrier height for testing at lower temperatures. In addition, the increase in the carrier concentration of GaN layers and the decrease in the parasitic resistances found at the higher testing temperature also have caused the rise of barrier height and the fall of ideality factor [21].

Similar results were also determined by Hsueh *et al*. [21]. They investigated the temperature dependence of the current-voltage characteristics of *n*-$Mg_xZn_{1-x}O$/*p*-GaN hetero-junction diodes. They concluded that at asubstrate temperature of 25˚C there was the lowest leakage current at the reverse bias. Furthermore, the extracted ideality factors *n* were in the range of 3.86 - 7.00, decreasing with an increase in the testing temperature (25˚C - 125˚C).

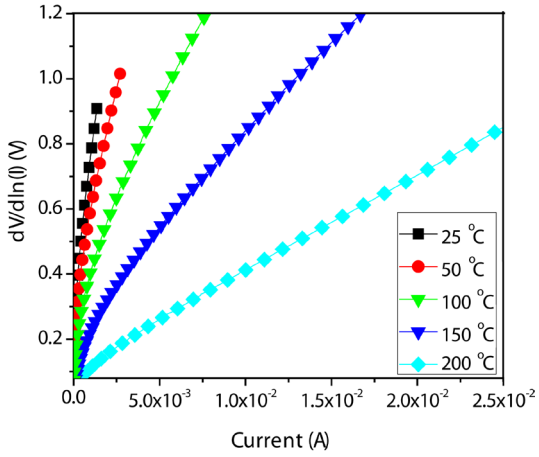


Figure 6. Plot of d*V*/dln(*I*) versus *I* for *p-n* GaN diode in the temperature range of 25˚C - 200˚C.

Table 1. The parameters calculated from electrical characteristics of a *p-n* GaN diode as a function of testing temperature.

Temp (˚C)	Leakage current (A) at −1 V	Barrier height	From *I-V*	Cheungs' function d*V*/dln(*I*) vs *I*	
		ϕ_B (eV)	*N*	*Rs* (Ω)	*n*
25	2.2×10^{-7}	0.56	5.0	560	5.2
50	3.8×10^{-7}	0.59	4.6	362	4.9
100	1.1×10^{-6}	0.63	3.7	165	4.0
150	3.1×10^{-6}	0.67	3.1	78	3.4
200	1.7×10^{-5}	0.69	2.5	38	2.7

In the other paper, they also investigated the *I-V* characteristics at different testing temperatures for Al-doped $Mg_xZn_{1-x}O$/AlGaN junction diodes with Mg-ZnO made by RF sputtering on the MOCVD-grown AlGaN. The extracted ideality factors were found in the range of 5.04 - 15.90, decreasing as the testing temperature increased from 25˚C to 125˚C [22]. Mohd Yusoff *et al*. described the growth and characterization of *p-n* junction diode based on GaN grown on Si (111) [10]. The leakage current was found 1.32×10^{-6} at the room temperature. The ideality factors *n* had the range of 15.14 - 19.68, decreasing with an increase in testing temperature (30˚C - 104˚C). Chen *et al*. studied the current rectification in a single GaN nanowire with a well-defined *p-n* junction [23]. Their ideality factor was calculated in the range of 5.5 - 6.5. The higher ideality factor was also obtained after testing at lower temperatures.

It is observed that there is a small difference between the values of ideality factor obtained from the ln*I-V* plot at forward bias and from the d*V*/d(ln*I*)-*I* plot. This difference could be due to the presence of series resistance, interface states, and the voltage drop across the interfacial layer [21]-[23]. A good diode is expected to have small temperature dependence in ideality factor. So, the observed high ideality factor could be due to several reasons such as accelerated recombination of electrons and holes in depletion region, the presence of interfacial layer, and the imperfections which may be due to the presence of crystalline and amorphousregions [5] [6].

From **Table 1**, there is also a clear trend of decreasingtheseries resistances R_s with a rise in the testing temperature. The R_s values were observed to drop from 560 Ω at 25˚C to 38 Ω at 200˚C. The fall in R_s for *p-n* GaN diode tested a higher temperature indicates that the diode has smaller ideality factor, more free electrons leading to the high current, and smaller series resistance in the forward bias.

4. Conclusion

p-n GaN diodes have been successfully fabricated only by using the cost-effective magnetron sputtering. The *p-n* diode has a good homo-junction with a distinguishable interface and free of voids and cracking. The leakage

current, turn-on voltage, ideality factor, and breakdown voltage of the diode device, obtained from *I-V* measurements, were found to be 2.2×10^{-7} A, 2.2 V, 5.0, and −6 V, respectively, at room temperature. With increasing the testing temperature, the barrier height increased from 0.56 eV at 25˚C to 0.69 eV at 200˚C; the ideality factor decreased from 5.0 to 2.5 for *I-V* tests and from 5.2 to 2.7 from Cheungs' method; and the series resistance decreased from 560 Ω to 38 Ω. It is observed that the ideality factor and series resistance decrease whereas the barrier height increases as the testing temperature increases.

Acknowledgements

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