Scientific Research

Designs of All-Optical Higher-Order Signed-Digit Adders Using Polarization-Encoded Based Terahertz-Optical-Asymmetric-Demultiplexer (TOAD)

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Abstract

Various designed circuits for multiple-valued all-optical arithmetic are demonstrated. The terahertz-optical-asymmetric-demultiplexer (TOAD) switch is used as the basic structure unit in the proposed circuits due to its compact size, thermal stability, and low power operation. The designs of trinary and quaternary signed-digit numbers based adders are presented using different polarized states of light. These proposed polarization-encoded based adders use much less switches and their speeds are higher than the intensity-encoded counterparts. Further, it will be shown that one of the proposed trinary signed-digit adders is twice as fast as a recently reported modified signed-digit adder.

Keywords

Multiple-Valued Signed-Digit, All-Optical Gates, Polarization-Encoding, Terahertz-Optical-Asymmetric-Demultiplexer (TOAD)

1. Introduction

Multiple-valued logic and arithmetic is being extensively investigated as being a promising choice for future digital and optical computing [1]-[10]. Redundant signed-digit is among the various multiple-valued number systems [11]. Attractions features of this choice are higher information transmission, higher data storage *i.e.* more logic density and higher processing speed due to the opportunity of having parallel computing algorithms

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[12]. The addition/subtraction of two signed-digit numbers restricts the carry propagation to one or two adjoining digits. Many researchers proposed optoelectronics implementations to achieve fast computing arithmetic [13]-[18]. On the other hand, the recent developments in all-optical switches that are capable of demultiplexing Tb/s pulse trains push the researchers to shift towards all-optical implementations to design ultra-fast logical and arithmetic units using binary and nonbinary algorithms [19]-[24].

Recently, all-optical arithmetic operations based on terahertz-optical-asymmetric-demultiplexer (TOAD) switch were demonstrated [20] [22]. All-optical multiple logic gates (XOR, NOR, NAND) as well as binary half- and full-adders were reported using parallel TOAD structures. Further, with the help of TOAD switches, fast nonbinary adders were demonstrated [23] where the input and the control signals are all-optical in nature. The high speed is achieved due to the use of the nonlinear optical materials and the nonbinary modified signed-digit (MSD) number representation. In contrast to binary adder, the proposed circuits can be extended to *n* digits by employing additional stages without affecting the total addition time. Since the multiple-valued digits cannot be directly implemented using the two binary states of the TOAD switches, intensity-encoding schemes are used to transform the signed-digits into binary bits. More recently, the intensity-encoded MSD adder was improved in terms of its TOAD switches count and its speed by utilization of polarization-encoded scheme [24].

Now since multiple-valued logic/arithmetic is being viewed as an interesting approach in optical information processing, we present, in this paper, design methods to implement trinary signed-digit (TSD) and quaternary signed-digit (QSD) arithmetic. TSD and QSD number systems are represented by five and seven literals, respectively. Consequently, the two-bit intensity-encoding (light, no light) scheme, as reported in [24], cannot be used in designing the higher-order signed-digit (SD) adders. A straightforward solution is to use a three-bit intensity-encoding scheme for each SD literal. However, in this case the all-optical circuit implementation will be very complicated. Alternatively, this limitation is solved by proposing the polarized state of light (vertical and horizontal) and a two-bit encoding scheme. The polarization-encoding method is used to design fast all-optical TSD and QSD number based adders. The proposed adders are compared in terms of numbers of gate delays, TOAD switches, beam combiners, and polarization converters. Further, these circuits are compared to the previously reported MSD adder [24]. It will be shown that the TSD adder is two times faster than the MSD one; while the QSD adder speed is the same. Sections 2 and 3 will briefly review the operation of the TOAD switch and the SD number representation, respectively. Section 4 and 5 provide five adder designs: three for the TSD and two for the QSD adders. In section 6, we summarize the results and make some conclusions.

2. Operation of TOAD Based Optical Switch

In the last few years, the TOAD switch [19] was extensively used in realizing various ultrafast logical and arithmetic operations. Its speed is due to its capability of demultiplexing tera bits per second pulse trains where a light signal controls another light beam. In addition to its speed, the relatively low power consumption makes it attractive for large-optical integration. TOAD switch consists of a loop mirror with an intra loop 2×2 coupler and a semiconductor optical amplifier (SOA) which is offset from the loop's midpoint by a distance Δx as shown in **Figure 1(a)**. The SOA constitutes the nonlinear element within the switch where when exposed to a strong light it saturates and its index of refraction is changed. Full details of the operation of the TOAD switch is explained in [19] [22]. The TOAD switch operates with two lights signal through nonlinear interaction in a material based on interferometer setup: a strong optical signal, called the control pulse—*CP*, and another optical signal, called the incoming pulse—*IP*.

Briefly, the TOAD switch works as follows. When there is no CP signal, the *IP* signal enters the loop shown in **Figure 1(a)** and splits into two counter propagating ones. These two signals now recombine and interfere at the input coupler and emerge as a single light at the input port. However, if a strong *CP* light is injected into the loop causing the SOA to saturate and its index of refraction is changed. Consequently, the two *IP* counter propagating signals will face differential phase shift such that they will interfere and re-emerge or transmitted from the output port. At the two ports (reflected and transmitted), a polarization or wavelength filter is used to block the optical *CP* signal and only pass the optical *IP* signal. The energy of the optical *CP* must be sufficient to modify the optical property of the SOA element whereas the two counter propagating *IP* signals do not. Further, the *IP* and the *CP* signals are to be entered the SOA at about the same time. Further, in the absence of the *CP* signal, the input light exits from the lower port in the figure (no light is present in the upper port). However, when both CP and *IP* signals are present simultaneously, all light is directed towards the upper port because of the refractive-index change induced by the *CP* signal (no light is present in the lower port). When there is no *IP*
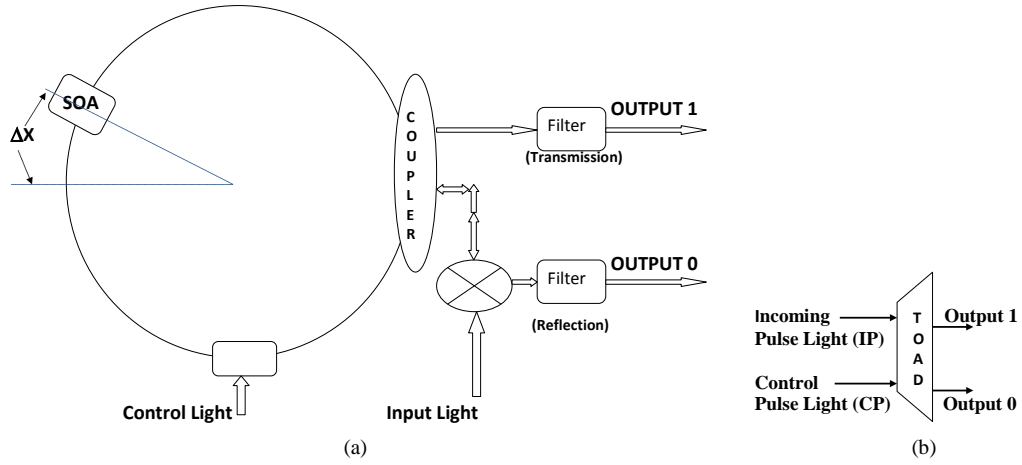
Figure 1. (a) TOAD-based optical switch; (b) a schematic diagram for the switch.

signal, both channels receive no light as the filter blocks the *CP* signal. A schematic block diagram for the TOAD switch is shown in **Figure 1(b)**.

TOAD switches can successfully be used for designing logical circuits. For instance, cascaded TOAD switches as shown in **Figure 2** are used to generate the sixteen minterms for four input logical variables $\left(x_i^1 x_i^2 y_i^1 y_i^2 \right)$. This structure can be viewed as a 1×16 decoder where only one output is activated that corresponds to a specific minterm. Note that the output ports are numbered according to the corresponding generated minterms. *OR*-ing of these minterms (sum-of-products) is performed with flexible outputs interconnectivities (beam splitters/combiners) and *ANDing* operations are achieved by cascading stages (switches) where any output port signal can be used as an input to another switch. Note that in this case, the output optical signal of the first switch may need to be amplified and/or wavelength converted before it is fed to the next switch. As a result, this switch structure can be used as a preliminary non minimized basic building block to realize any logical Boolean function.

3. Signed-Digit Numbers

Signed-digit (SD) numbers are formally defined as follows [12]: given a radix *r*, each digit of SD number assumes $(2\alpha + 1)$ values of the digit set $\{-\alpha,\ \cdots, -1, 0, 1,\ \cdots, \alpha\}$ where $\alpha \leq r - 1$ and $r \geq 3$. In general, a decimal number D may be represented in terms of an *n*-digits SD number as

$$D = \sum_{j=0}^{n-1} b_i r^j \tag{1}$$

where b_i digit is selected from the set $\{-\alpha,\ \cdots, -1, 0, 1,\ \cdots, \alpha\}$ to produce the appropriate decimal representation. For trinary signed-digit (TSD) $r = 3$, the digit set is $\{\bar{2},\ \bar{1}, 0, 1, 2\}$; whereas for quaternary signed-digit (QSD) $r = 4$ and the digit set is $\{\bar{3},\ \bar{2},\ \bar{1}, 0, 1, 2, 3\}$. Here the digits $\bar{3}$, $\bar{2}$, and $\bar{1}$ denote -3, -2, and -1, respectively.

For radix ≥ 3, the addition operation of two SD numbers is performed in two successive steps because some digit combinations cause carry propagation to the next higher-order digit. The generation of a carry may be avoided by mapping the two SD digits in question into an intermediate sum and an intermediate carry (also known as weight and transfer digits) such that the *i-th* intermediate sum and the $(i-1)$-*th* intermediate carry when added generate no carry. The two-step addition is governed by the following equations:

$$\text{Step-one} \to X_i + Y_i = rT_{i+1} + W_i \tag{2}$$

$$\text{Step-two} \to S_i = T_i + W_i \tag{3}$$

where T_i and W_i represent the intermediate carry and sum, respectively, and S_i is the final carry-free sum. Further, subtraction of two SD numbers can be obtained by first complementing the subtrahend and then an addition operation is applied. Thus, the subtraction of two SD numbers involves three steps.
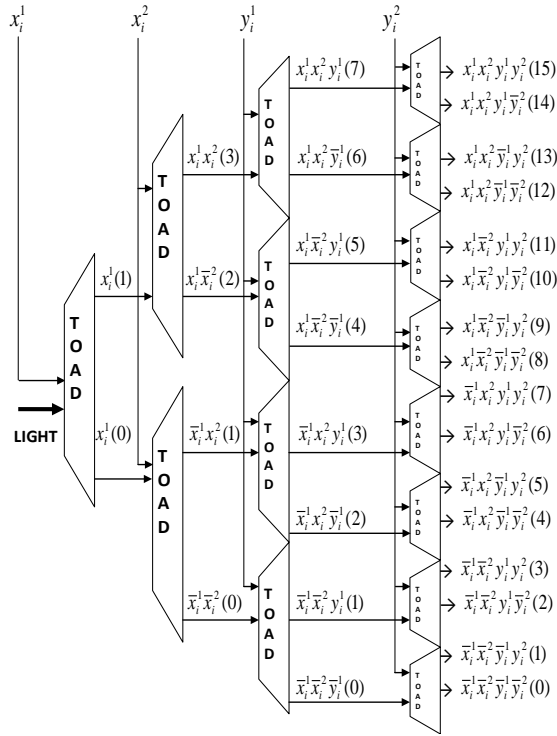
Figure 2. 1×16 TOAD based decoder.

The totally-parallel adder for SD number representation is shown in **Figure 3** where the functional blocks **A** and **B** represent the computing rules generated from Equations (2) and (3), respectively.

For TSD and QSD numbers, all possible two SD numbers that satisfy Equations (2) and (3) above are listed in **Table 1** and **Table 2**, respectively. Note that the SD numbers in these tables are grouped according to the value of the output digit. The pairs of the to-be-added trinary digits are first divided into nine groups (for the first step) as shown in the second column of Table 1a whereas the third column of the table shows the necessary interme-diate carry and intermediate sum digits for carry-free addition. **Table 1(b)** lists the rules for the second step of the addition. Thus, **Table 1(a)** and **Table 1(b)** represent the 25 and the 9 computational rules that are used in blocks **A** and **B** of **Figure 3** for the TSD addition. Notice that these tables include polarization encoding of the SD digits that will be explained in the next section.

Similarly, the pairs of the to-be-added quaternary digits are arranged into thirteen groups for the first step and seven groups for the second step as shown in **Table 2**.

4. Polarization-Encoded TOAD-Based TSD Adder Circuits

It was mentioned in the previous section that the TOAD-based decoder method can be used to implement any logical function expressed as sum-of-products. The variables of the minterms are the control signals of the de-coder. Now, since the TSD numbers $\{\bar{2}, \bar{1}, 0, 1, 2\}$ have five symbols, a three-bit intensity-encoding scheme (light, no light) is needed for each SD symbol to provide the control signals. Therefore, the addition of two SD numbers requires six control signals. Consequently, the design of the all-optical circuit requires 1×64 decoder with tens of TOAD switches. Obviously, this is not practical. As a solution to this limitation we propose using polarized state of light (vertical and horizontal) and a two-bit encoding scheme such that the TSD numbers $\{\bar{2}, \bar{1}, 0, 1, 2\}$ are encoded as $\{H0, 0H, 00, 0V, V0\}$, respectively. Further, recall that the light of the two inputs in a TOAD switch (the CP and the IP lights) must have different intensities, different wavelengths, or different light polarization states. Since we do not know the polarization state of the light representing the TSD number ahead of time, then we cannot feed this light signal to the decoder as a control signal. This difficulty can be solved by using polarization beam splitters in order to generate two polarization channels for each TSD digits. Therefore, a TSD digit X_i, which is decoded as $X_i = x_i^1 x_i^2$, is routed to polarization beam splitters (PBS) to produce

(a)

Group Number	Addend/Augend $x_i\, y_i\ \left(x_i^{1H}\, x_i^{2H}\, y_i^{1H}\, y_i^{2H}\quad x_i^{1V}\, x_i^{2V}\, y_i^{1V}\, y_i^{2V}\right)$	Intermediate Carry/Sum $T_{i+1} W_i$
G1	2 2 (0 0 0 0 V 0 V 0)	1 1 (V V)
G2	2 1 (0 0 0 0 V 0 0 V) 1 2 (0 0 0 0 0 V V 0)	1 0 (V 0)
G3	1 1 (0 0 0 0 0 V 0 V) 0 2 (0 0 0 0 0 0 V 0) 2 0 (0 0 0 0 V 0 0 0)	1 $\bar{1}$ (V H)
G4	0 1 (0 0 0 0 0 0 0 V) 1 0 (0 0 0 0 0 V 0 0) 2 $\bar{1}$ (0 0 0 H V 0 0 0) $\bar{1}$ 2 (0 H 0 0 0 0 V 0)	0 1 (0 V)
G5	0 0 (0 0 0 0 0 0 0 0) 1 $\bar{1}$ (0 0 0 H 0 V 0 0) $\bar{1}$ 1 (0 H 0 0 0 0 0 V) 2 $\bar{2}$ (0 0 H 0 V 0 0 0) $\bar{2}$ 2 (H 0 0 0 0 0 V 0)	0 0 (0 0)
G6	$\bar{2}$ 1 (H 0 0 0 0 0 0 V) 1 $\bar{2}$ (0 0 H 0 0 V 0 0) 0 $\bar{1}$ (0 0 0 H 0 0 0 0) $\bar{1}$ 0 (0 H 0 0 0 0 0 0)	0 $\bar{1}$ (0 H)
G7	$\bar{1}$ $\bar{1}$ (0 H 0 H 0 0 0 0) 0 $\bar{2}$ (0 0 H 0 0 0 0 0) $\bar{2}$ 0 (H 0 0 0 0 0 0 0)	$\bar{1}$ 1 (H V)
G8	$\bar{1}$ $\bar{2}$ (0 H H 0 0 0 0 0) $\bar{2}$ $\bar{1}$ (H 0 0 H 0 0 0 0)	$\bar{1}$ 0 (H 0)
G9	$\bar{2}$ $\bar{2}$ (H 0 H 0 0 0 0 0)	$\bar{1}$ $\bar{1}$ (H H)

(b)

Group Number	Intermediate Carry/Sum $T_i W_i\left(T_i^{H}\, T_i^{V}\, W_i^{H}\, W_i^{V}\right)$	Final Sum $S_i\left(S_i^{1}\, S_i^{2}\right)$
G1	1 1 (0V0V)	2 (V 0)
G2	0 1 (000V) 1 0 (0V00)	1 (0 V)
G3	0 0 (0000) 1 $\bar{1}$ (0VH0) $\bar{1}$ 1 (H00V)	0 (0 0)
G4	0 $\bar{1}$ (00H0) $\bar{1}$ 0 (H000)	$\bar{1}$ (0 H)
G5	$\bar{1}$ $\bar{1}$ (H0H0)	$\bar{2}$ (H 0)

$X_i = x_i^{1H}\, x_i^{2H}\, x_i^{1V}\, x_i^{2V}$ as shown in **Figure 4**. This encoding scheme is used for the addend and the augend for the TSD numbers in **Table 1** and **Table 2**. Further, whenever the intermediate carry or the intermediate sum digit in the adder belongs to the set $\{\bar{1}, 0, 1\}$, one-bit encoding such as $\{H, 0, V\}$ is used in the encoding scheme.

Table 2. (a) Truth table and polarization-encoding for the first step QSD addition; (b) Truth table and polarization-encoding for the second step QSD addition.

(a)

Group Number	Addend/Augend $x_i y_i$ $\left(x_i^{1H} x_i^{2H} y_i^{1H} y_i^{2H}\quad x_i^{1V} x_i^{2V} y_i^{1V} y_i^{2V}\right)$		Intermediate Carry/Sum $T_{i+1} W_i$ $\left(t_{i+1} w_i^{1V} w_i^{2V} w_i^{1H} w_i^{2H}\right)$	
G1	3 3	(0 0 0 0 V V V V)	1 2	(V V 0 0 0)
G2	2 3	(0 0 0 0 V 0 V V)	1 1	(V 0 V 0 0)
	3 2	(0 0 0 0 V V V 0)		
G3	3 1	(0 0 0 0 V V 0 V)	1 0	(V 0 0 0 0)
	1 3	(0 0 0 0 0 V V V)		
	2 2	(0 0 0 0 V 0 V 0)		
G4	2 1	(0 0 0 0 V 0 0 V)	1 $\bar{1}$	(V 0 0 0 H)
	1 2	(0 0 0 0 0 V V 0)		
	0 3	(0 0 0 0 0 0 V V)		
	3 0	(0 0 0 0 V V 0 0)		
G5	1 1	(0 0 0 0 0 V 0 V)	0 2	(0 V 0 0 0)
	0 2	(0 0 0 0 0 0 V 0)		
	2 0	(0 0 0 0 V 0 0 0)		
	3 $\bar{1}$	(0 0 0 H V V 0 0)		
	$\bar{1}$ 3	(0 H 0 0 0 0 V V)		
G6	0 1	(0 0 0 0 0 0 0 V)	0 1	(0 0 V 0 0)
	1 0	(0 0 0 0 0 V 0 0)		
	2 $\bar{1}$	(0 0 0 H V 0 0 0)		
	$\bar{1}$ 2	(0 H 0 0 0 0 V 0)		
	3 $\bar{2}$	(0 0 H 0 V V 0 0)		
	$\bar{2}$ 3	(H 0 0 0 0 0 V V)		
G7	0 0	(0 0 0 0 0 0 0 0)	0 0	(0 0 0 0 0)
	1 $\bar{1}$	(0 0 0 H 0 V 0 0)		
	$\bar{1}$ 1	(0 H 0 0 0 0 0 V)		
	2 $\bar{2}$	(0 0 H 0 V 0 0 0)		
	$\bar{2}$ 2	(H 0 0 0 0 0 V 0)		
	$\bar{3}$ 3	(H H 0 0 0 0 V V)		
	3 $\bar{3}$	(0 0 H H V V 0 0)		
G8	0 $\bar{1}$	(0 0 0 H 0 0 0 0)	0 $\bar{1}$	(0 0 0 0 H)
	$\bar{1}$ 0	(0 H 0 0 0 0 0 0)		
	$\bar{2}$ 1	(H 0 0 0 0 0 0 V)		
	1 $\bar{2}$	(0 0 H 0 0 V 0 0)		
	$\bar{3}$ 2	(H H 0 0 0 0 V 0)		
	2 $\bar{3}$	(0 0 H H V 0 0 0)		
G9	$\bar{1}$ $\bar{1}$	(0 H 0 H 0 0 0 0)	0 $\bar{2}$	(0 0 0 H 0)
	0 $\bar{2}$	(0 0 H 0 0 0 0 0)		
	$\bar{2}$ 0	(H 0 0 0 0 0 0 0)		
	$\bar{3}$ 1	(H H 0 0 0 0 0 V)		
	1 $\bar{3}$	(0 0 H H 0 V 0 0)		
G10	$\bar{1}$ $\bar{2}$	(0 H H 0 0 0 0 0)	$\bar{1}$ 1	(H 0 V 0 0)
	$\bar{2}$ $\bar{1}$	(H 0 0 H 0 0 0 0)		
	$\bar{3}$ 0	(H H 0 0 0 0 0 0)		
	0 $\bar{3}$	(0 0 H H 0 0 0 0)		
G11	$\bar{3}\bar{1}$	(H H 0 H 0 0 0 0)	$\bar{1}$ 0	(H 0 0 0 0)
	$\bar{1}$ $\bar{3}$	(0 H H H 0 0 0 0)		
	$\bar{2}$ $\bar{2}$	(H 0 H 0 0 0 0 0)		
G12	$\bar{3}$ $\bar{2}$	(H H H 0 0 0 0 0)	$\bar{1}$ $\bar{1}$	(H 0 0 0 H)
	$\bar{2}$ $\bar{3}$	(H 0 H H 0 0 0 0)		
G13	$\bar{3}$ $\bar{3}$	(H H H H 0 0 0 0)	$\bar{1}$ $\bar{2}$	(H 0 0 H 0)

(b)

Group Number	Intermediate Carry/Sum $T_i\,W_i\ \left(T_i^H T_i^V\, w_i^{1V}\, w_i^{2V}\, w_i^{1H}\, w_i^{2H}\right)$	Final Sum $S_i\left(S_i^1 S_i^2\right)$
G1	1 2 (0 V V 0 0 0)	3 (V V)
G2	1 1 (0 V 0 V 0 0)	2 (V 0)
G3	0 1 (0 0 0 V 0 0) 1 0 (0 V 0 0 0 0)	1 (0 V)
G4	0 0 (0 0 0 0 0 0) 1 $\bar{1}$ (0 V 0 0 0 H) $\bar{1}$ 1 (H 0 0 V 0 0)	0 (0 0)
G5	0 $\bar{1}$ (0 0 0 0 0 H) $\bar{1}$ 0 (H 0 0 0 0 0)	$\bar{1}$ (0 H)
G6	$\bar{1}$ $\bar{1}$ (H 0 0 0 0 H)	$\bar{2}$ (H 0)
G7	$\bar{1}$ $\bar{2}$ (H 0 0 0 H 0)	$\bar{3}$ (H H)
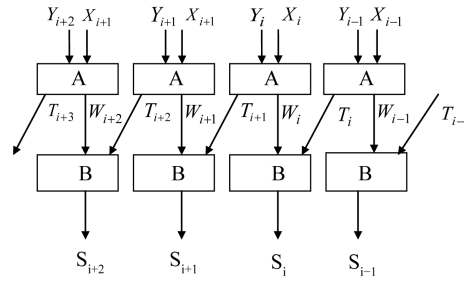
Figure 3. The two-step multiple-valued SD addition scheme.
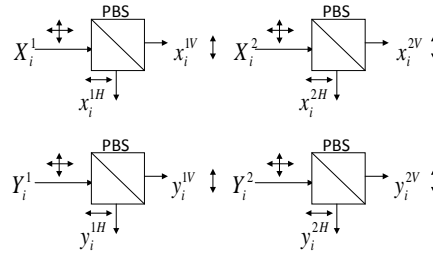
Figure 4. Two-bit polarization-encoding of the multiple-valued SD digits.

4.1. TSD: DESIGN1

The TSD addition is a two-step process where the first step generates an intermediate transfer T_{i+1} digit and an intermediate weight W_i digit that do not have the symbols $\bar{2}$ and 2; whereas the second step adds the digits T_i and W_i to produce the final sum. **Table 1** lists the <*H*, *V*> polarization-encoding of the two-step TSD addition. Studying **Table 1(a)** reveals that the minterms can be divided into three parts: (i) one group of minterms (the first eight entries) that have only *V* symbols; (ii) s second group of minterms (entries eighteen to twenty five) that have only *H* symbols; and (iii) a third group of minterms that have mixed *V* and *H* symbols. Therefore, a straight forward design method is to construct three channels or circuits to combine these minterms and produce the corresponding $T_{i+1}W_i$ digit outputs using the 1×16 decoder as the basic building block. **Figure 5** illustrates this design method for the TSD adder based on this minterms grouping. **Figure 5(a)** and **Figure 5(b)** illustrate the *V*-channel and the *H*-channel circuits, respectively; while the circuit in **Figure 5(c)** takes some outputs of the *V*- and the *H*-channel and combine them in order to produce the corresponding $T_{i+1}W_i$ digits. Note that the output of the 1×16 decoders in these circuits are denoted by numbers in parentheses with a superscript letter
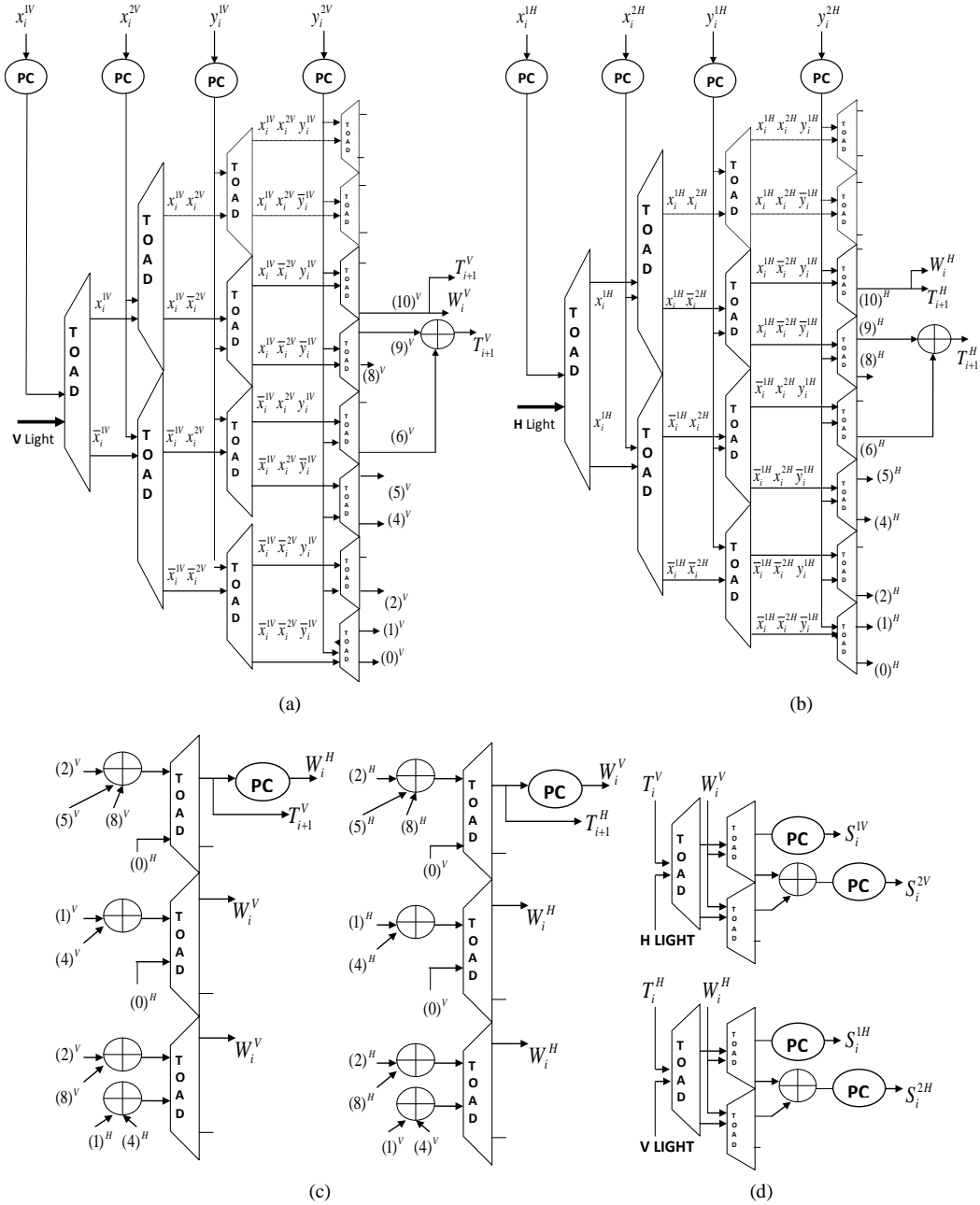
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Figure 5. Designed circuits of the TSD adder: DESIGN1: (a) Step 1 *V*-channel circuit; (b) Step 1 *H*-channel; (c) Step 1 *HV-*channel circuit; and (d) Step 2 circuit.

representing the polarization state. **Figure 5(d)** represents the designed circuit for the second step (**Table 1(b)**) of the adder that generates the sum digits. In this figure, a simplified 1×4 decoder is used. This adder design requires only 36 switches and it takes seven gate delay units for the addition. Note that this is a non-minimized TSD adder design, which can be improved by reducing both the numbers of TOAD switches and the delay units. Further, polarization converters (PC) are used before the control signals and continuous light sources are needed for the circuit to work properly.

4.2. TSD DESIGN2

This subsection demonstrates a second design method for the TSD adder which is not based on the 1×16

TOAD decoder. When a closer look at the polarization-encoded TSD digits of **Table 1(a)** is carried out, it is observed that when the signals (x_i^{1H}, x_i^{2H}, y_i^{1H}, y_i^{2H}) are combined and produced no light output, then this indicates the *V*-channel entries in the table. In a similar way, the signals (x_i^{1V}, x_i^{2V}, y_i^{1V}, y_i^{2V}) indicate the *H*-channel entries of the truth table. Now, the combined signals of (x_i^{1V}, x_i^{2V}, y_i^{1V}, y_i^{2V}) can be used as *IP* input and the combined signals (x_i^{1H}, x_i^{2H}, y_i^{1H}, y_i^{2H}) can be used as *CP* input in one TOAD switch; while they can be used as *CP* and *IP* inputs in a second TOAD switch as illustrated in **Figure 6(a)** and **Figure 6(b)**. This same method is used to distinguish the mix polarization channel as shown in **Figure 6(c)**.
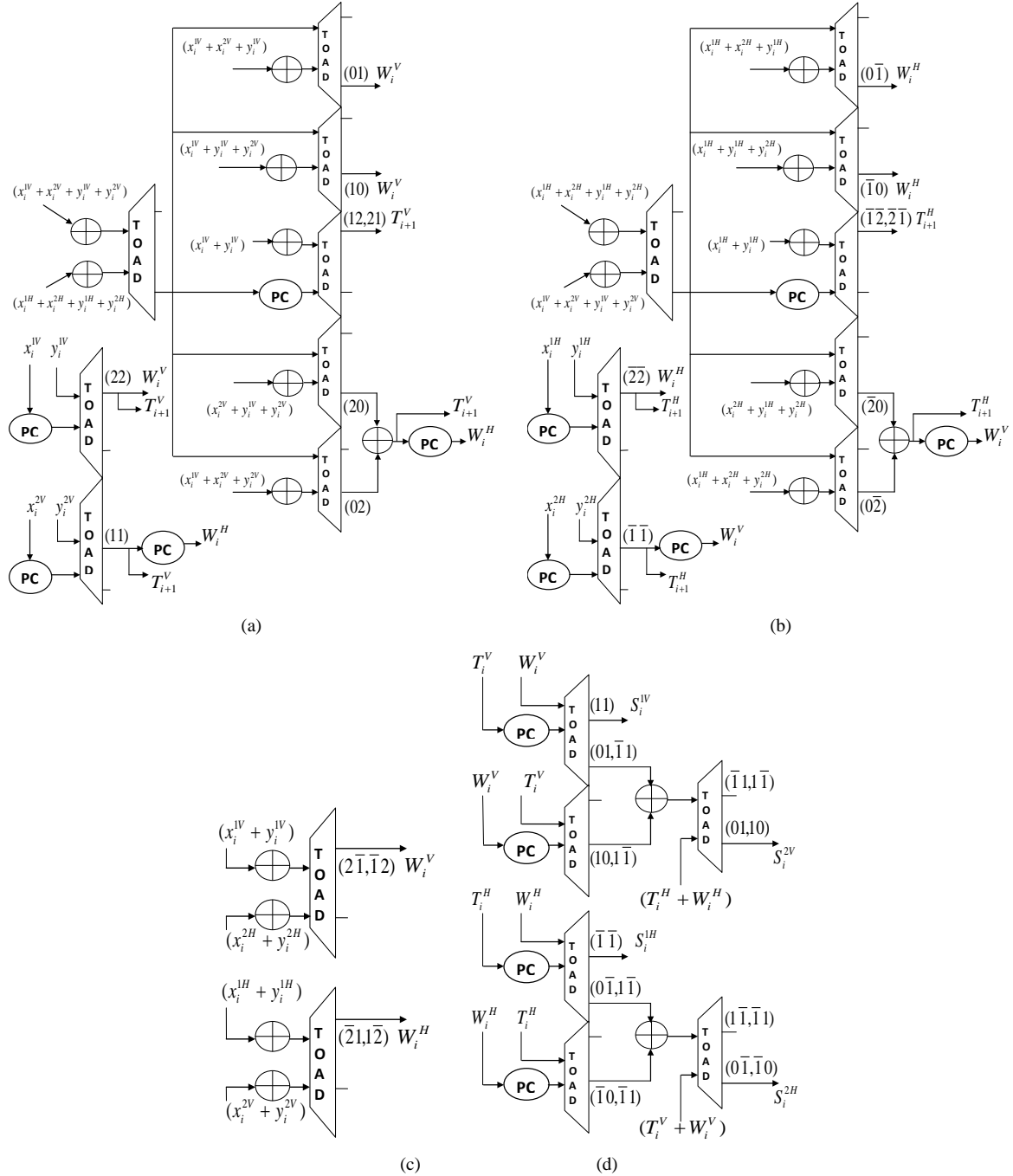

Figure 6. Designed circuits of the TSD adder: DESIGN2: (a) Step 1 *V*-channel circuit; (b) Step 1 *H*-channel; (c) Step 1 *HV*-channel circuit; and (d) Step 2 circuit.

On the other hand, the second step of the TSD adder is redesigned in order to eliminate the continuous *H*- and *V*-light sources in the circuits and at the same time maintain the same numbers of TOAD switches and the delay units as demonstrated in **Figure 6(d)**. Furthermore, to clarify the generated outputs of each TOAD switch in the circuit, we posted the corresponding minterms at the output ports. This design method resulted in a better and a faster adder than DESIGN1. Thus, DESIGN2 requires only 24 gates and it takes only four gate delay units for the addition. Note that this design needs more beam combiners.

4.3. TSD DESIGN3

This proposed design method avoids using the 1×16 TOAD decoder, the polarization beam splitters that generate the *H*- and the *V*-channels, and the continuous *H*- and *V*-light sources. The TSD numbers $\{\bar{2}, \bar{1}, 0, 1, 2\}$ are encoded by two digits $X_i = x_i^1 x_i^2$ as $\{H0, 0H, 00, 0V, V0\}$. This imposes on the designer to carefully consider the state polarizations of both the control and the incoming pulse signals (*CP* and *IP*) for every possible combination digits of the TSD adder. In this regard, every signal in the TOAD switch (being an input or an output signal) has a trinary representation *i.e.* the signal can have vertically polarized, horizontally polarized, or no light. Exhaustive considerations of x_i^1, x_i^2, y_i^1, y_i^2 or any combinations of these digits as being either *CP* or *IP* inputs along with polarization conversion, lead to DESIGN3 as shown in **Figure 7**. Again in this figure, the minterms of the adder of **Table 1** are posted at the outputs of every TOAD switch. A huge improvement is achieved in this design since the number of gates is reduced by 70% to 11 and the delay is reduced by 72% to 2 units.

5. Polarization-Encoded TOAD-Based QSD Adder Circuits

The quaternary literals $\{\bar{3}, \bar{2}, \bar{1}, 0, 1, 2, 3\}$ need a three-bit intensity encoding (light, no light encoding) for each signed-digit representation. However, a two-bit scheme is sufficient to represent the seven symbols when polarization-encoding is used such as $\{\bar{3} = HH, \bar{2} = H0, \bar{1} = 0H, 0 = 00, 1 = 0V, 2 = V0, 3 = VV\ HH\}$. In a similar manner to the TSD adder, the QSD addition is a two-step process where the first step generates an intermediate transfer T_{i+1} digit that belongs to the set $\{\bar{1}, 0, 1\}$ and an intermediate weights W_i digit that belongs to the set $\{\bar{2}, \bar{1}, 0, 1, 2\}$; whereas the second step adds the digits T_i and W_i to produce the final sum. Therefore, a single polarized bit can be used to represent the transfer digits T_{i+1} while two polarized-bit are needed to represent the weight digits W_i.
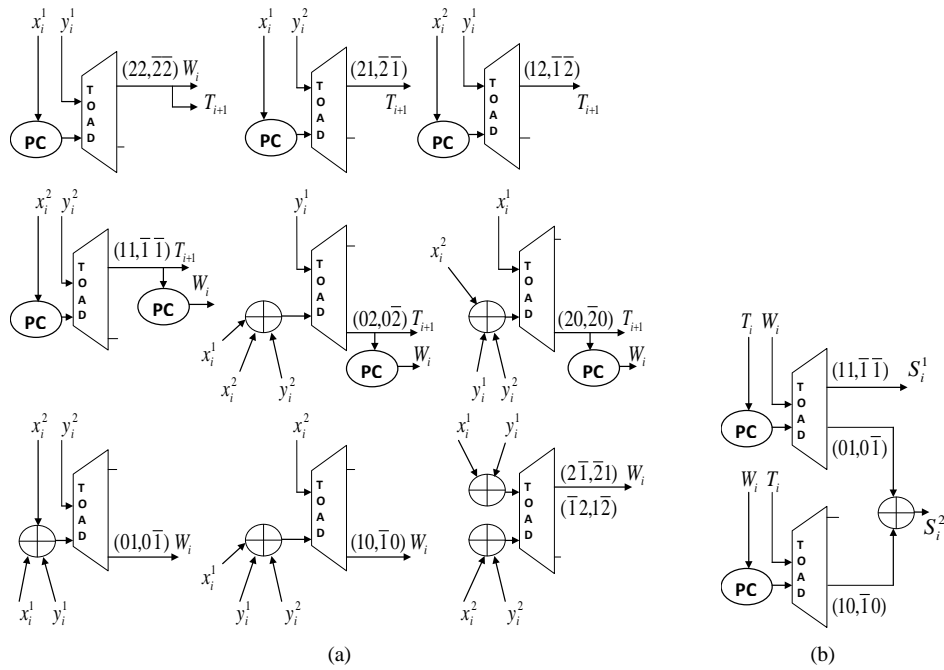

Figure 7. Designed circuits of the TSD adder: DESIGN3: (a) Step 1 circuit; (b) Step 2 circuit.

5.1. QSD DESIGN1

This design uses the same approach as for DESIGN1 of the TSD adder where the 1×16 TOAD decoder constitutes the core part of the design. In this regard, polarization beam splitters are needed to generate the appropriate polarized *CP*. **Table 2** lists the *<H,V>* polarization encoding of the two-step QSD addition. Again, the entries in the table are classified as three groups that have only *V* symbols, only *H* symbols, and mixed *HV* symbols. Accordingly, the adder is designed in a straight forward manner and divided into three channels. The combinations of output digits of these channels will produce the appropriate sum. **Figure 8** illustrates the circuits for this QSD adder. As it is expected, the circuit is more complicated having 54 TOAD switches and it takes eight gate delay units for the addition.

5.2. QSD DESIGN2

It can be shown that by following a similar procedure to that of DESIGN2 of the TSD adder of the previous section, a better and reduced number of gate count for the QSD adder can be obtained. However, in this subsection we will provide a much better QSD adder, which follows the design method used in DESIGN3 of the TSD adder. **Figure 9** presents this design where the nonzero outputs of the minterms (the entries in **Table 2**) are realized individually and they are shown at the output ports of the TOAD switches. To illustrate the working mechanisms of this design, let us consider generating the output for the minterms $3\bar{1}$, which is encoded as $x_i^1 x_i^2 y_i^1 y_i^2 = VV0H$. This minterms is obtained using the circuit in the upper left corner in **Figure 9(a)**. The input light to TOAD1 is $y_i^2 = H$ and the control signal is $\left(x_i^2 + y_i^1\right) = V$. Thus the upper port of TOAD1 will have *H*-light and it is used as input signal to TOAD2. Since the control signal of TOAD2 is $x_i^1 = V$, then the upper port of TOAD2 will have *H*-light, which is polarization converted to generate *V*-light as it is required. In a similar way, we can obtain the output of the minterm $\bar{3}1$. This QSD adder is denoted as DESIGN2 where the size is reduced by one half and the speed is increased by a factor of two compared to QSD DESIGN1 adder. The designed circuit requires only 27 gates and it takes four gate delay units for the addition.

6. Conclusions

In this paper, designs of ultra-fast all-optical TOAD-based adders for multiple-valued SD numbers are reported.
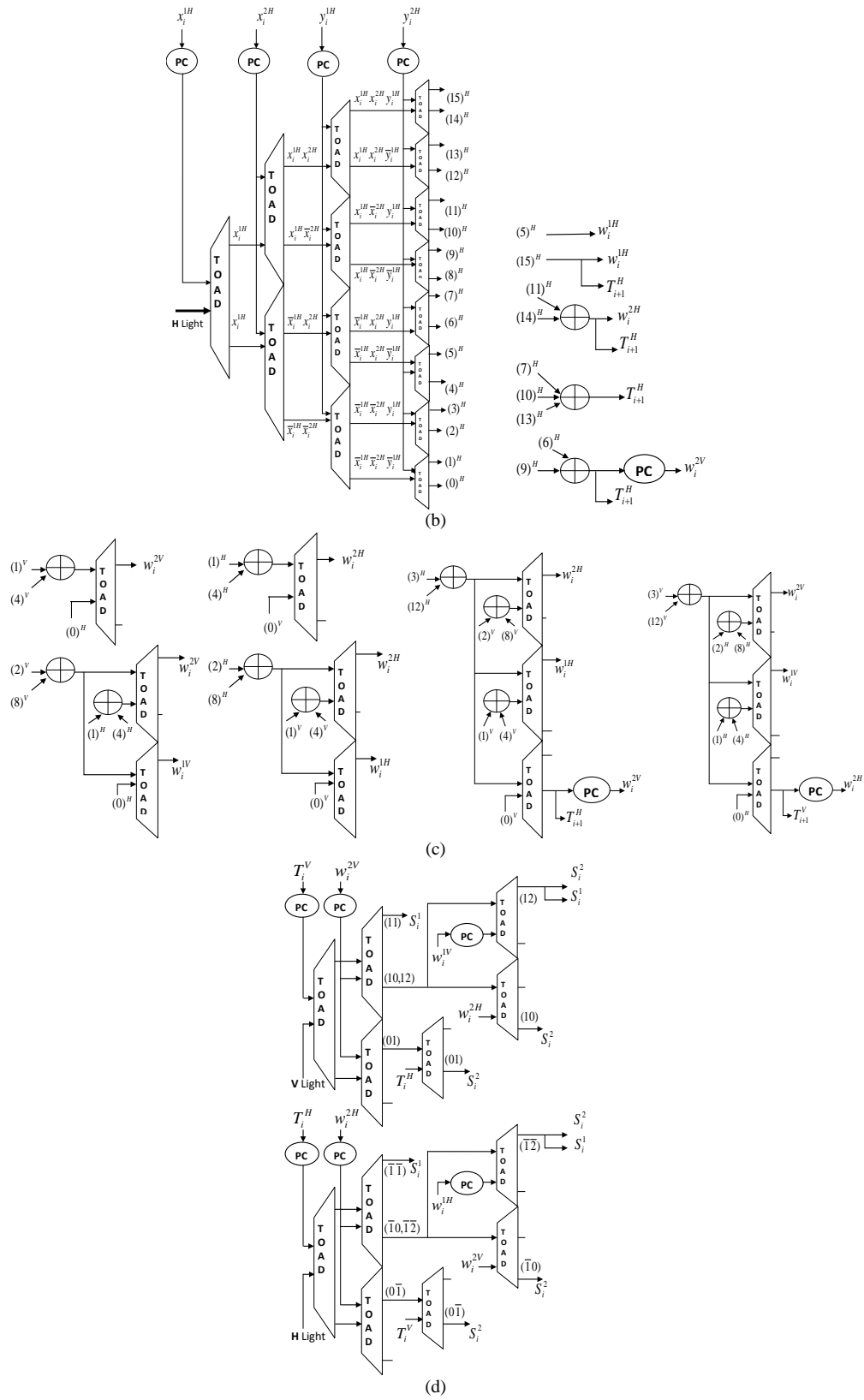

(a)
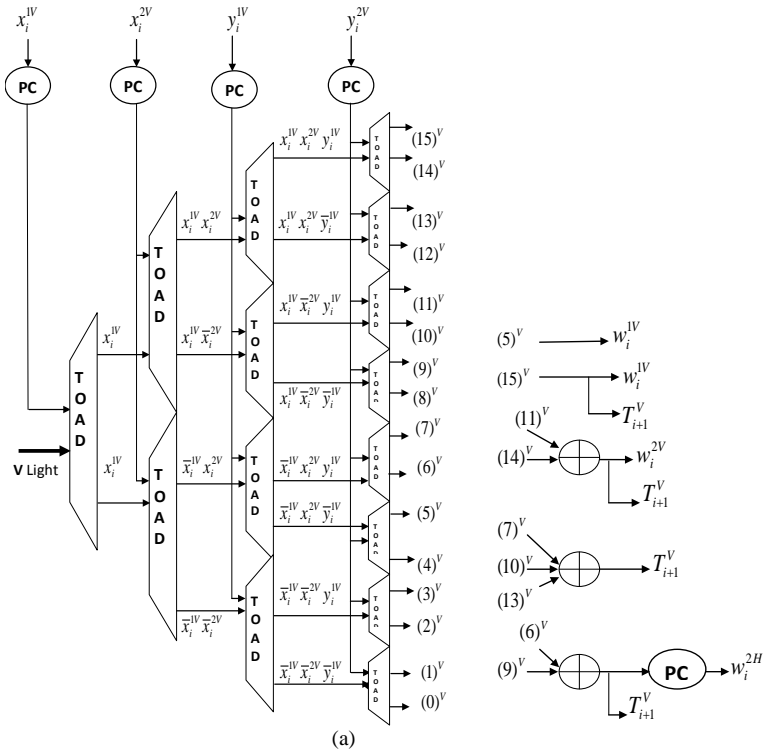
Figure 8. Designed circuits of the QSD adder: DESIGN1: (a) Step 1 *V*-channel circuit; (b) Step 1 *H*-channel circuit; (c) Step 1 *HV-*channel circuit; and (d) Step 2 circuit.
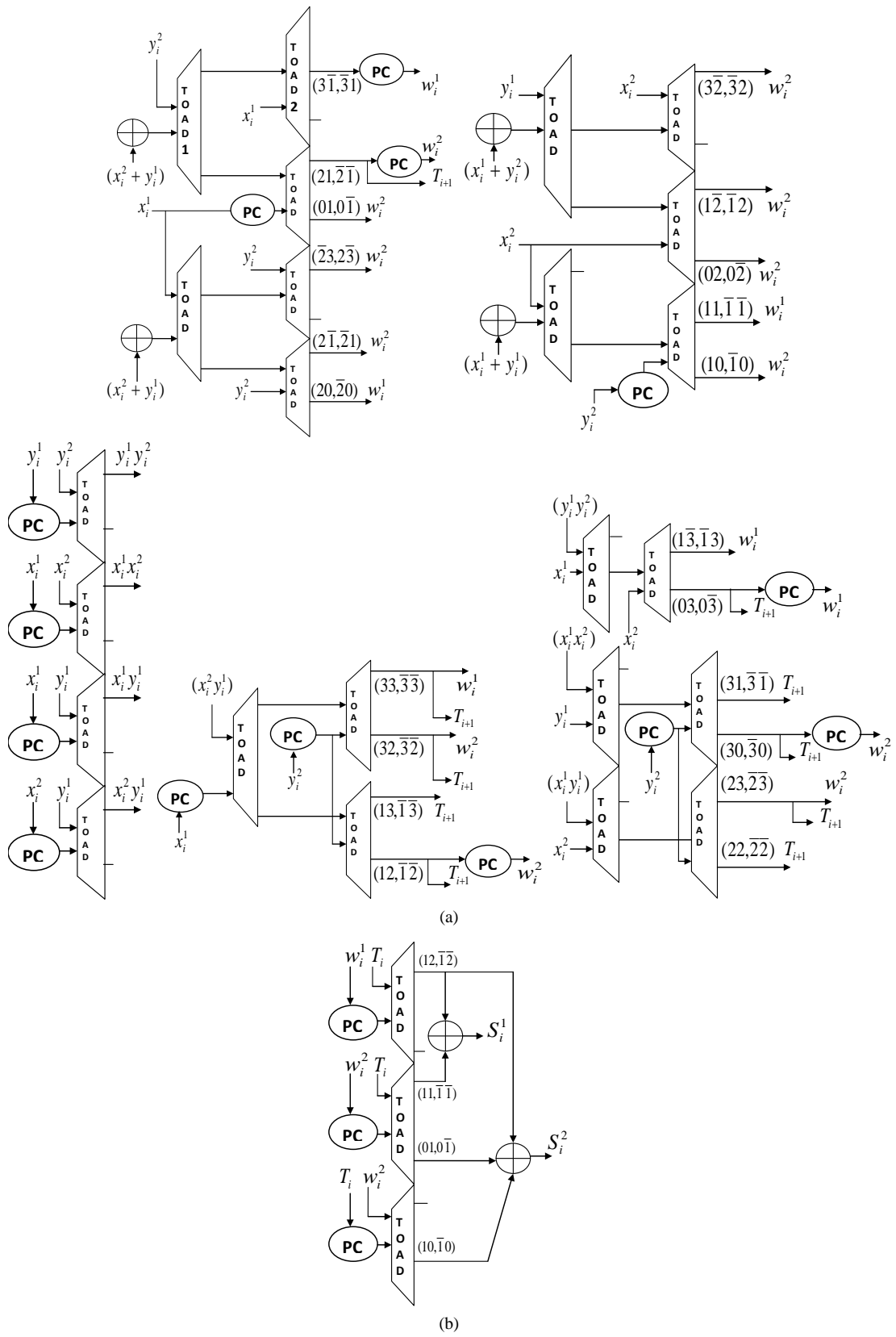
(a)

(b)

Figure 9. Designed circuits of the QSD adder: DESIGN2: (a) Step 1 circuit and (b) Step 2 circuit.

Table 3. Comparison between the multiple valued SD circuit designs.

Adder		Unit delay	Gates count	Beam combiners	Polarization converters
TSD	DESIGN1	7	36	14	14
	DESIGN2	4	24	26	12
	DESIGN3	2	11	9	9
QSD	DESIGN1	8	54	20	18
	DESIGN2	4	27	8	17
MSD	DESIGN2	4	10	11	7

These adders can be used as subtracters units once the augends are complemented and used as input digits to the designed adders. Three TSD (two QSD) circuits are designed and demonstrated. **Table 3** summarizes the design elements of the proposed TSD and QSD adders as well as the most recently proposed MSD adder [24]. From this table, we can see that the QSD adder (DESIGN2) has the same speed (unit delay) as for the MSD adder while the gates count is higher as expected. Thus, this makes the proposed QSD adder an attractive circuit candidate knowing that the QSD number system (7 literals) provides more transmission information and more storage density than the MSD number system (3 literals).

On the other hand, the TSD adder (DESIGN3) is two times faster than both the QSD and the MSD counterparts. While the TSD gates count is almost the same as for the MSD adder and about 60% less than the QSD adder. Consequently, these results make the TSD adder very attractive and a good candidate for future considerations in digital optical computing.

It is worth mentioning that the previous proposed designs are theoretical. However, many theoretical simulations of similar TOAD-based circuits that prove their feasibilities were reported [25]-[28]. In addition, many reported works using TOAD switches demonstrated results with simulations using practical parameters or results from laboratories experimental data. Furthermore, note that when implementing multistage interconnection circuits using TOADs as the basic switch, one has to be aware of many practical issues such as synchronization and cascadability in addition to light intensity losses due to splitters/combiners, polarization, pulse duration, noise and others related issues [29]-[33].

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