

Behavioral Modeling and Simulation of Cascade Multibit $\Sigma\Delta$ Modulator for Multistandard Radio Receiver

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ABSTRACT

In this paper, a cascade Sigma-Delta ($\Sigma\Delta$) Analog to Digital Converter (ADC) for multistandard radio receiver was presented. This converter is supposed to be able to support GSM, UMTS, Wifi and WiMAX communication standards. The Sigma-Delta modulator makes use of 4 bit quantizer and Data-Weighted-Averaging (DWA) technique to attain high linearity over a wide bandwidth. A top-down design methodology was adopted to provide a reliable tool for the design of reconfigurable high-speed $\Sigma\Delta$ s. VHDL-AMS language was used to model the analog and mixed parts of the selected 2-1-1 cascade $\Sigma\Delta$ converter and to verify their reconfiguration parameters based on behavioural simulation. This multistandard architecture was high level sized to adapt the modulator performance to the different standards requirements. The effects of circuit non-idealities on the modulator performance were modeled and analyzed in VHDL-AMS to extract the required circuit parameters.

Keywords: $\Delta\Sigma$ ADC; Multistandard; VHDL-AMS Language; Behavioural Simulation

1. Introduction

The most significant design challenge in current and future wireless devices is to support several wireless and cellular standards in the same handheld device. The goal was to design multistandard RF terminals that are very flexible and reconfigurable with neither a decrease in the circuit performance nor an increase in power consumption or silicon area [1-4]. A high resolution high speed ADC will only allow the shifting of several RF and analog processing to the digital domain in order to provide more flexibility and increase the design complexity [5]. The use of $\Delta\Sigma$ modulators in multistandard receivers is suitable for several reasons among which we can cite, firstly, that $\Sigma\Delta$ modulators are very linear and are also less sensitive to circuit non-idealities than other types of data converters [6]. Secondly, the noise shaping and the oversampling performed by $\Sigma\Delta$ modulators allow to achieve high Dynamic Range (DR) for narrow bandwidths and lower DR for higher bandwidths. This characteristic is coherent with wireless standards requirements and their RF specifications which makes $\Sigma\Delta$ ADC suitable to perform the Analog/Digital (A/D) conversion function in a multi-standard capable RF receiver [7]. Another important advantage of $\Sigma\Delta$ ADC is it consumes less power than full Nyquist ADCs [8]. In this paper, the reconfigurable $\Sigma\Delta$ was modelled to be designed for a

GSM/UMTS/WiFi/WiMAX radio receiver. **Figure 1** shows the adopted multistandard receiver architecture. The proposed architecture is a multistandard Zéro-IF receiver. It uses a multiband antenna, four RF filters for GSM/UMTS/WLAN/WiMAX selection, a multistandard low noise amplifier (LNA) and multistandard mixers for I and Q components. The A/D conversion is performed with multistandard anti Alias filter and multistandard $\Sigma\Delta$ Modulator ($\Sigma\Delta$ M). The digital processing is supported by a DSP circuit. Zero_IF architecture was chosen for its high level of integration, associated with excellent multistandard capabilities [9]. Contrary to several multistandard Zero-IF architectures proposed in literature which use channel selection in analog domain and use an automatic Gain Control (AGC) to decrease ADC dynamic requirement [10,11], in our selected multistandard receiver, channel selection is performed in the digital domain and a very high dynamic ADC is used to eliminate the need for AGC. It uses a multistandard oversampled $\Delta\Sigma$ M followed by a digital decimation filter as shown in **Figure 2**. This approach achieves a more programmable solution rather than an analog approach thereby, enabling such receivers to upgrade easy to multi-mode operation.

Digital channel select filtering can be made easily programmable by changing the filter coefficients in the decimation filter. However, the dynamic range of the ADC must also be made programmable to fit the RF specifica-

tions. Fortunately, Sigma-Delta modulators allow the designer to trade off bandwidth and dynamic range which make them suitable to perform the A/D conversion function in a multi-standard capable RF receiver. Relying on system specifications for various addressed RF communications standards and on chosen receiver characteristics, ADC specifications were established for each standard (Table 1).

The remaining of the paper is organized as follows: Section 2 shows the multistandard cascaded Sigma-Delta modulator architecture and discusses its reconfiguration. Section 3 describes the system level design of the proposed modulator using VHDL-AMS language. The simulation results modeling are presented in Section 4. Finally, we draw our conclusion in Section 5.

2. Reconfigurable $\Sigma\Delta$ Modulator Architecture

Given that reconfigurability must be considered to find out the optimal multistandard $\Sigma\Delta$ modulator architecture, the cascade $\Sigma\Delta$ ADC was selected as the best suited architecture (Figure 3) [12-14]. This fourth order cascade

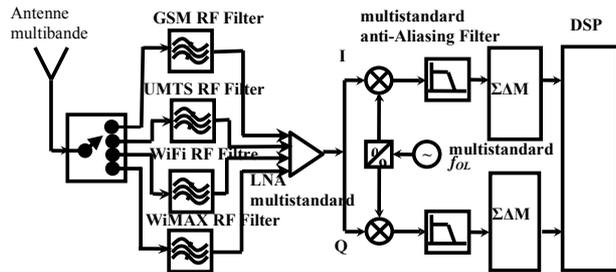


Figure 1. Proposed multistandard receiver architecture.

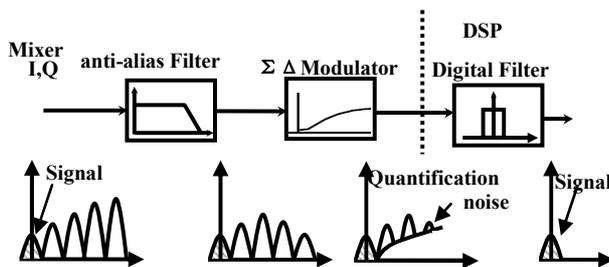


Figure 2. Channel selection with a $\Delta\Sigma$ M and digital filter.

Table 1. DR requirements in the multistandard receiver.

Standard	Channel Bandwidth	DR (dB)
GSM	200 KHz	90 - 108
UMTS	3.84 MHz	70 - 90
Wifi	20 MHz	60 - 70
WiMAX	20 MHz	50 - 65

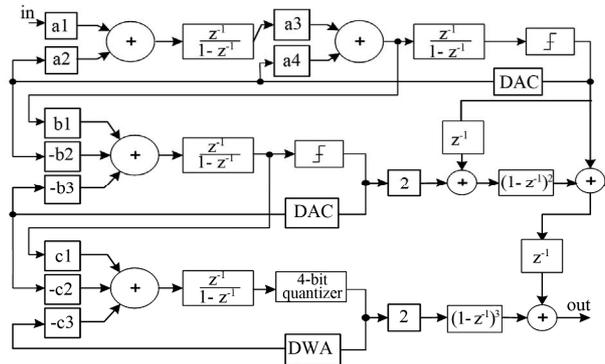


Figure 3. 2-1-1_{4bits} $\Delta\Sigma$ M linearized by DWA.

topology is a 2-1-1 architecture implemented using a cascade of second order sigma-delta loop and two first-order loops. The cascade architecture recombines the outputs of each stage in the digital domain to achieve fourth-order noise shaping. Inherently linear single-bit Digital/Analog (D/A) converters are employed in the first two stages while a four-level D/A converter is employed in the lower resolution third stage to improve the dynamic range. The proposed topology overcomes the influence of mismatch-induced errors in the multibit DAC on the 2-1-1 modulator performance of [15] by introducing a DEM algorithm; Data Weighted Averaging (DWA) to correct the DAC mismatch non-linearity. Based on [15], the coefficients were optimized in such a way that analog coefficients could be constructed with small integer ratios in order to achieve a compact layout and good matching in the switched-capacitor (SC) implementation. The value of the integrator weights are given in Table 2. The presented $\Sigma\Delta$ modulator provides a flexible solution to the support of a large variety of specifications. It is able to operate in three distinguishable modes as in the cases of GSM, UMTS and WLAN/WiMAX. It was considered that WLAN and WiMAX standards require the same ADC dynamic at the same bandwidth. Each mode consists of a $\Sigma\Delta$ topology and an over-sampling ratio (OSR) as shown in Table 3. A three order cascaded single bit 2-1 $\Sigma\Delta$ M has been selected as the two first stages in order to meet the specifications of the GSM mode. The unused block in the third stage is switched off while working in the GSM mode, taking into account the design considerations like power consumption. In all the others modes, the fourth order modulator 2-1-1_{4bits} cascaded is switched to operation by putting off the switch thus making it programmable. In the UMTS, this architecture operates at OSR of 16. In the WLAN/WiMAX mode, we use the same topology but at an OSR of 8. In order to validate its performance, the chosen multistandard topology was simulated using Simplorer schematic Software based on VHDL-AMS language. The obtained results are detailed in Table 3. Figure 4 presents the simulated Signal-to-Noise Ratio (SNR)

versus input signal amplitude, for GSM/UMTS/Wifi/WiMAX standards. Simulation results show a peak SNR of 107 dB in GSM mode, a peak SNR of 91 dB in UMTS mode, and a peak SNR of 68 dB in the Wifi/WiMAX mode. In Zero IF multiband GSM/UMTS/Wifi/WiMAX architecture, the ADC signal bandwidth is 100 KHz/1.92 MHz/10 MHz respectively.

3. $\Sigma\Delta$ Modulator Noise Modeling

The estimation effect of the non-ideality on the performance of the $\Sigma\Delta$ modulators is the main problem faced in their design. Since they have an inherent non-linearity of the modulator loop, the optimization of their performance must be done with behavioral time domain simulations. Needless to remind that the circuit level simulation is the most precise. Nevertheless, the evaluation of the effect of the circuit non-idealities and the optimization of the modulator's building blocks are quite difficult to execute because of the long simulation time required. An intermediate stage of behavioral simulations is therefore

Table 2. Coefficients Values.

a1	0.25	b2	0.5	d0	-2
a2	0.25	b3	0.5	d1	2
a3	1	c1	2	d2	0
a4	0.5	c2	1	d3	2
b1	1	c3	1		

Table 3. Performance of the multi-standard $\Sigma\Delta$ M.

Mode	Architecture	OSR	Band (MHz)	Sampling frequency	SNR _{max} (dB)
GSM	2-1	64	0.1	12.8 MHz	107
UMTS	2-1-1 _{4bit}	16	1.92	64 MHz	91
Wifi/WiMAX	2-1-1 _{4bit}	8	10	176 MHz	68

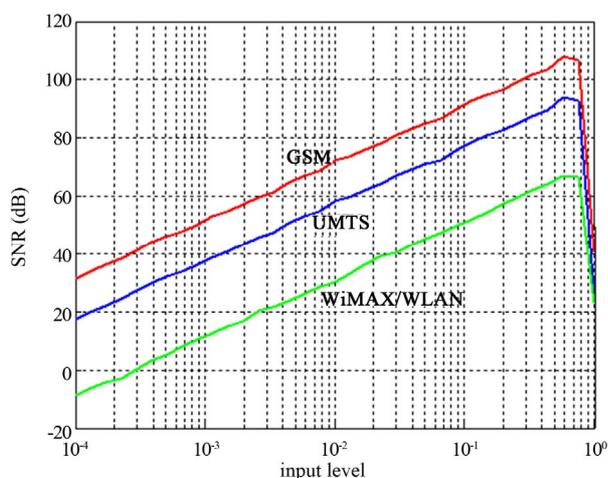


Figure 4. SNR as function of the input power.

necessary. Through multi-level abstraction models, VHDL-AMS enables us to overcome the problems. Besides, it allows a top-down design methodology. In fact, VHDL-AMS reduce simulation time and reflect circuit non-idealities phenomena through an efficient behavioral model. It also determines possible ranges of circuit specifications with reasonable design margins before the implementation of circuit components. Each block of the multistandard 2-1-1_{4bits} $\Sigma\Delta$ modulator was modeled using Simplorer schematic models. The obtained blocks were connected in Simplorer Software environment to obtain a behavioural description of the 2-1-1 multibit architecture. The previous simulation results assume the use of ideal components and only consider the quantization noise. Nevertheless, this is not the case in practice. Then, the behavioural approach has been used to investigate the overall circuit non-idealities effects, to optimize the system parameters and establish the specifications of the analog blocks. A description level using Simplorer schematic allowing parameter setting according to the non-idealities has been performed [16]. The main non-idealities considered in this paper are finite DC gain, slew rate and gain-bandwidth limitations, capacitor mismatch, KT/C noise, clock jitter and DAC capacitor mismatch.

3.1. Operational Transconductance Amplifier (OTA) parameters

The Switched Capacitor (SC) integrator is the most building block of $\Sigma\Delta$ converters and the OTA is the basic building block in a SC integrator. Therefore, behavioral simulations were carried out using VHDL-AMS environment in order to determine the specifications of the OTA for the different standards. The SC integrator model is developed using schematic level description as shown in **Figure 5**. Several non-idealities of the integrator have been included in the behavioral model: finite OTA DC gain, slew rate and gain bandwidth limitations. Using the behavioral simulations, the peak SNR was calculated as a function of each of the finite gain OTA, the gain bandwidth OTA and of slew rate OTA for the various modes. The results obtained are plotted in **Figures 6-8**, respectively. These VHDL-AMS Simulation results show that added to the proposed multistandard modulator which can tolerate an OTA dc gain of 60 dB, the OTA bandwidth needs to be at least 200 MHz and the slew rate at least 200 V/ μ s. These specifications have been used to select an appropriate OTA circuit topology that can meet the integrator performance requirements at minimum power dissipation. The fully differential folded cascade OTA, whose schematic is shown in **Figure 9**, has been chosen for the four integrators. This enabled us to reach the most suitable operating speed over power consumption ratio. The OTA parameters were set according to a design sample developed in [17]. The simulated param-

ters of the OTA are summarized in **Table 4** and reported on Simplorer OTA model.

3.2. Thermal Noise and Jitter Noise

In addition to noise from OTA, the thermal and jitter noises can also degrade the performance of the $\Sigma\Delta$ modulator. Thermal noise is mainly produced by the SC integrator finite switch resistance during the sampling and integration phases [18]. In a SC Sigma-Delta modulator, the sampling capacitor C_s is in series with a switch, which has a finite resistance R_{on} , that periodically opens.

Table 4. Proposed telescopic OTA performance.

Performance	Values
DC gain (dB)	78
GBW ($C_L = 2$ pF) (MHz)	306
Phase margin (degrees)	67
Slew rate (V/ μ s)	187
Power consumption (mW)	9.3
Process node/supply voltage (μ m/V)	0.35/ \pm 1.3

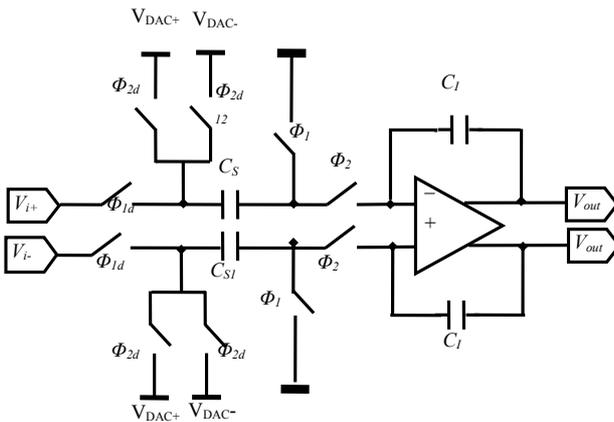


Figure 5. Switched capacitor integrator Simplorer model.

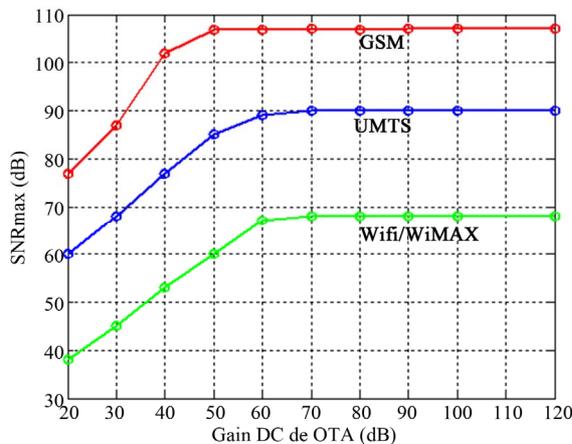


Figure 6. SNR versus OTA DC gain.

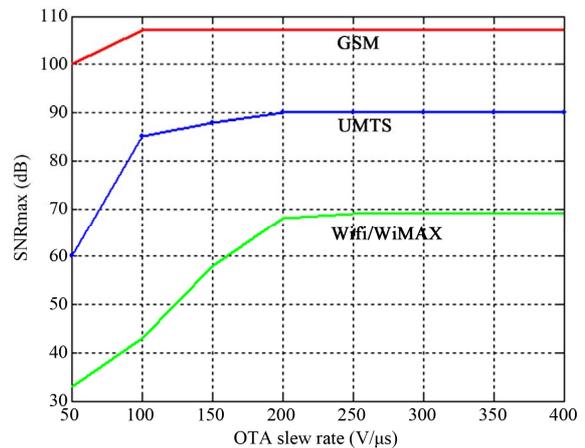


Figure 7. SNR versus OTA slew rate.

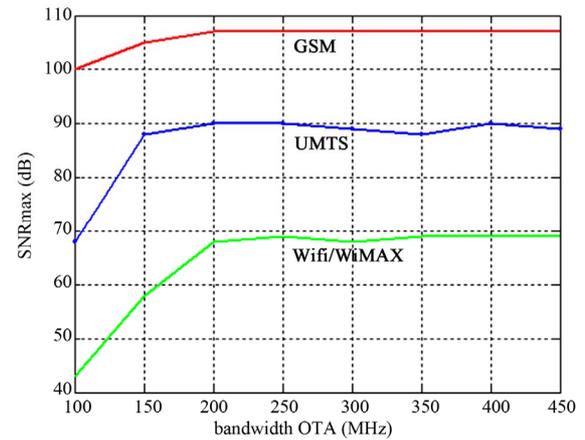


Figure 8. SNR versus OTA Bandwidth.

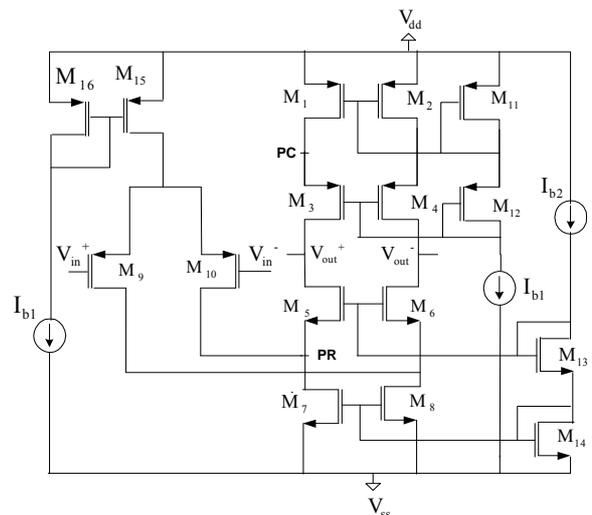


Figure 9. Fully differential folded cascode OTA topology.

Therefore it samples a noise voltage onto C_s . The total noise power can be calculate to evaluate the integral in Equation (1):

$$e_T^2 = \int_0^\alpha \frac{4KTR_{on}}{1 + (2\pi f R_{on} C_S)^2} df = \frac{KT}{C_S} \quad (1)$$

where K is the Boltzmann's constant, T the absolute temperature, and $4KTR_{on}$ the noise PSD associated with the switch on-resistance. The switch thermal noise voltage e_{Th} (usually called KT/C noise) appears as an additive noise to the input voltage $x(t)$ leading to:

$$\begin{aligned} y(t) &= [x(t) + e_r(t)]c = \left[x(t) + \sqrt{\frac{KT}{C_S}} n(t) \right] c \\ &= \left[x(t) + \sqrt{\frac{KT}{cC_i}} n(t) \right] c \end{aligned} \quad (2)$$

where $n(t)$ denotes a Gaussian random process with unity standard deviation, and c is the integrator gain and $c = C_s/C_i$. The behavior model of the switched thermal noise is shown in **Figure 10**. The clock jitter of an SC circuit can be defined as a short-term, non-cumulative variation of the switching instant of a digital clock from its ideal position in time. It produces a non-uniform sampling time sequence and results in an error that increases the total error power quantizer output. It should be noted that when the analog signal is sampled, the clock period variation doesn't have any direct effect on the performance of the circuit. Thus, the clock jitter is introduced only by the input signal sampling, and its effect on the $\Sigma\Delta$ modulator is independent of the modulator structure or order [19]. When a sinusoidal input signal $x(t)$ with amplitude Ax and frequency fx is sampled at an instant, which is in error by a statistical non-uniform uncertainty Δt , the magnitude of this error is given by:

$$e(nT_s + \Delta t) = x(nT_s + \Delta t) - x(nT_s) = \Delta t \frac{d}{dt} x(t) \Big|_{nT_s} \quad (3)$$

Thermal and jitter noises effects have been modeled with VHDL-AMS at the behavioral level as described in **Figure 10**. Where $x(t)$ is the input signal and $r(t)$ is a random noise signal implemented with a random block, which generates a sequence of random numbers with Gaussian distribution, zero mean, and unity standard deviation. Thermal noise, called also KT/C noise, is modeled as an additive white noise source of variance KT/C

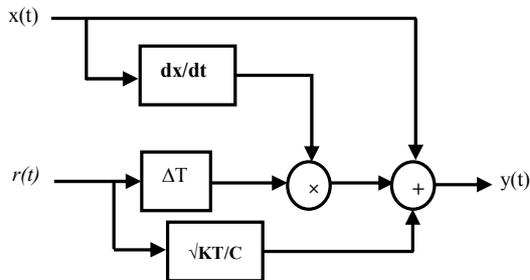


Figure 10. Thermal noise and jitter noise model.

to the input signal. Jitter noise, however, is included as an additive Gaussian random process with standard deviation ΔT [20,21]. The sampling and thermal noises effect is simulated at the system level for the largest bandwidth mode WLAN/WiMAX. As shown in **Figure 11**, such noises increase the inband noise floor, which seems to degrade the modulator performance. Such degradation is not significant in the presence of jitter noise $\Delta T < 10$ ps and thermal noise $C_s > 0.2$ pF as it was proved by several simulations. Actually the total SNR of the modulator is set to be almost unchanged when each of these noises is introduced into the modulator model.

3.3. Mismatch of the Capacitor Values

In SC integrators, the gain factors are implemented using capacitors ratios. Although fabrication process can produce matching and gains that differ from their nominal values affecting the performance of the integrator. Moreover, this capacitance mismatch alters the integrator transfer function, consequently affecting the signal and quantization noise [22]. In the behavioral model integrators we assume that the mismatch error of integrator weights (capacitors) has Gaussian distribution with Standard deviation "sigma". For the behavioral simulation results in **Figure 12**, a significant degradation of SNR can be caused by a sigma value up to 0.5%.

3.4. Mismatch in Multibit DAC

The four-bit DAC in the feedback of the last stage of our multistandard 2-1-1_{4bits} $\Sigma\Delta$ M can be built with 15 capacitors to determine the analog feedback signal. Due to process tolerances and variations, the values of these unit elements will deviate from the ideal weight C_u , resulting in errors in the DAC. The DWA was used to reduce the effect of such errors. Simulations were run for the UMTS

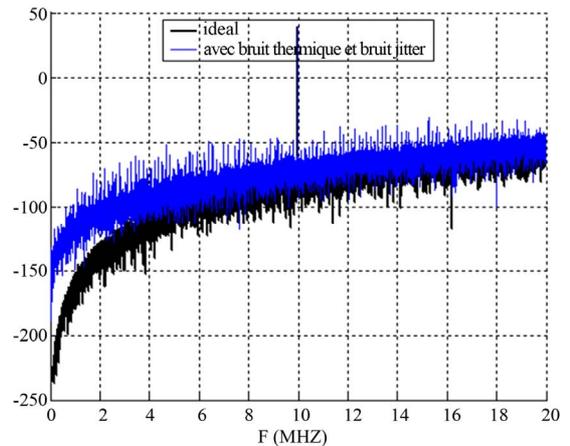


Figure 11. Power spectral density of 2-1-1_{4bits} $\Sigma\Delta$ modulator with an ideal modulator and addition of thermal noise and jitter noise model ($\Delta T = 200$ ps and $C_s = 0.1$ pF).

mode of the multistandard 2-1-1_{4bits} $\Sigma\Delta\text{M}$ including DAC Integral Non Linearity (INL) of 0.5% Full Scale (FS) and 1.0% FS when the DWA was inactive and active. **Figure 13** shows the PSD for the 2-1-1_{4bits} $\Sigma\Delta\text{M}$ in UMTS mode when the DAC error is 0.0%, 0.1% and 1.0% when the DWA is inactive and active, respectively. **Figure 14** shows how the DAC mismatch decreases significantly the SNR. Moreover, it is noticeable in the same figure how the DWA algorithm eliminated the SNR degradation.

4. Simulation Results

The chosen topology was simulated using Ansoft Simplorer Software to perform a system level simulation of the proposed architecture, verifying its performance and behavior when facing analog imperfections. Based on SIMPLORER models, it was possible to include several non-idealities, such as thermal noise, jitter noise, DC gain, finite bandwidth and slew rate. **Figure 15** shows

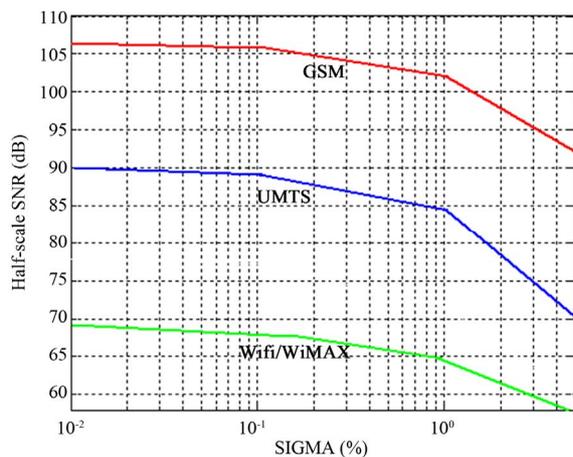


Figure 12. SNR versus capacitor mismatch.

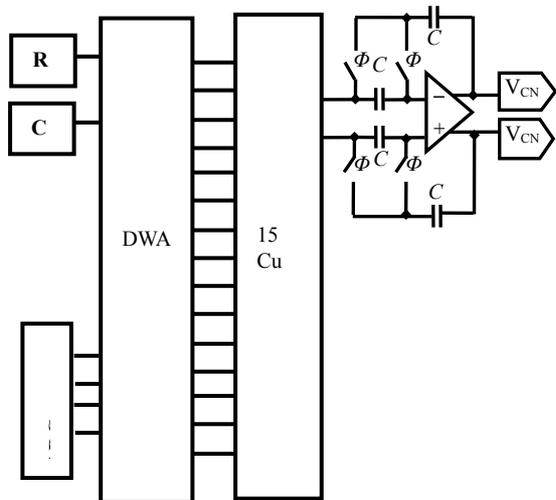


Figure 13. 4 bit DAC linearized with DWA model.

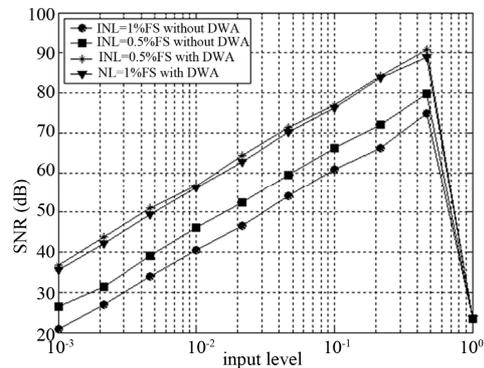
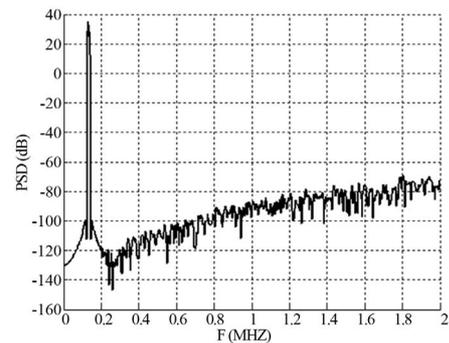
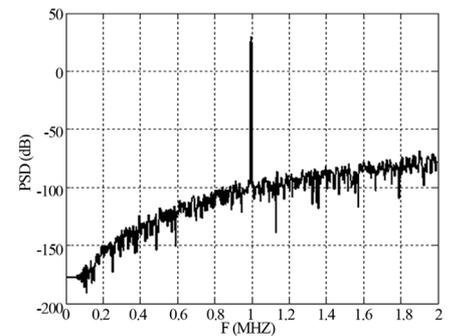


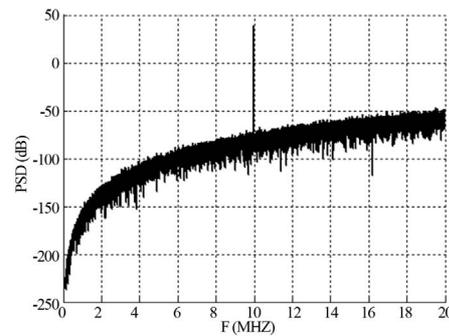
Figure 14. The SNR as function of the input power of the 2-1-1 $\Sigma\Delta\text{M}$ (UMTS mode) using a non-ideal DAC with and without DWA.



(a)



(b)



(c)

Figure 15. Power spectrum density for VHDL-AMS model validation in (a) GSM mode; (b) UMTS mode; (c) Wifi/WiMAX

the modulator output spectrum for GSM/UMTS/Wifi/WiMAX modes for a 0.1/1.92/10 MHz input signal at a sampling frequency of 12.8/64/176 MHz under the condition of 0.2% random capacitor mismatch, 0.5% DAC INL mismatch. Jitter and thermal noises are the other limitations assumed in this simulation with clock jitter of 10 ps and C_s equal to 0.25 pF. Taking into account the use of the real selected folded cascode OTA in the four integrators of the reconfigurable $\Sigma\Delta$, these simulation results show that a high linearity can be achieved thanks to the low-distortion of the Sigma-Delta modulator. Behavioral simulation results indicate that the proposed multistandard topology achieves a peak SNR of 105/98/65 dB for GSM/WCDMA/WLAN standards respectively in the presence of these circuit non-idealities.

5. Conclusion

The major contribution of this work is the development of an accurate behavioral model of multistandard $\Sigma\Delta$ for GSM/UMTS/Wifi/WiMAX zero-IF receiver using VHDL-AMS as the modeling language. It takes into account at the behavioural level most of SC $\Sigma\Delta$ modulator non-idealities, such as DAC non-linearity, OTA parameters (finite DC gain, finite bandwidth, slew rate), thermal noise and capacitor mismatch, thus it permits to obtain a good estimation of the $\Sigma\Delta$ modulator performance with a short simulation time. Future works would involve the implementation of the 2-1-1 cascade $\Sigma\Delta$ converter using device-level simulations.

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