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Simulation of Seven and Nine Level CHBMLI with Elliptical Phase Disposition PWM Technique

Chinmayi[1], B. G. Shivaleelavathi[2], Veeramma Yatnalli[2]

[1]Department of Electronics and Communication Engineering, Jyothy Institute of Technology, Bengaluru, Visvesvaraya Technological University, Belagavi, Karnataka, India
[2]Department of Electronics and Communication Engineering, JSS Academy of Technical Education, Bengaluru, Visvesvaraya Technological University, Belagavi, Karnataka, India
Email: shivaleelavathi@gmail.com

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Abstract

Electric vehicles are in demand in recent days due to depleting conventional energy resources. Electric vehicles which are environmental friendly are set to increase on road in coming days. The Electric vehicles which consist of electric drive systems are made up of electric motors, inverters and batteries. There is a need to increase their output quality while decreasing their size and cost. The multilevel inverter plays a vital role in improving the quality of the output voltage of the inverter. This paper presents the implementation of Elliptical Phase Disposition Pulse Width Modulation (EPD PWM) technique for higher level of Cascaded H-Bridge Multi Level Inverter (CHBMLI). The performance of 5, 7 and 9-level CHBMLI with proposed EPD PWM scheme is analyzed for three-phase RL-load. The simulation results prove that the voltage %THD reduces from 28.09 to 12.85 to 9.69 and current %THD reduces from 25.58 to 10.22 to 9.42 as the number of inverter output level increases from 5-7-9 level respectively. The simulation is carried out on MATLAB/SIMULINK platform and the results were compared with conventional method to validate the proposed scheme. The simulation results prove that the novel EPD-PWM technique can be used to effectively control the CBHMLI.

Keywords

Electric Vehicles (EVs), MATLAB/Simulink, %THD, EPD PWM Technique, Multi Level Inverter (MLI), CHBMLI

1. Introduction

Inverters convert DC power from batteries to alternating current to accelerate or

decelerate the vehicle speed and to control the motor speed and torque. The PWM technique is used to change the output frequency of the inverters, which changes required speed of the drive. The inverters required so are to be highly efficient and reliable [1]. Inverters are expensive component of EV power conversion system and also it is the critical factor in terms of overall system reliability and operation [1]. The AC output produced by the inverter can have square wave, quasi sine wave, modified sine or pure sine wave waveforms. The pure sine wave inverters are preferred as it has high efficiency and best power quality compared to remaining output types. The Total Harmonic Distortion (THD) of the inverter output is governed by the shape of the distorted wave. The poor power quality and the presence of %THD in square, modified sine and quasi sine wave definitely affects the performance of the load connected to the inverter output. Hence, the pure sine wave inverters are preferred for enhancing the quality of the output power so that life of the loads is increased.

To achieve the pure sine wave outputs at the inverter, Multi Level Inverters (MLI) are used. The MLI converts power from DC to AC in multilevel voltage steps to obtain sinusoidal voltage with lower switching losses, improved electromagnetic compatibility and higher dv/dt capability [2] [3]. The different topologies of MLI that can generate a stepped voltage waveform and that are suitable for different applications are Diode Clamped MLI, Capacitor Clamped or Flying Capacitor (FC) MLI, Neutral Point Clamped (NPC) MLI, Cascaded H-bridge (CHBMLI), etc. [4] [5] [6] [7].

The CHBMLI very agreeable for high power medium voltage drives and even for utility applications, for regenerative type motor drive, Hybrid electric vehicles, Vehicles which are based on Fuel cells, main traction drives used in electrical vehicles. As the topology requires isolated DC sources, CHBMLI are perfect for linking PV power generation with an AC grid such as in Fuel cells or PV cells, they are used in static Var generators [8].

Research shows that not a single PWM method is the best suited for all applications. There are numerous PWM Techniques developed in the field with advances in solid-state power electronics devices and microcontrollers. For above reasons, the PWM techniques are considered for intensive research subject since 1970's [9]. To minimize harmonics and switching losses in inverters, particularly in three-phase systems, PWM strategy has an important role. The main objective of modulation technique is to achieve a variable output with a supreme fundamental component and least harmonics.

The "MCPWM" methods are widely used in majority of the MLI applications [10] [11]. Sinusoidal PWM (SPWM) is one of the initial modulation signals for multicarrier based PWM. The "SPWM" technique compares a carrier signal and a pure sinusoidal modulation signal. The utilization rate of DC bus voltage for the traditional sinusoidal PWM is only 78.5%. Improvement in the rate of the DC bus voltage utilization has been the focus for research in power electronics [12].

The under-utilization of the DC bus voltage in traditional sinusoidal PWM, headed to the development of "Third Harmonic Injection PWM (THIPWM)", which added a third-order harmonic content into the sinusoidal reference signal resulting in an increase of 15.5% in the utilization rate of the DC bus voltage [12].

Abbas *et al.* [13] present the effect of over-modulation technique on single-stage three-phase grid-connected boost inverter. Performance of THIPWM is compared with over-modulation of SPWM. The THIPWM increases the inverter gain by 15% without distorting the inverter output voltage. The amplitude of modulating sinusoid is increased beyond the input voltage; the capacitor voltage will clip to input voltage. The output voltage increases during the over-modulation, but due to the clipping of the capacitors' voltage, the waveform is distorted.

Space-Vector PWM (SVPWM), one more method of enhancing the output voltage. When compared with the SPWM technique, the SVPWM technique generates less harmonics distortion and utilizes the DC bus voltage more efficiently. The "SVPWM" technique has the maximum peak fundamental magnitude of nearly 90.6% of the inverter capacity. The rise in the maximum voltage compared with conventional SPWM is 15.5% [14] [15].

Zulkifile *et al.* [16] compare SPWM, THIPWM and SVPWM for three-phase Voltage Source Inverters. The performance comparison is evaluated in terms of inverter output voltage, modulation index and switching frequency. The simulation outcomes conclude that the SPWM technique is not proficient in over modulation region and not suitable for high frequency applications. THD remains constant with the variation in input voltage for SPWM and THIPWM.

Phuong Hue Tran *et al.* [17] assessed 3 different PWM techniques "SPWM", "THIPWM" and "SVPWM" in the linear and over modulation mode and concludes from simulation results of all three PWM techniques that "SVPWM" and "THIPWM" have a greater performance compared to SPWM. SVPWM technique is intensively studied in the over-modulation region owing to its performance benefits when compared to SPWM and THIPWM, as it has higher modulation index, lower switching losses, less THD. 5% increase in ma. But SVPWM can only be applied to three-phase converters [16].

The "SPWM" technique is the easiest modulation technique to understand and to implement in software and hardware. However, this technique is incapable to fully utilize the DC bus voltage and this shortcoming led to the development of "THIPWM" and "SVPWM". In "THIPWM" technique a third-order harmonic content is added to a sinusoidal modulating signal thereby increasing the utilization rate of DC bus voltage by 15.5%. The implementation of the "SVPWM" is comparatively difficult as it requires complex mathematical operations. In under-modulation region, this algorithm provides 15.5% improved output voltages when compared to the traditional "SPWM" technique.

The present research paper proposes a novel Elliptical modulating for MCPWM technique to improve the DC bus voltage utilization. The increase in the DC bus utilization is achieved without operating PWM in over modulation region and

without injecting "third harmonic". The proposed EMC PWM technique can be easily extended to any number of output level of inverter without any complex mathematical operations involved.

This paper presents simulation of Elliptical Phase Disposition PWM (EPD-PWM) technique to control 5, 7 and 9-level inverter connected with RL-Load. The simulation results show that, as the number of levels at the output increases, the output voltage becomes smoother and also reduced harmonic content when compared to PD PWM technique [18]. The subsequent sections present the 5-level, 7-level and 9-level CHBMLI topologies with RL-Load, Simulation results Discussion and Conclusion.

2. Five-Level CHBMLI with RL-Load

Figure 1 shows the H-bridge arrangement for 5-level output [19]. An m-level CHBMLI comprises of 2 (m − 1) power semi-conductor switches, (m − 1)/2 H-Bridge cells which are fed with separate DC sources. These H-Bridges are connected in series to obtain the required m-level output. This MLI can generate nearly sinusoidal voltage waveform with one time switching per cycle of switches resulting in reduced switching losses. Figure 2 shows the use of elliptical modulating with the 4 carrier waves used for generating the PWM for the eight switches of the five-level CHBMLI.

3. Seven-Level CHBMLI with RL-Load

To achieve seven-level output in single-phase CHBMLI, the asymmetrical [20] sources of values V1 = 3/4 V_{dc} and V2 = 1/4 V_{dc} are used, where V_{dc} = 325 V to achieve r.m.s output voltage of 230 V at the inverter of Figure 3 [21]. The

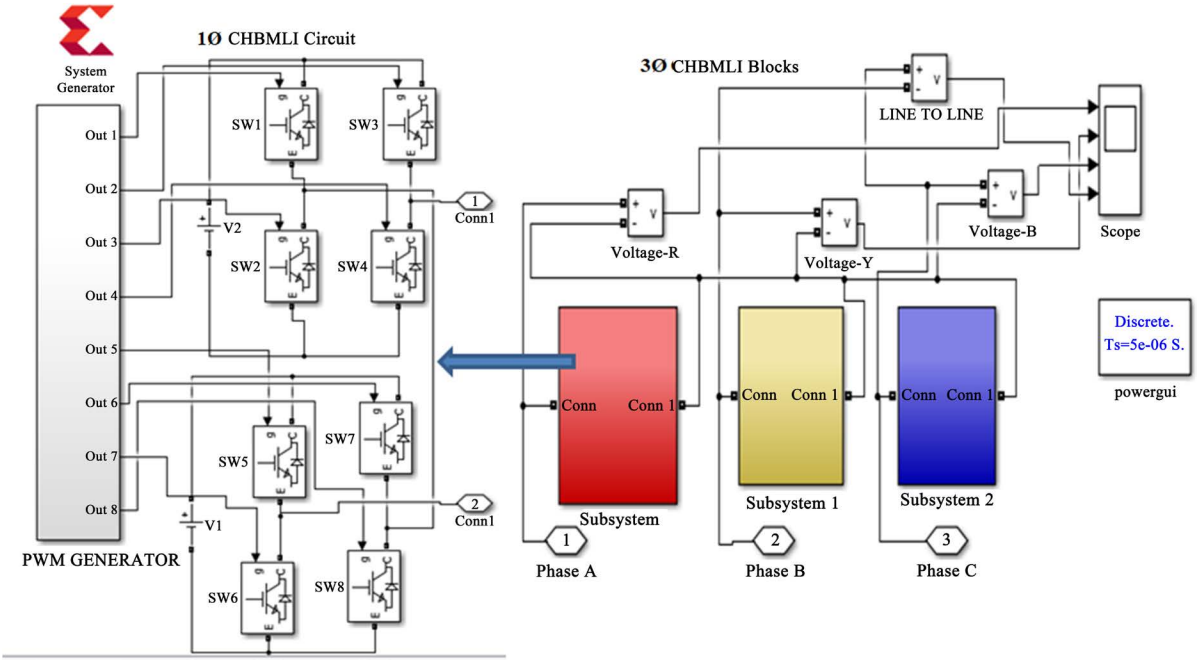

Figure 1. Simulation model of Three-phase 5-level CHBMLI topology for 5-level output.

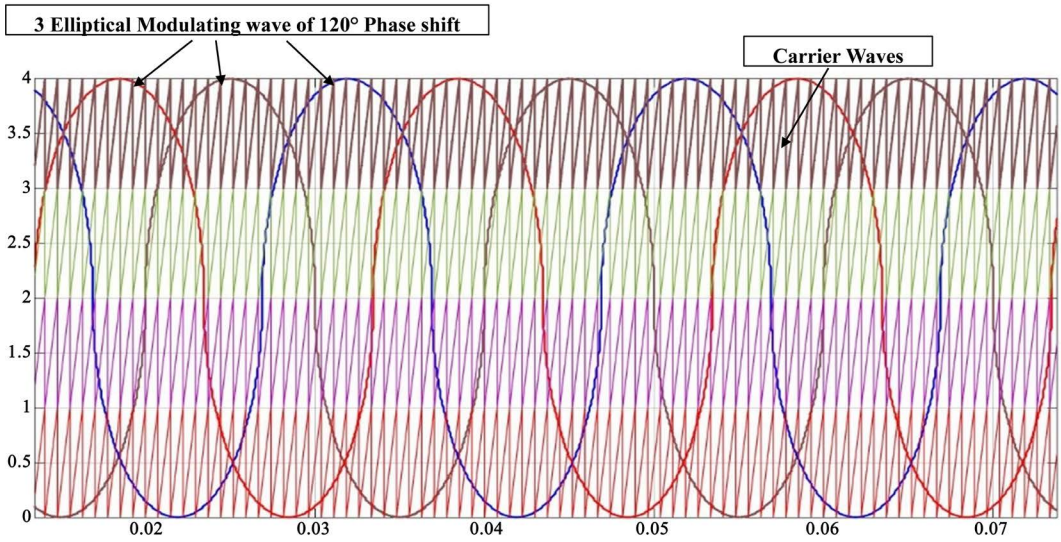

Figure 2. Comparison of carrier waves with three elliptical modulating waves of 120˚ phase shift for generating switching pulses.

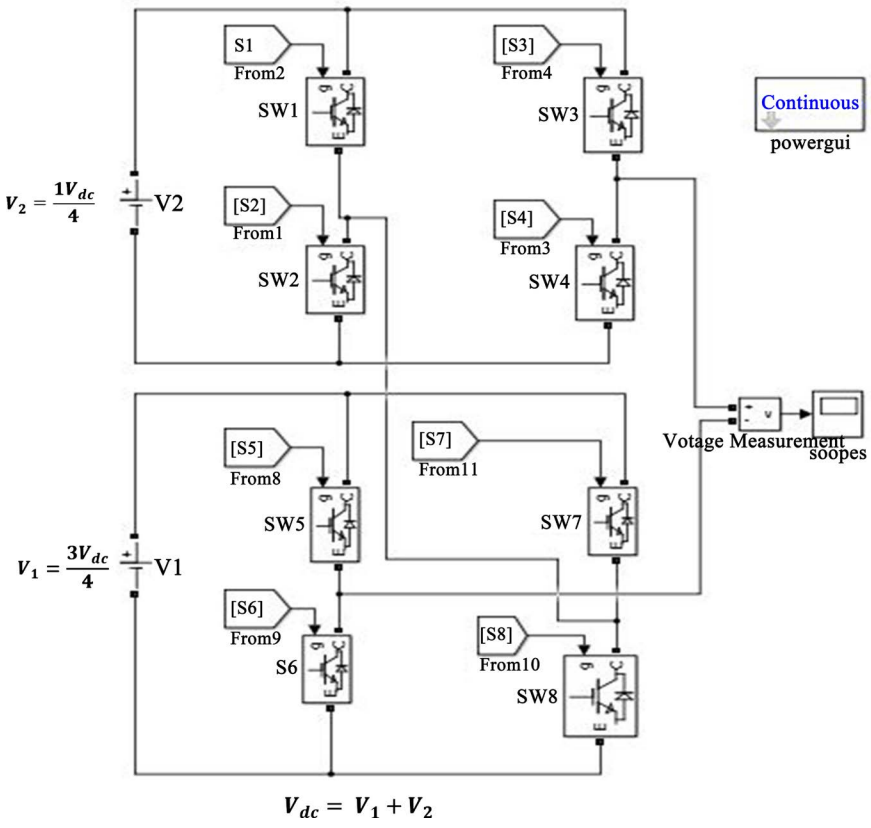

Figure 3. Single Phase 7-level CHBMLI with Asymmetrical DC sources.

switching sequence for switches to attain seven-level at the output of the inverter is given in **Table 1** [22]. To generate the required switching pulses the EPD PWM technique is used as shown in **Figure 4**, where in six carrier waves are compared with elliptical modulating wave and the switching pulses generated

are shown in Figure 5. The carrier frequency of 1350 Hz and elliptical modulating wave of fundamental frequency 50 Hz are set in the simulation.

The output voltage waveform obtained for seven-level CHBMLI at no-load is shown in Figure 6. The waveform indicates the seven-level marked with DC voltage level of {0, V1, V2, (V1 + V2), −V1, −V2, −(V1 + V2)}. To generate the PWM pulses for three-phase CHBMLI, elliptical modulating waves of 120˚ phase difference are compared with 6 carrier waves. The generated switching pulses were applied to respective ABC phases to obtain three-phase output. When a RL-Load of 400 Ω and 40 mH is connected across the three-phase CHBMLI the simulation circuit is shown in Figure 7. The Output voltage waveform and current waveform at modulation index set to 0.8 measured from the scope is as shown in Figure 8.

The output voltage is having an r.m.s value of 380 V with load current being 0.54 A. The corresponding FFT spectrum of voltage is shown in Figure 9 reads

Table 1. The switching states of 7-level CHBMLI.

Switches when turn ON	Voltage level
S1, S4, S5, S8	V_{dc}
S5, S8	$3V_{dc}/4$
S1, S4	$V_{dc}/4$
No switches are ON	0
S3, S2	$-V_{dc}/4$
S5, S6	$-3V_{dc}/4$
S3, S2, S7, S6	$-V_{dc}$

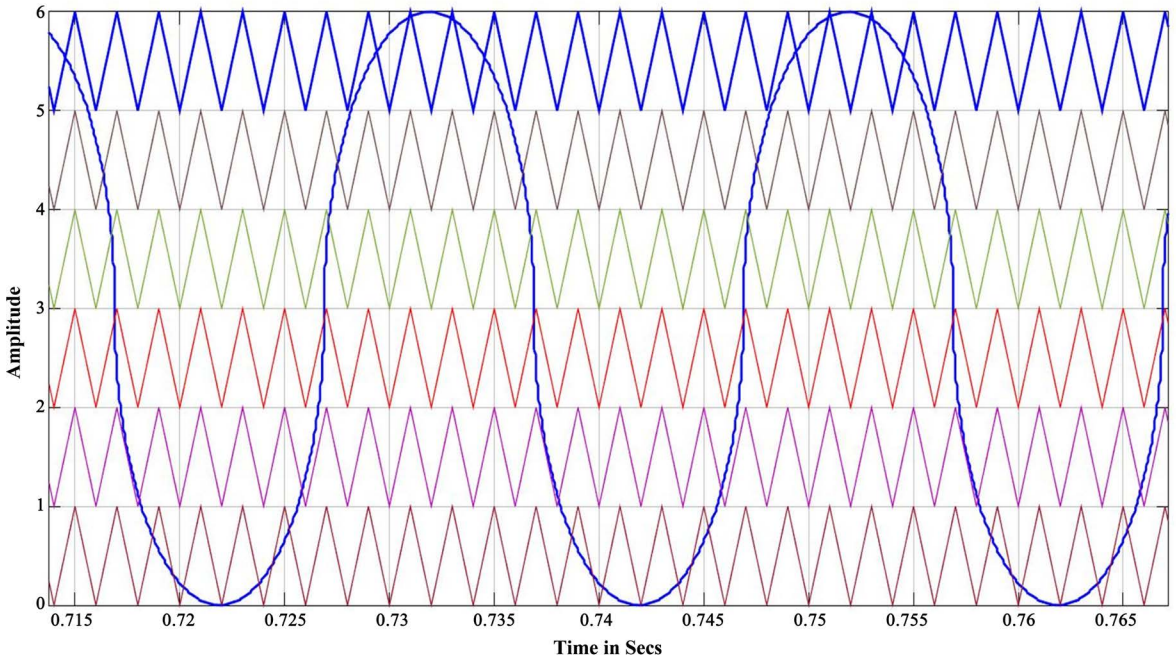

Figure 4. Carriers arrangement for EPD PWM technique for 7-level CHBMLI.

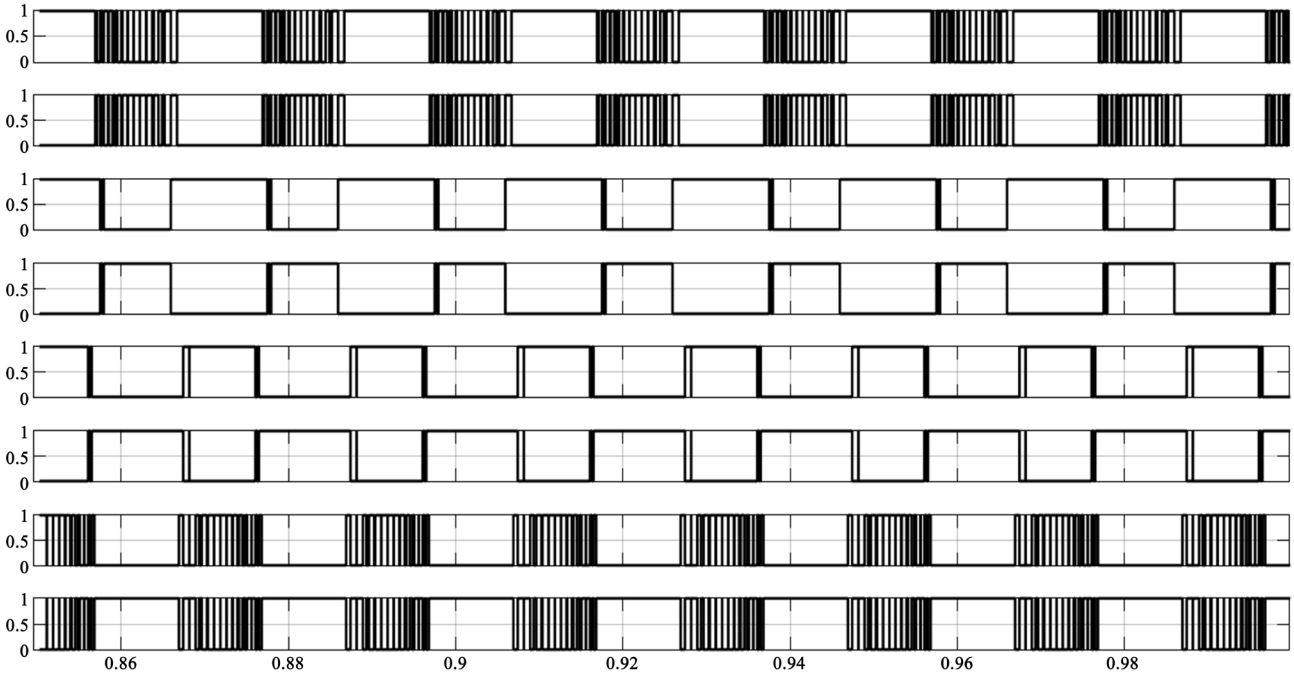

Figure 5. Switching Pulses from EPD PWM Technique for 7-level CHBMLI.

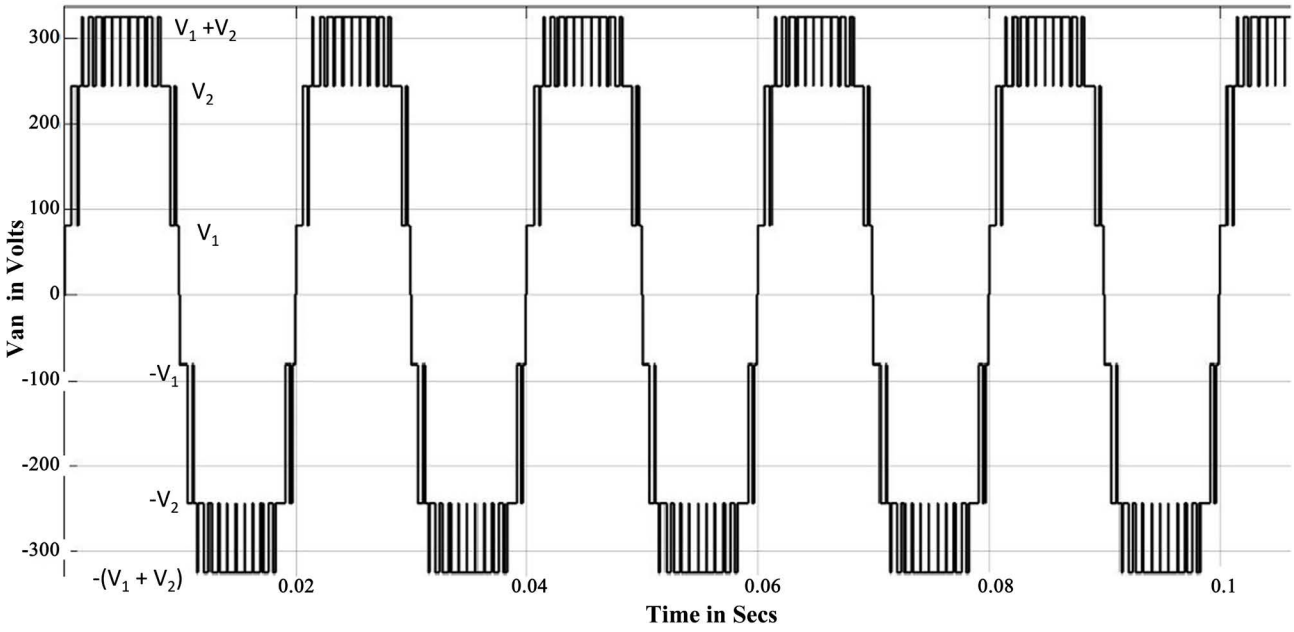

Figure 6. No-load output voltage of 7-Level CHBMLI with EPD PWM Technique at $m_a = 1$.

14.07%. For the same simulation conditions, the output voltage waveform and current waveform and the corresponding FFT spectrum for PD PWM technique are shown in Figure 10 and Figure 11 respectively. The output obtained from the two PWM methods indicates that the proposed method has resulted in increased output voltage and current with reduction in %THD.

As the number of level in the output increases, output waveform will be very near to sine wave, hence the waveform becomes smoother. The harmonic content

also reduces and quality of the waveform also improves. The same features can be noticed when the proposed EPD PWM technique is applied to 7-level CHBMLI. The results obtained from three-phase 5-level CHBMLI and 7-level CHBMLI for the same simulation conditions are compared in Table 3. The comparison is made for line voltage, line current and %THD for different modulation indices at fundamental frequency of 50 Hz. The results clearly show that

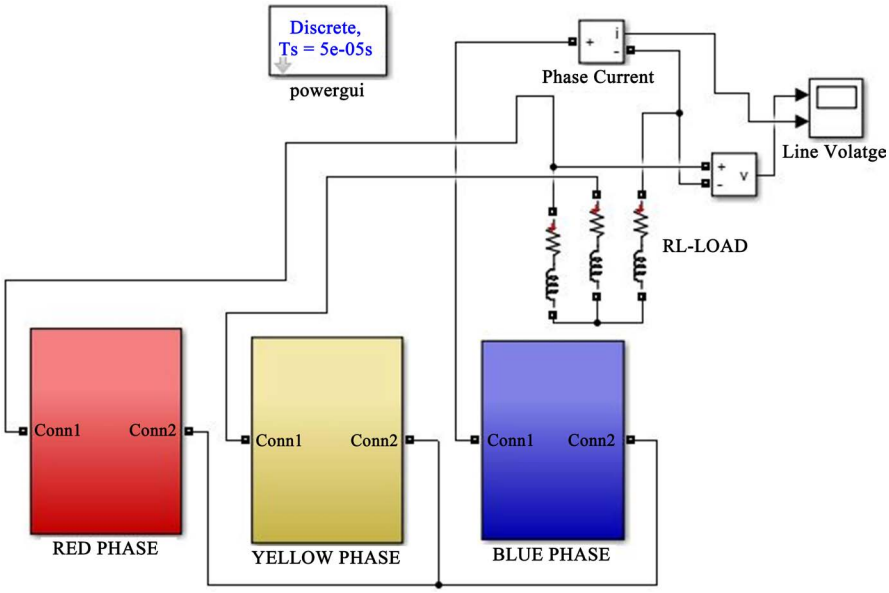

Figure 7. Three-Phase 7-level CHBMLI with RL-load.

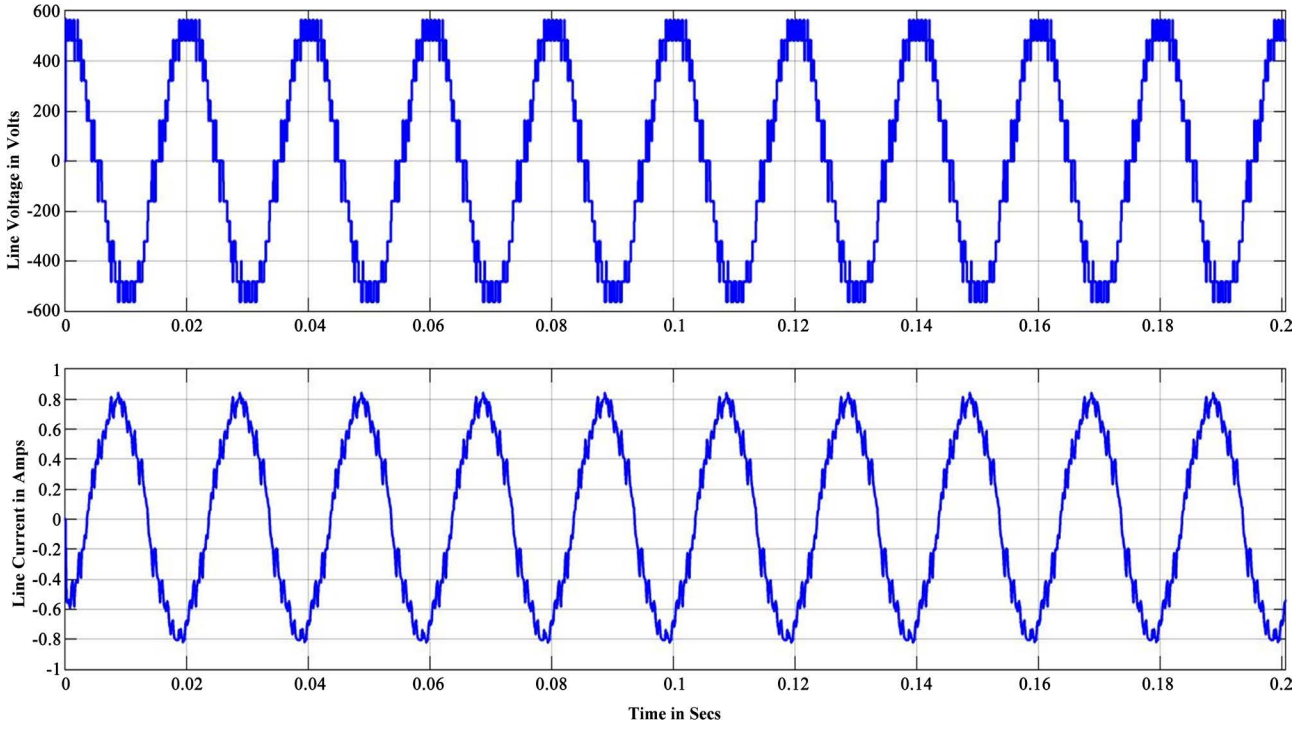

Figure 8. Output line Voltage and Current Waveform of three-phase 7-level CHBMLI with EPD PWM Technique with RL-Load at $m_a = 0.8$.

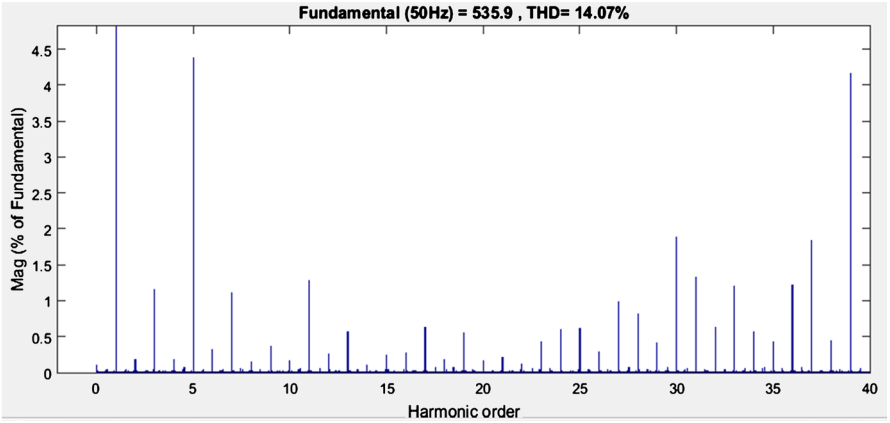

Figure 9. FFT spectrum of output line voltage of EPD PWM technique with $m_a = 0.8$.

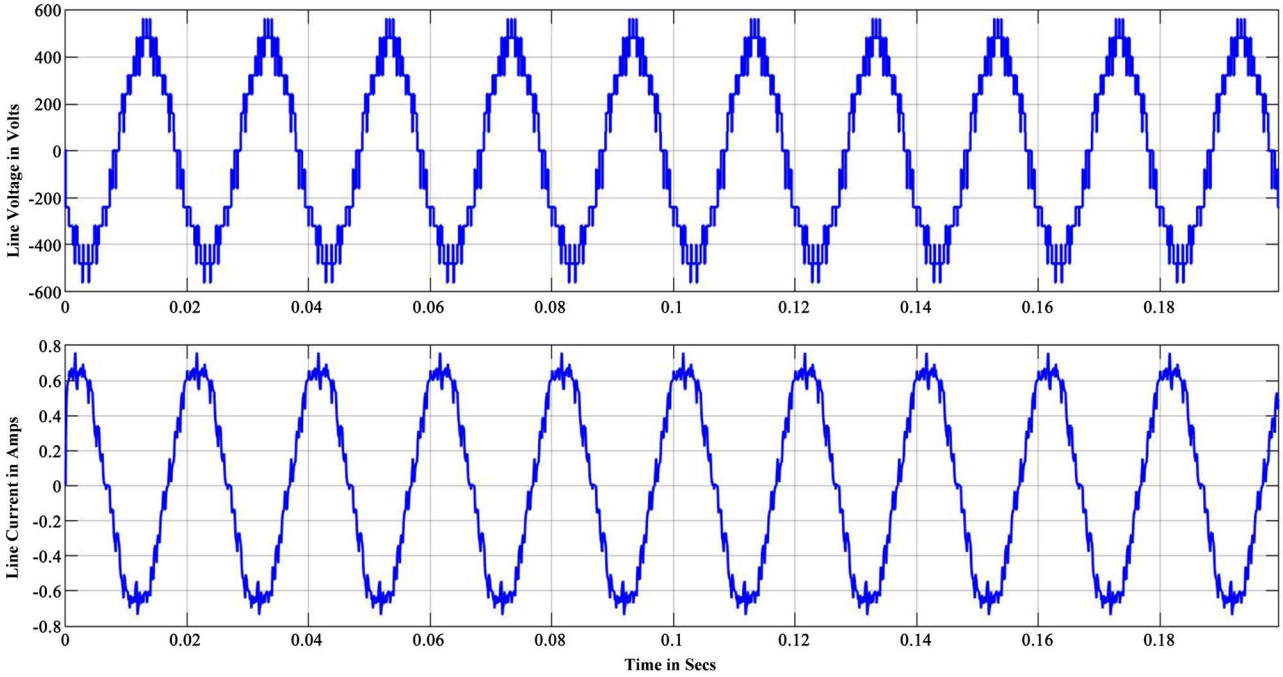

Figure 10. Output line Voltage and Current Waveform of three-phase 7-level CHBMLI with PD PWM Technique with RL-Load at $m_a = 0.8$.

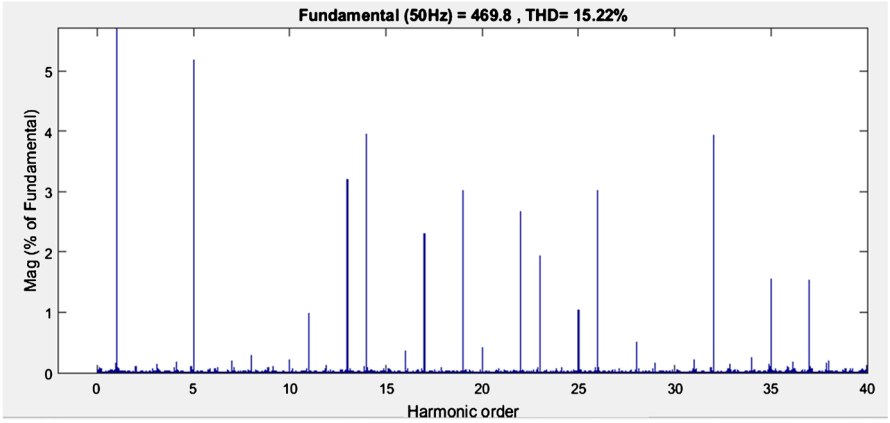

Figure 11. FFT spectrum of output voltage of PD PWM technique with $m_a = 0.8$.

there is an increase in the output voltage of 7-level CHBMLI.

The comparison is made for line voltage, line current and %THD for different modulation indices at fundamental frequency of 50 Hz. The results clearly show that there is an increase in the output voltage of 7-level CHBMLI.

At $m_a = 1$, the output of 7-level CHBMLI produces a line voltage of 454 V when compared to 5-level CHBMLI which is producing 452.5 V. At the same time the harmonic spectrum has also been reduced at all modulation indices in the 7-level CHBMLI. Even the r.m.s current is increased in 7-level CHBMLI. There is remarkable suppression of current harmonics in the 7-level compared to 5-level inverters, which results in reducing the output filter component size.

4. Nine-Level Single-Phase CHBMLI

Figure 12 shows the 9-level CHBMLI with three H-Bridges connected to separate DC sources having values 75 V, 150 V and 100 V, so that the total input voltage is equal to 325 V. The Elliptical Phase Disposition PWM technique is used to control the output voltage with a switching frequency of 1350 Hz. The switching table to generate the 9-level output voltage is listed in Table 2 and the output no-load voltage in Figure 13.

The output voltage waveform obtained for 9-level CHBMLI at no-load is shown in Figure 13. The waveform indicates the seven-level marked with DC

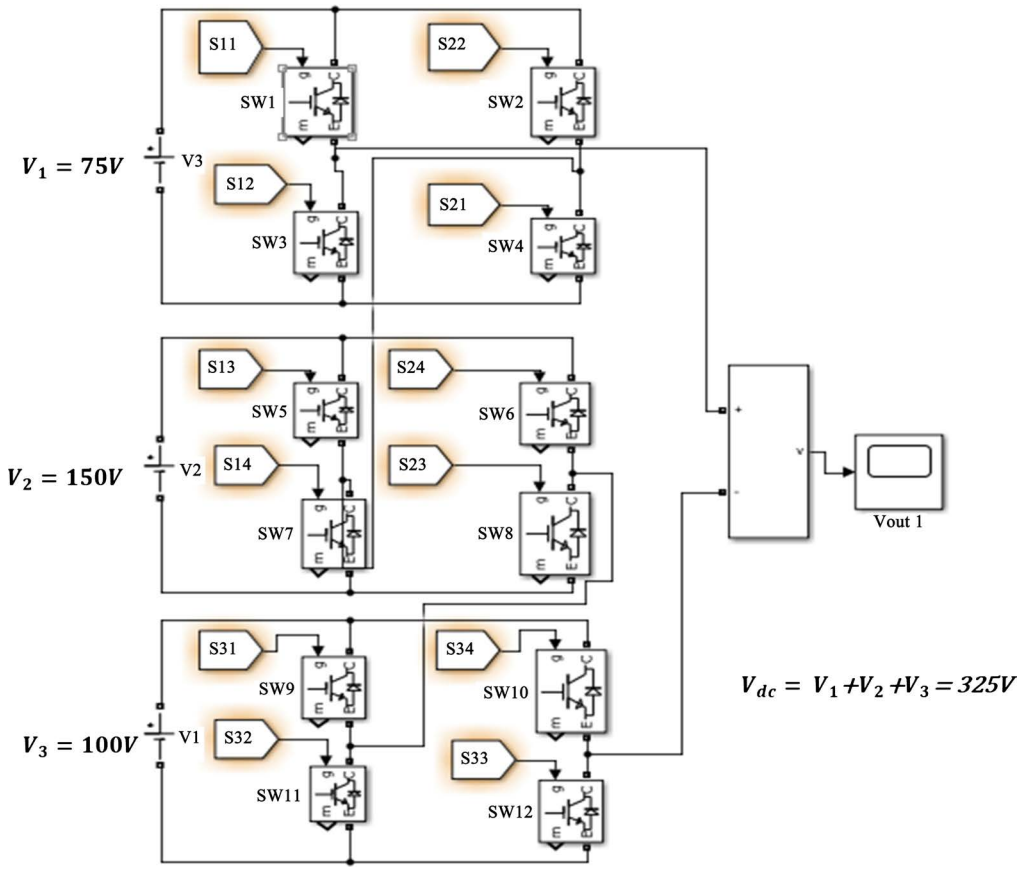

Figure 12. Nine-level single-phase CHBMLI circuit with No-load.

Table 2. Switching table to generate 9-level output voltage.

Switches when turn ON	Voltage level
S1, S4, S5,S8, S9, S12	V1 + V2 + V3
S1,S4, S5, S8, S9, S10	V1 + V2
S2,S4, S5, S8, S9, S10	V2
S1, S4, S7, S8, S9, S10	V1
No switches are ON	0
S2, S3, S7, S8, S9, S10	−V1
S2, S4, S7, S6, S9, S10	−V2
S2, S3, S7, S6, S9, S10	V1 + V2
S2, S3, S7, S6, S11, S10	V1 + V2 + V3

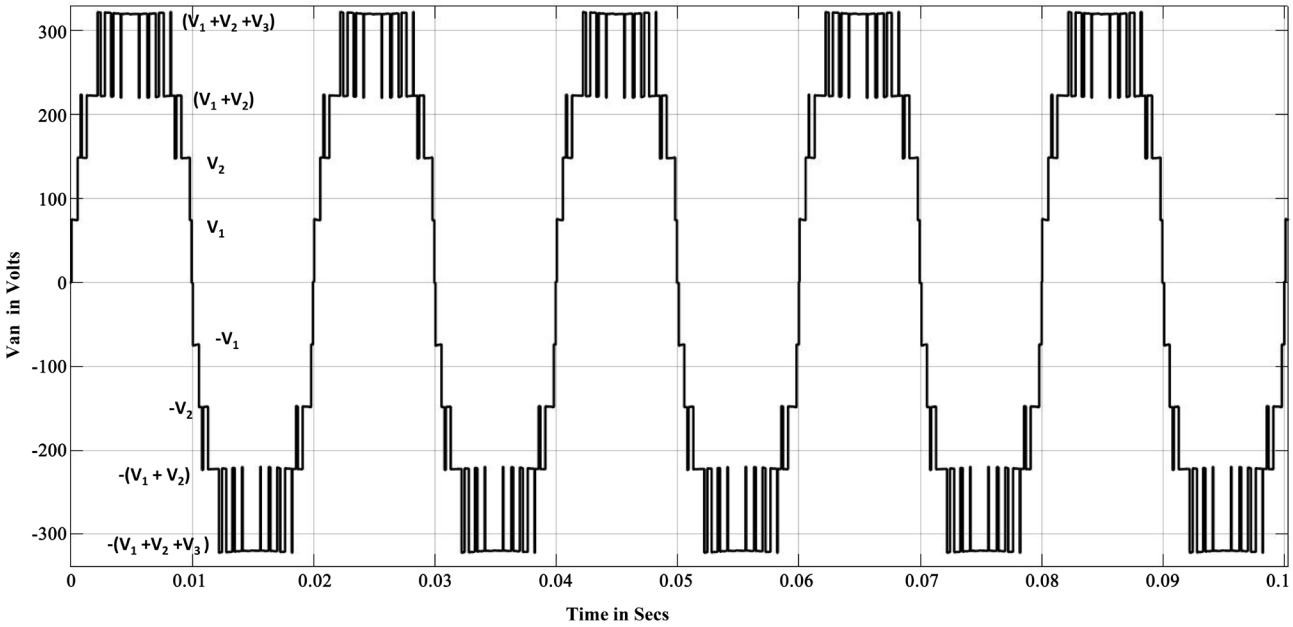

Figure 13. Output phase voltage of 9-level CHBMLI with no-Load.

voltage level of {0, V1, V2, (V1 + V2), (V1 + V2 + V3), −V1, −V2, −(V1 + V2), −(V1 + V2 + V3)}. To generate the PWM pulses for three-phase CHBMLI, elliptical modulating waves of 120˚ phase difference are compared with 8 carrier waves. The generated switching pulses were applied to respective ABC phases to obtain three-phase output. When a RL-Load of 400 Ω and 40 mH is connected across the three-phase CHBMLI.

5. Simulation Results Discussion

The performance comparison of 5, 7 and 9-level three-phase inverters are listed in Table 3. The output at the inverter is maintained to 325 V peak to achieve 230 V r.m.s value and 400 V line voltage. The modulation index is varied from 0.4 to 1 and the output voltage and current are recorded with corresponding %THDs. From the outputs obtained at modulation index 1 of all the three-level inverters

shows that there is an increase in the output r.m.s value compare to sinusoidal PWM technique [18] [23] [24]. The output voltage quality has also improved with reduction in the %THD. The comparison chart is shown in Figure 14 for output voltage harmonic contents and Figure 15 for output current harmonics

Table 3. Performance comparison of EPD PWM Technique fed Three-phase 5-Level, 7-level and 9-level CHBMLI with RL-Load.

Output Level	M_a	V_{rms}	$\%THD_V$	I_{line}	$\%THD_I$
5-level	1	452.5	**16.86**	0.61	20.88
	0.8	362.2	**18.09**	0.514	25.85
	0.6	271.7	25.75	0.385	25.18
	0.4	181.1	40.01	0.258	40.4
7-Level	1	454	**12.85**	0.65	10.36
	0.8	380.1	**14.4**	0.54	10.22
	0.6	273.2	23.89	0.39	15.16
	0.4	245.5	37.4	0.2	21.8
9-Level	1	442.1	**9.69**	0.632	**8.88**
	0.8	337.6	**9.69**	0.483	**9.42**
	0.6	249	14.64	0.357	10.38
	0.4	166.7	19.17	0.238	13.05

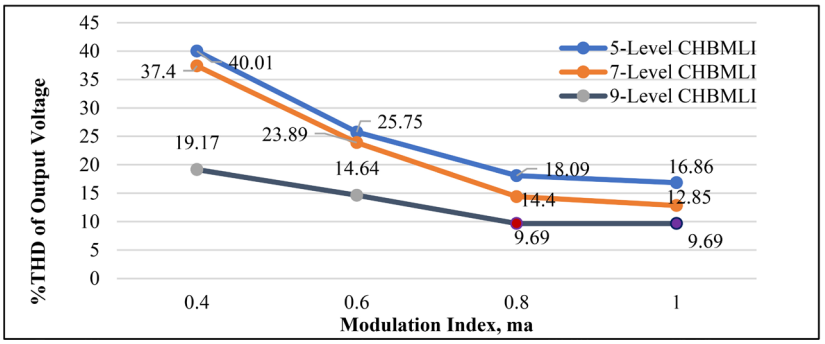

Figure 14. Comparison of %THD of output voltage in 5, 7 and 9-level inverter.

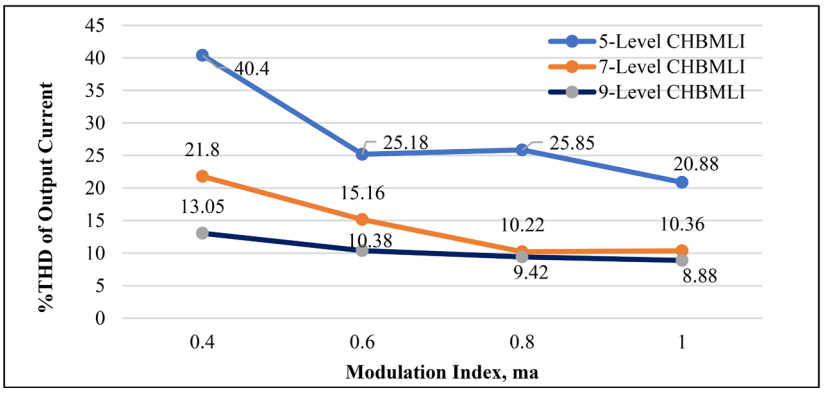

Figure 15. Comparison of %THD of output current in 5, 7 and 9-level inverter.

proves that, as the number of output level increases the harmonics reduces achieving improved performance of the inverter which reduces the losses thereby increasing the efficiency of the inverter system in power conversion.

6. Conclusion

The proposed novel Elliptical Phase Disposition PWM (EPDPWM) technique is applied to three-phase 5, 7 and 9-level CHBMLI and the performance are investigated. The results of line voltage and %THD for both voltage and current are noted for different modulation indices. The proposed elliptical wave produces enhanced output line voltage and the %THD reduces and is less when compared to conventional Sine PWM. Simulation results illustrate the performance and effectiveness of the proposed EPD-PWM Technique in generating a high quality five, seven and nine-level multilevel inverter output voltage waveform. The proposed EPD PWM technique can be easily extended to any output level of the inverter, with less complexity involved in the implementation of control strategy and PWM generation. Also, it works very efficiently improving DC bus utilization 15% compared to traditional MCPWM technique. This increase in the output is obtained without over-modulation and without third harmonic injection to modulating wave.

Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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