

On the Performance of ISFET-Based Device for Water Quality Monitoring

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Abstract

A new configuration realizing water quality monitoring device using ISFET involving low power CMOS Integrated “Ion Sensitive Field Effect transistor (ISFET)—Operational Amplifier is presented. The study’s main focus is on simulation of power and performance analysis of ISFET device, which is used for water quality monitoring. This approach can improve calibration of device to a fairly wide range without the use of a high speed digital processor. The conventional device has a drawback of slow slew rate but in this novel design, the device has a better slew rate. A new slew rate enhancement (SRE) incorporated into a ISFET, which does not affect the small signal frequency response. The functionality of the circuit is tested using Tanner simulator version 15 for a 70 nm CMOS process model also the transfer function realization is done on MATLAB R2011a version, the Very high speed integrated circuit Hardware description language (VHDL) code for the same scheme is simulated on Xilinx ISE 10.1 and various simulation results are obtained. Simulation results are included to demonstrate the results.

Keywords: ISFET, Slew Rate, Calibration, Simulation, Monitoring Applications, pH Value, Alkalinity

1. Introduction

Monitoring the pH of water resources and sewage discharge for water pollution is typical and necessary task in today’s overdeveloped scenario. The normal pH for surface water systems is 6.5 - 8.5 and for ground water system 6 - 8. Water with low pH is acidic, corrosive and contains several toxic materials which are very dangerous for health, but the water having pH more than 8.5 is called hard water which does not contain harmful materials but the long use of such kind of water can cause aesthetic problems [1-3]. With the invention of ISFET [4] there has been a rapid development of pH Measurement Instruments [5]. With the further advancement of semiconductor technology ISFET emerged as a standard device. In spite of the fact that ISFET Sensor has been developed 30 years ago [6], several drawback of ISFET sensor remained unsolved, such as phenomena of fluctuation with time and temperature variations. This cause in drift in the pH values [7], and result in poor and slow response [8] of the device. The second phenomenon is pH dependent Temperature Coefficient [9] and non linear temperature dependent mobility in MOSFETS of

ISFET device [10]. Also it was observed that in ISFET drift rate has an exponential incremental tendency with pH values as well as Temperature.

In Urban water supply system, the water quality determining indices such as pH value and turbidity are monitored continuously. When the indices exceed the limiting value, the system will effectively handle the treatment against deterioration ensuring the safety of water. Water is vital for all known forms of life. Many research works have contributed to design water quality measuring devices. But it has always been a challenge to find a precise and accurate device for monitoring the quality of water.

The concept of pH was first introduced by Danish chemist Soren Peder Lauritz Sorensen at the Carlsberg Laboratory in 1909 and revised to the modern pH in 1924 after it became apparent that electromotive force in cells depended on activity rather than concentration of hydrogen ions. The pH is a measure of the acidity or basicity of an aqueous solution.

The use of micro sensors for infield monitoring of environmental parameters is gaining interest due to their advantages over conventional sensors. In the field of

micro sensors for environmental applications, Ion Selective Field Effect Transistors (ISFETs) has proved to be of special application. They are particularly helpful for measuring pH and other ions in small volumes and they can be integrated in compact flow cells for continuous measurements and monitoring [11-16].

Pure water is said to be neutral, with a pH close to 7.0 at 25°C (77 F). Solutions with a pH less than seven (7) are said to be acidic and solutions with a pH greater than seven (7) are basic or alkaline.

This study highlights a performance analysis of low power CMOS Integrated “Ion Sensitive Field Effect transistor (ISFET)—Operational Amplifier. The studies mainly focus on the simulation of power and performance analysis of ISFET device, which is used for water quality monitoring applications [17-23]. This approach can improve calibration of device to a fairly wide range without the use of a high speed digital processor. The conventional device generally used, consumes high power and is not stable with temperature and frequency variations for long term monitoring. The conventional device has a drawback of slow slew rate but in this novel design the device has a fairly good slew rate this device has a simple architecture, and hence is very suitable for the water quality monitoring application. In this novel design, the device is free from noise and other effect and is seen consuming low power of the order of 13 μ W.

The paper is organized as follows: Section 2 describes the ISFET, Section 3 explains the device description and mathematical modeling and, Section 4 Simulation and result analysis, Section 5 gives the results and conclusions and Section 6 present the future works to be done.

2. ISFET

An ISFET is an ion-sensitive field-effect transistor which has a property of measuring ion concentrations in solution; when the ion concentration (such as H^+) changes, the current through the transistor will change accordingly [5]. Here, the solution is used as the gate electrode. A voltage between substrate and oxide surfaces arises due to an ions' sheath.

The ISFET has the similar structure as that of the MOSFET except that the poly gate of MOSFET is removed from the silicon surface and is replaced with a reference electrode inserted inside the solution, which is directly in contact with the hydrogen ion (H^+) sensitive gate electrode as shown in **Figure 1** [6].

At the interface between gate insulator and the solution, there is an electric potential difference that depends on the concentration of H^+ of the solution, or so called, pH value. The variation of this potential caused by the

pH variation will lead to modulation of the drain current [7]. As a result, the Id-Vgs transfer characteristic of the ISFET, working in triode region, can be observed similar with that of MOSFET:

$$I_{ds} = \frac{\mu C_{ox} W}{L} \left[(V_{gs} - V_{th_isfet}) V_{DS} - \frac{1}{2} (V_{ds})^2 \right] \quad (1)$$

The threshold voltage is only different in case of MOSFET. In ISFET, defining the metal connection of the reference electrode as a remote gate, the threshold voltage is given by:

$$V_{th(ISFET)} = E_{Ref} + \Delta\Phi^{lj} - \Psi_{eol} + \chi^{sol} + \frac{-\Phi_s}{q} - \frac{Q_{ox} + Q_{ss}}{C_{ox}} + \gamma \{2\phi\epsilon\}^{1/2} + 2\Phi_\epsilon \quad (2)$$

where E_{Ref} is Potential of reference electrode, $\Delta\Phi^{lj}$ is the potential drop between the reference electrode and the solution, which typically has a value of 3 mV [8]. Ψ_{eol} is the potential which is pH-independent; it can be viewed as a common-mode input signal for an ISFET interface circuit in any pH buffer solution and can be nullified during system calibration and measurement procedures with a typical value of 50 mV [9]. χ^{sol} is the surface dipole potential of the solvent being independent of pH.

The terms in the parentheses are almost the same as that of the MOSFET threshold voltage except that of absence of the gate metal function. The other terms in above equation are a group of chemical potential, among which the only chemical input parameter shown has to be a function of solution pH value. This chemical dependent

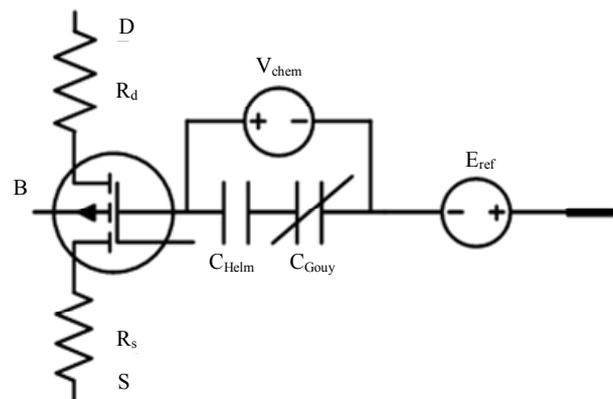


Figure 1. Sub circuit block of ISFET macro model.

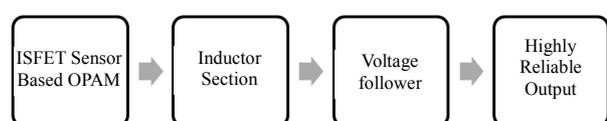


Figure 2. Block diagram of monitoring device.

characteristic has already been explained by the Hal and Eijkel's theory [15] which is elaborated using the general accepted site-binding model and the Gouy-Chapman-Stern model.

3. Device Description and Mathematical Modeling

The basic structure of the device consists of three major parts, (I) ISFET (II) Inductor section, and (III) voltage follower, as shown in **Figure 2**. The proposed circuit of device is shown above, in which the output of the ISFET sensor is fed into one of the terminal of the voltage follower, which helps from the loading effect and keeping the voltage level constant irrespective of the change in the current value. This practise increases the sensitivity of the sensor, and even a very small value can be observed at the output.

As

$$V_o = V_{in} + \frac{R_f}{R_i} \quad (3)$$

Under ideal condition the Op-Amp $R_i = \infty$ and thus

$$V_o = V_{in} \quad (4)$$

ISFET Sensor Based Op-Amp

The threshold voltage of a dual dielectric gate ISFET is given by

$$V_{TH} = \phi_{ES} - \frac{Q_{SS}}{C_{in}} - \frac{Q_i}{C_l} + 2\phi_F - \frac{\sqrt{2K_s \epsilon_0 q N_B |2\phi_F + V_{SB}|}}{C_{in}} + 2.303 \frac{kT}{q} \cdot S \cdot (pH - pH_{pzc}) \quad (5)$$

where ϕ_{ES} is the "work function" difference between the electrode in contact with the electrolyte and the semiconductor = ϕ_i , is the interface charge sandwiched between the dual dielectric of the ISFET gate Q_{SS} , is a lumped interface and fixed charge referred to the oxide/silicon interface C_l is the top gate dielectric capacitance per unit area, C_{in} is the total gate capacitance per unit area, N_B is the bulk doping, V_{SB} is the source-to-bulk reverse bias, ϕ_F is the Fermi-level of the silicon bulk, S is the sensitivity factor of the top pH sensing insulator and pH_{pzc} is the point-of-zero-charge of the sensing insulator of the ISFET.

The circuit functions as follows: when the ISFET-operational amplifier is configured as a voltage follower as shown in **Figure 3** the output voltage (V_o) is equal to the input voltage (V_{in}); any difference in threshold voltages and bias currents between the two input transistors at the differential input stage will also appear at the output. The output voltage of the device is found to be

$$V_o = V_{in} + \phi_{ms} - \phi_{ES} - 2.303 \frac{kT}{q} \cdot S \cdot (pH - pH_{pzc}) + V_{os} \quad (6)$$

where V_{in} is the offset voltage which is temperature and light sensitive but chemically insensitive. The offset: voltage includes terms arising from the mismatch of the total gate capacitances (C_{in}), semiconductor bulk charges $\sqrt{2K_s \epsilon_0 q N_B |2\phi_F + V_{SB}|}$, insulator interface charges (Q_{ss} , Q_i), and transistor gain (β) between the MOSFET and the ISFET.

The ideal reference electrode commonly employed in combination with the ISFET sensor as shown in **Figure 4** serves two functions:

1) to provide an electrical contact to the test electrolyte and thus define the electrical potential of the electrolyte;

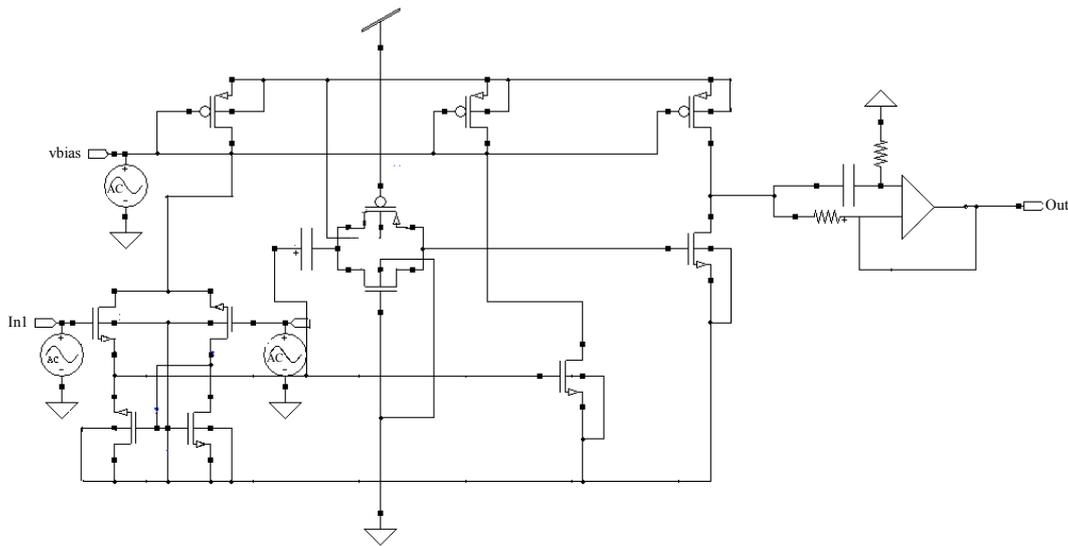


Figure 3. Equivalent circuit of device.

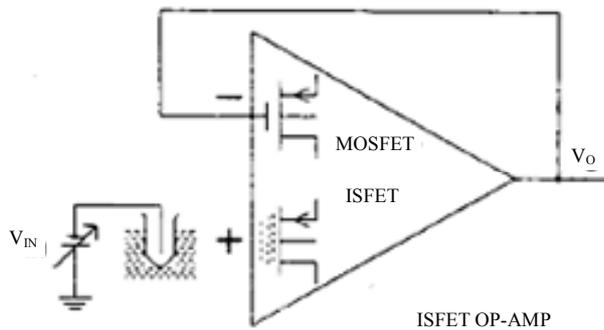


Figure 4. Block diagram Representation of ISFET based OP-amp.

and 2) to provide an electrode-electrolyte interface potential invariant with the electrolyte composition such that the dependence of the threshold voltage of the ISFET on the electrolyte composition arises only from the electrolyte-insulator interface of the ISFET.

4. Simulation and Result Analysis

The circuit of the Op-amp based Ion Sensitive Field Effect Transistor (ISFET) is implemented on Tanner tool version-15. The device is modeled on 250 nm technology as shown in **Figure 5** and the output results of T-spice command file and output waveform of the transient

analysis are found and shown in **Figures 6** and **7**. From the transient analysis it is observed that the output waveform is not linear. This shows that the slew rate of the device is poor. To improve the slew rate, a simulated inductor is placed at the output and the analysis results as computed are shown in the **Figures 8-10**. It may be seen that there is a significant improvement in the slew rate when a simulated inductor is placed parallel to the load at the output. **Figures 11-13** show the RTL diagram of the device, the components used in device, VHDL instantiation created from source file results obtained when the VHDL code of the device is simulated on Xilinx ISE 10.1. The synthesis file and power result obtained by simulation of the circuit is shown in appendix at the end of the paper. In this proposed design, the device is free from interference effects. It also consumes much low power, in order of $13 \mu\text{W}$. The output observed in **Figure 9** is highly linear, indicating that the device is stable for a large dynamic range of input signals.

In the above **Table 1** shows the various readings of the device during the transient analysis.

Table 2 Shows the various process parameters used in the proposed scheme and it is observed that the Average power consumed by the device is $13 \mu\text{W}$ and the max power consumed is $16 \mu\text{W}$ under the current range of $1 \mu\text{A} - 50 \mu\text{A}$.

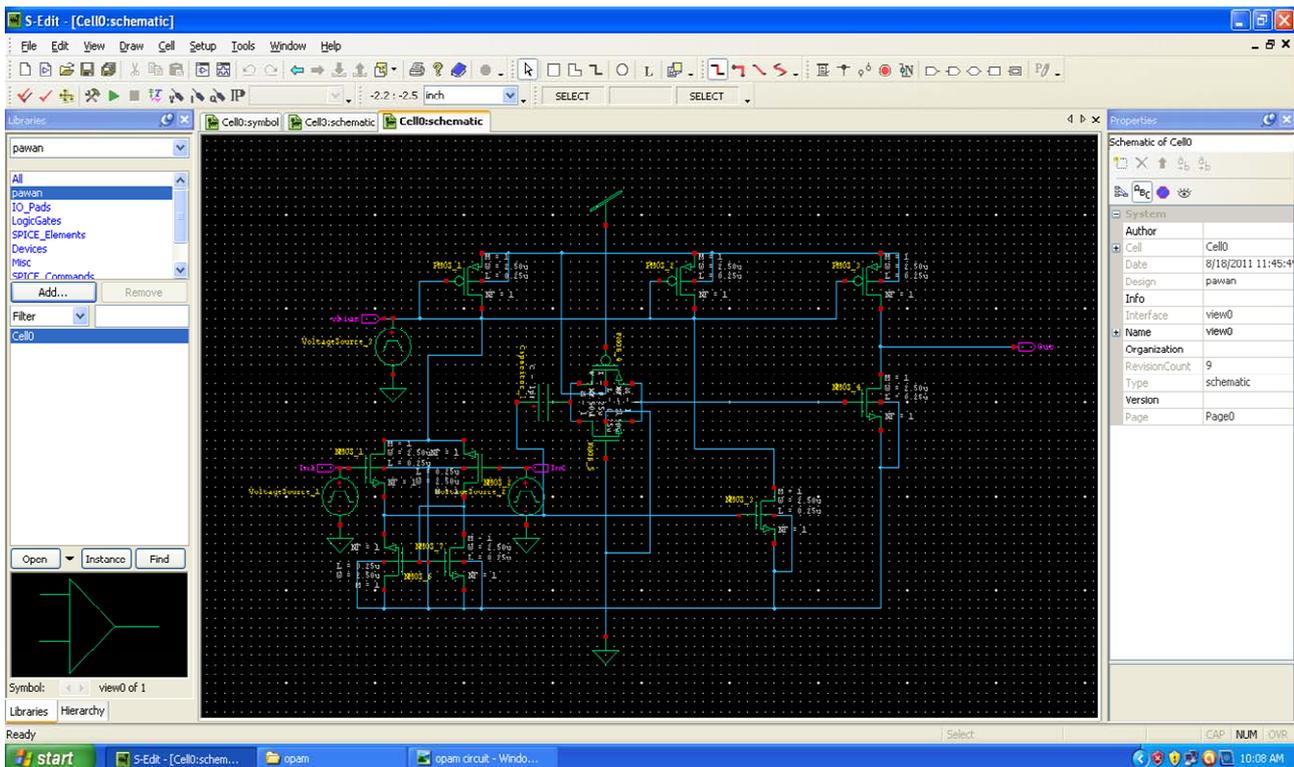


Figure 5. Circuit diagram of device.

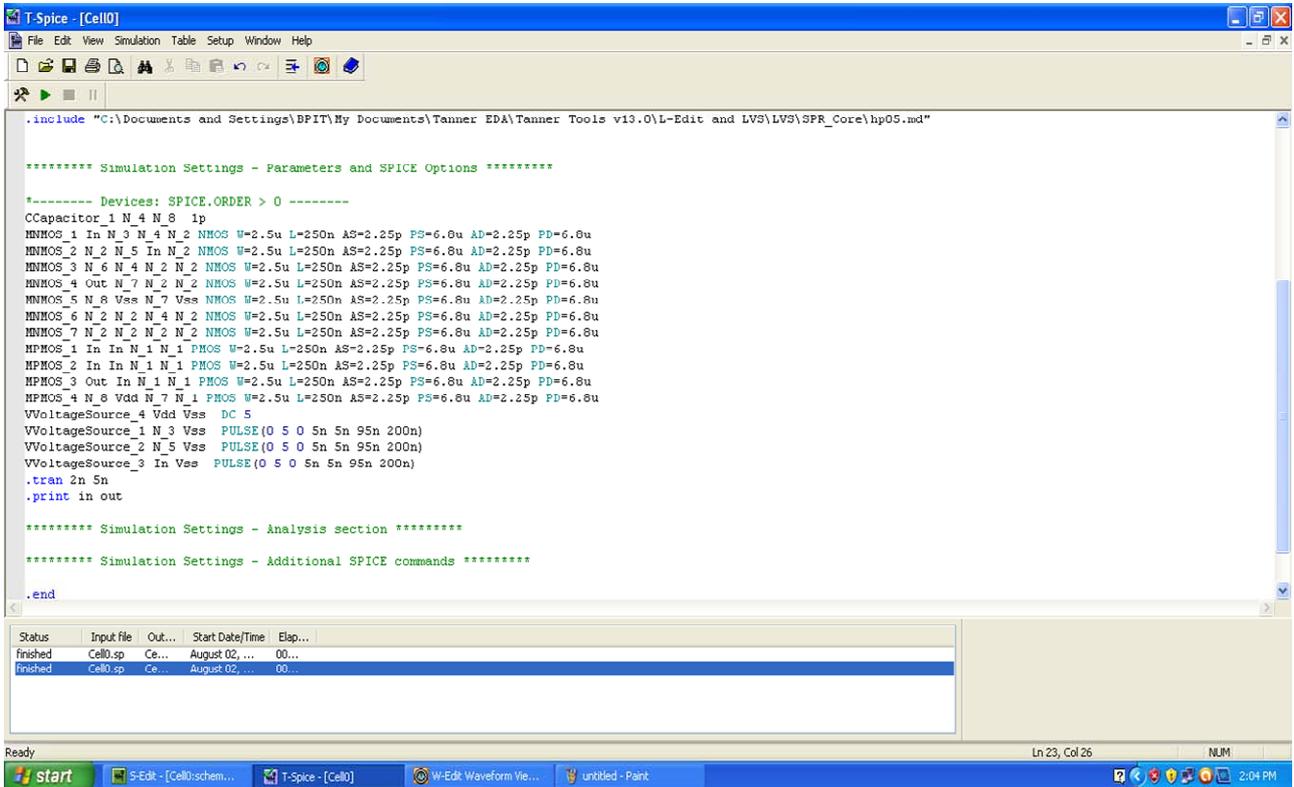


Figure 6. T-Spice file for the above circuit.

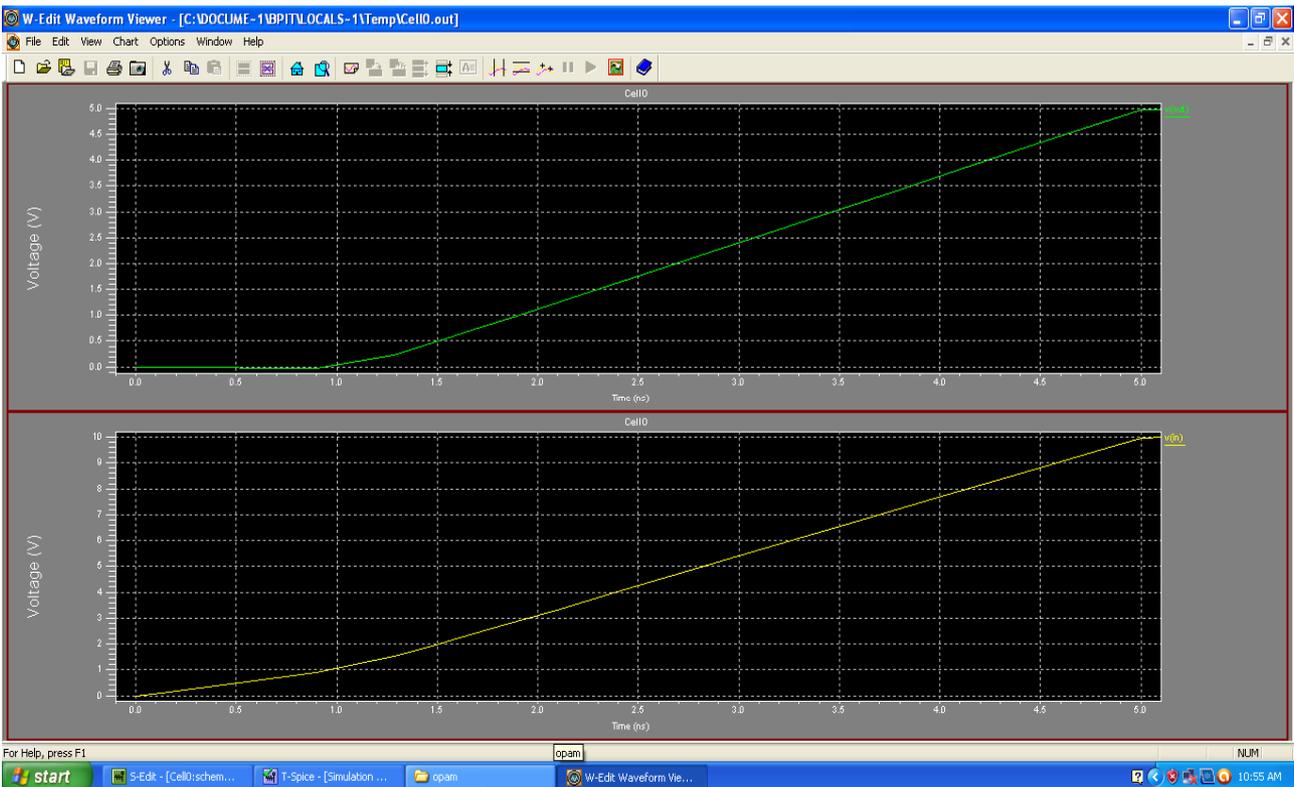


Figure 7. Output waveform of the above circuit.

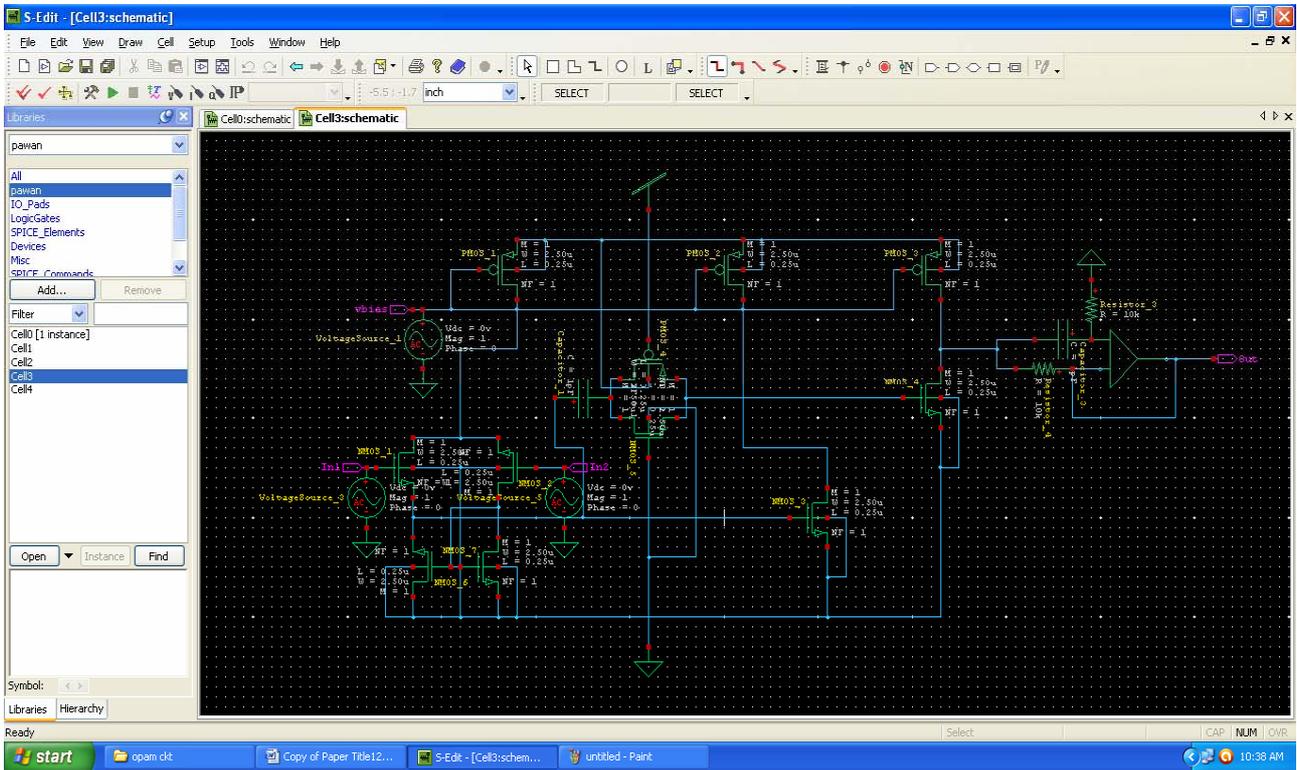


Figure 8. Circuit diagram of device using inductor.

```

.include "C:\Documents and Settings\BPIT\My Documents\Tanner EDA\Tanner Tools v13.0\L-Edit and LVS\LV5\SPR_Core\hp05.md"

***** Simulation Settings - Parameters and SPICE Options *****
+----- Devices: SPICE.ORDER > 0 -----
CCapacitor_1 N_4 N_8 1p
LInductor_1 Out Vss L=1n
MNMOS_1 In N_3 N_4 N_2 NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MNMOS_2 N_2 N_5 In N_2 NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MNMOS_3 N_6 N_4 N_2 N_2 NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MNMOS_4 Out N_7 N_2 N_2 NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MNMOS_5 N_8 Vss N_7 Vss NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MNMOS_6 N_2 N_2 N_4 N_2 NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MNMOS_7 N_2 N_2 N_2 N_2 NMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MPMOS_1 In In N_1 N_1 PMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MPMOS_2 In In N_1 N_1 PMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MPMOS_3 Out In N_1 N_1 PMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
MPMOS_4 N_8 Vdd N_7 N_1 PMOS W=2.5u L=250n AS=2.25p PS=6.8u AD=2.25p PD=6.8u
VVoltageSource_4 Vdd Vss DC 5
VVoltageSource_1 N_3 Vss PULSE(0 5 0 5n 5n 95n 200n)
VVoltageSource_2 N_5 Vss PULSE(0 5 0 5n 5n 95n 200n)
VVoltageSource_3 In Vss PULSE(0 5 0 5n 5n 95n 200n)
.tran 2n 50n
.print in out

***** Simulation Settings - Analysis section *****
***** Simulation Settings - Additional SPICE commands *****
    
```

Status	Input file	Out...	Start Date/Time	Elap...
finished	Cell0.sp	Ce...	August 17, ...	00...
finished	Cell0.sp	Ce...	August 17, ...	00...
finished	Cell0.sp	Ce...	August 17, ...	00...
finished	Cell0.sp	Ce...	August 17, ...	00...
finished	Cell0.sp	Ce...	August 17, ...	00...

Figure 9. T-Spice file for the above circuit.

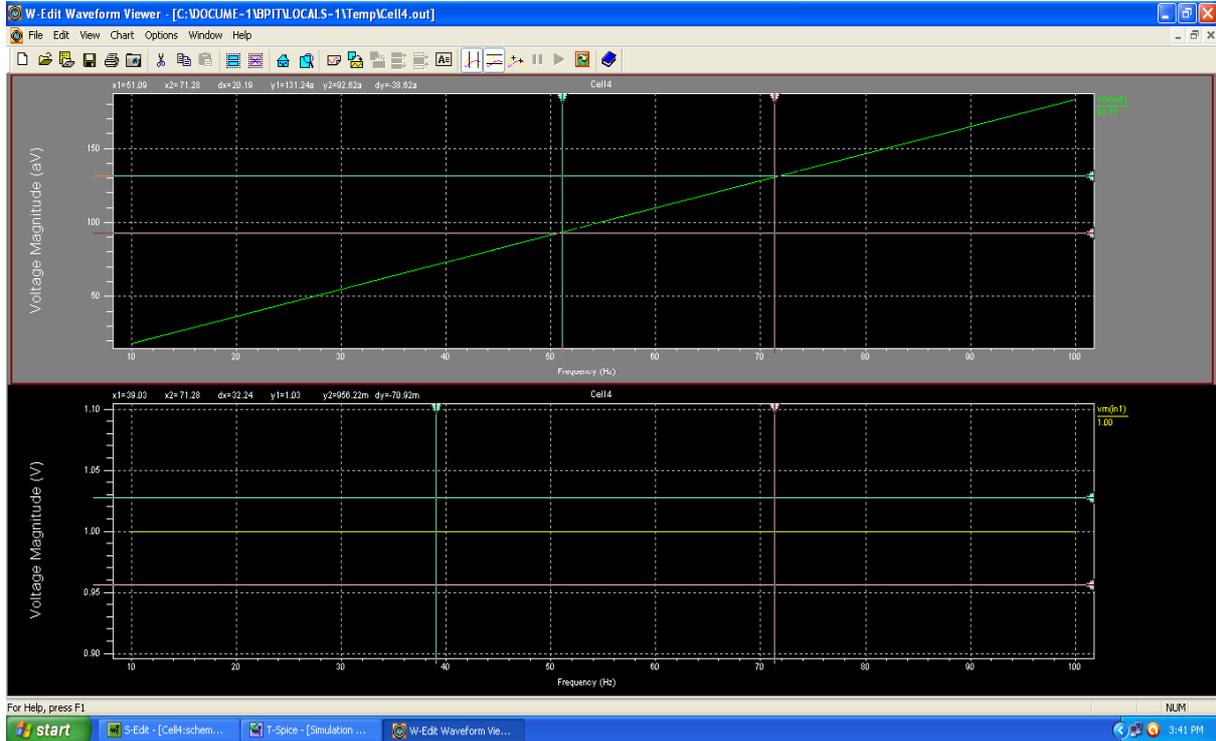


Figure 10. Output waveform of device using simulated inductor.

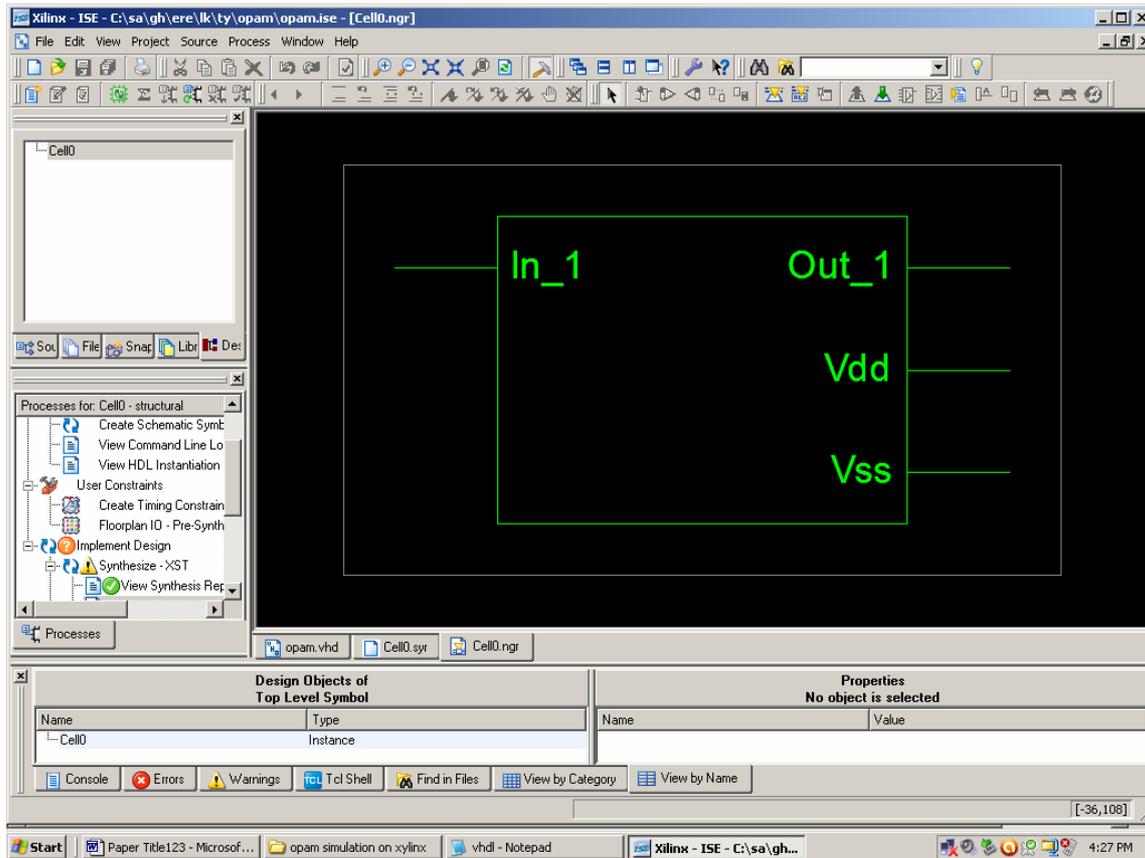


Figure 11. RTL diagram of device.

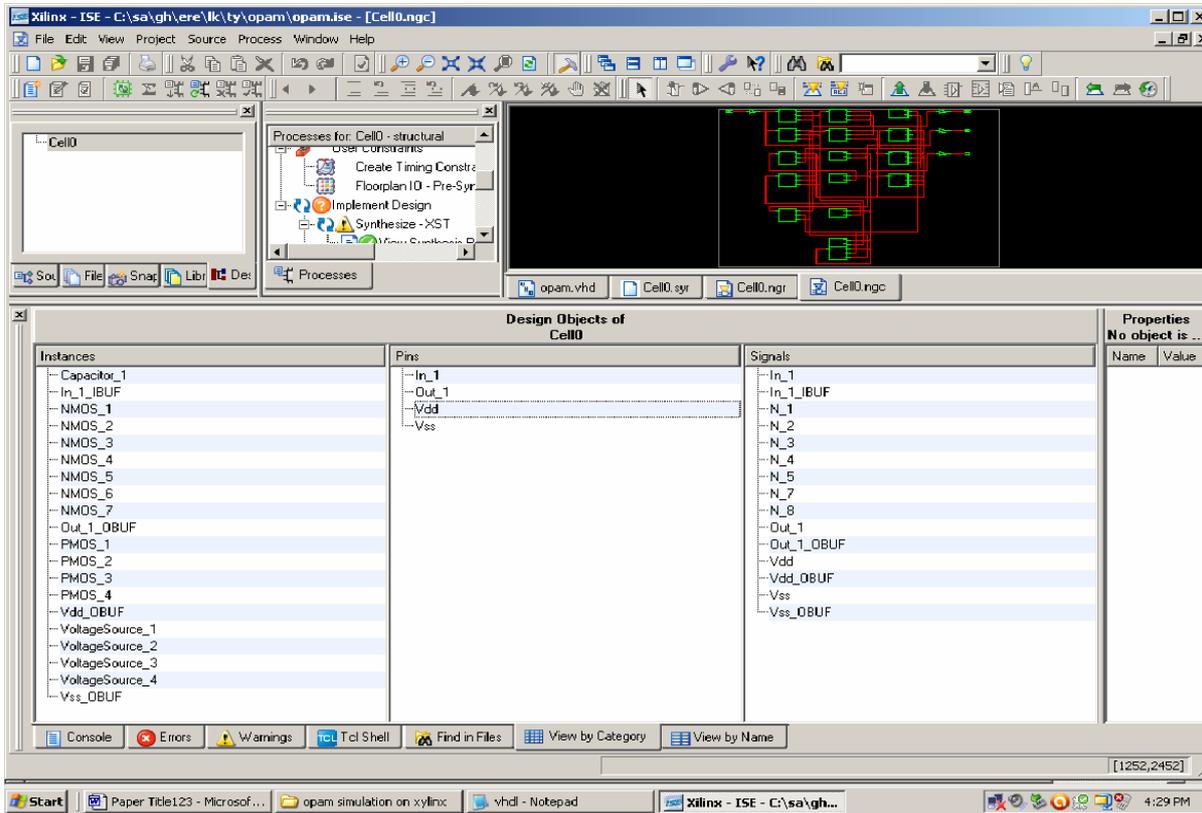


Figure 12. Objects used in the device.

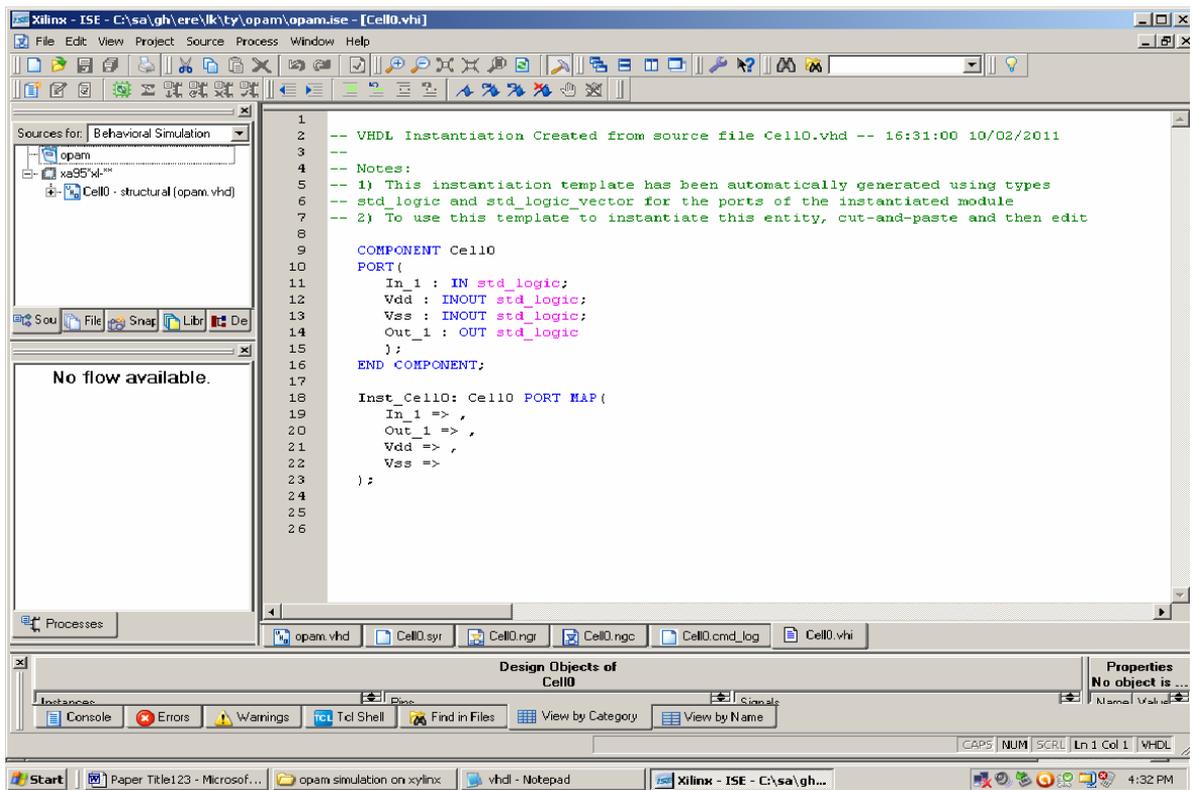


Figure 13. VHDL instantiation created from source file.

Table 1. Transient analysis.

Time<s>	V(in 1)<V>	V(out)<V>
0.000000e+000	0.0000e+000	0.0000e+000
1.250000e-010	1.2500e-001	9.5606e-002
6.786460e-010	6.7865e-001	5.4378e-001
9.554690e-010	9.5547e-001	7.8071e-001
1.093880e-009	1.0939e+000	8.39976e-001
1.316775e-009	1.3168e+000	1.0922e+000
1.600582e-009	1.6006e+000	1.3394e+000
1.922991e-009	1.9230e-000	1.6229e-000
2.303210e-009	2.3032e+000	1.9608e+000
2.758169e-009	2.7582e+000	2.3703e+000
3.296876e-009	3.2969e+000	2.8964e+000
3.931074e-009	3.9311e+000	3.4780e+000
4.678083e-009	4.6781e+000	4.2192e+000
5.000000e-009	5.0000e+000	4.5821e+000

Table 2. Device process parameters.

Process Parameters	
Power Supply	5 V
Load Regulation	3.93
Line Regulation	0.6 m
Current Range	1 μ A - 50 μ A
Average Power Consumed	13 μ W
Max power	16 μ W

5. Conclusions

A new slew rate enhancement (SRE) circuit which is targeted for ISFET driving with large capacitive load has been presented in this paper. In the proposed design, the device is free from interference effects and seen consuming much low power, in order of 13 μ W. There is the significant improvement in the slew rate when a simulated Inductor is placed parallel to the load at the output. The output is highly linear, indicating that the device is stable. Both simulation and power results obtained on Xilinx ISE 10.1 and Tanner Tool-15 justify a significant improvement in slew rate and power consumption by using the proposed SRE circuit.

6. Future work

This study can be extended and more improvement in

terms of power and size can be achieved at layout level and thus more effective results can be obtained.

7. References

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Appendix

Synthesis file

Release 10.1 - xst K.31 (nt)

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--> Parameter TMPDIR set to C:/Users/Project Lab Server/PASWAN/WEW/GH/xst/projnav.tmp

Total REAL time to Xst completion: 1.00 secs

Total CPU time to Xst completion: 0.13 secs

--> Parameter xsthdpdir set to C:/Users/Project Lab Server/PASWAN/WEW/GH/xst

Total REAL time to Xst completion: 1.00 secs

Total CPU time to Xst completion: 0.13 secs

--> Reading design: Cell0.prj

Synthesis Options Summary

---- Source Parameters

Input File Name : "Cell0.prj"

Input Format : mixed

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "Cell0"
Output Format : NGC
Target Device : Automotive 9500XL

---- Source Options

Top Module Name : Cell0

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Mux Extraction : YES

Resource Sharing : YES

---- Target Options

Add IO Buffers : YES

MACRO Preserve : YES

XOR Preserve : YES

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Library Search Order : Cell0.lso

Keep Hierarchy : YES

Netlist Hierarchy : as_optimized

RTL Output : Yes

Hierarchy Separator : /

Bus Delimiter : <>

```
Case Specifier      : maintain
Verilog 2001       : YES
---- Other Options
Clock Enable       : YES
wysiwyg           : NO
```

=====
* Final Report *
=====

Final Results

```
RTL Top Level Output File Name : Cell0.ngr
Top Level Output File Name     : Cell0
Output Format                   : NGC
Optimization Goal              : Speed
Keep Hierarchy                 : YES
Target Technology               : Automotive 9500XL
Macro Preserve                 : YES
XOR Preserve                   : YES
Clock Enable                   : YES
wysiwyg                       : NO
Design Statistics
# IOs                          : 4
Cell Usage :
# IO Buffers                   : 4
# IBUF                         : 1
# OBUF                         : 3
# Others                       : 16
# Capacitor                    : 1
# NMOS                        : 7
# PMOS                        : 4
# VoltageSource                : 4
```

```
=====  
Total REAL time to Xst completion: 3.00 secs
Total CPU time to Xst completion: 2.50 secs
Total memory usage is 166132 kilobytes
Number of errors : 0 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)
```

Power Analysis

```
* T-Spice 13.02 Simulation Fri Oct 07 15:57:37 2011
C:\DOCUME~1\BPIT\LOCALS~1\Temp\Cell4.sp
* Command line: tspice -o
C:\DOCUME~1\BPIT\LOCALS~1\Temp\Cell4.out
C:\DOCUME~1\BPIT\LOCALS~1\Temp\Cell4.sp
* T-Spice Win32 13.02.20080516.01:34:09
```

TRANSIENT ANALYSIS

Time<s>	v(in1)<V>	v(out)<V>
0.000000e+000	0.0000e+000	0.0000e+000
1.250000e-010	1.2500e-001	9.5606e-002
6.786460e-010	6.7865e-001	5.4378e-001
9.554690e-010	9.5547e-001	7.8071e-001
1.093880e-009	1.0939e+000	8.9976e-001
1.316775e-009	1.3168e+000	1.0922e+000
1.600582e-009	1.6006e+000	1.3394e+000
1.922991e-009	1.9230e+000	1.6229e+000
2.303210e-009	2.3032e+000	1.9608e+000
2.758169e-009	2.7582e+000	2.3703e+000
3.296876e-009	3.2969e+000	2.8694e+000
3.931074e-009	3.9311e+000	3.4780e+000
4.678083e-009	4.6781e+000	4.2192e+000
5.000000e-009	5.0000e+000	4.5821e+000

* BEGIN NON-GRAPHICAL DATA

Power Results

vdd from time 0 to 5e-009

Average power consumed -> 1.304338e-005 watts

Max power 1.635414e-005 at time 5e-009

Min power 0.000000e+000 at time 0

* END NON-GRAPHICAL DATA*

* Parsing	0.00 seconds
* Setup	0.01 seconds
* DC operating point	0.00 seconds
* Transient Analysis	0.01 seconds
* Overhead	1.20 seconds

* -----

* Total 1.23 seconds

* Simulation completed with 1 Warning

* End of T-Spice output file