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Review of the Global Trend of Interconnect Reliability for Integrated Circuit

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Abstract

Interconnect reliability has been regarded as a discipline that must be seriously taken into account from the early design phase of integrated circuit (IC). In order to study the status and trend of the interconnect reliability, a comprehensive review of the published literatures is carried out. This can depict the global trend of ICs' interconnect reliability and help the new entrants to understand the present situation of this area.

Keywords

Integrated Circuit, Interconnect Reliability, Interconnect Modeling, Interconnect Process

1. Introduction

Nowadays, the wireless communication industry has revolutionized the whole society, from satellite transmission, radio and television broadcasting to the ubiquitous mobile telephone. All these revolutions all need plenty of integrated circuits (ICs) which are a set of electronic circuits on one small plate ("chip") of semiconductor material. Modern ICs can be made compactly by incorporating up to several billions of transistors and other electronic components in an area of about 1 cm^2. With the advent of 4 G era, the frequency and current density of IC increase dramatically, which can lead to the increase of IC failure. Hence, the IC reliability increases significantly as our reliance on electronic products has increased tremendously in our daily lives. Furthermore, all the transistors and components have to be electrically interconnected to provide the proper functionality in ICs. Interconnect reliability has attached increasing importance, especially when the line width becomes narrower that renders high current density as shown by Srinivasan [1]. As the IC undergoes the continuous downscaling

according to the Moore's law [2], interconnect reliability has become crucial and affected the performance, power consumption and reliability of the whole circuit [3]. Especially, the interconnect reliability of IC can directly determine the quality of communication.

Furthermore, to tackle the challenge of interconnect reliability, there are several reviews about interconnect reliability from different aspects. For example, Jeng *et al.* presented a broad overview on the reliability research of nanotechnology and highlighted the importance of interconnect reliability [4]. Hu *et al.* reviewed the goals and constraints of MOSFET scaling, highlighting the role of reliability constraints [5]. Meanwhile, as to the research on reliability modeling and simulation, please refer to the works on EM by Tan *et al.* [6] [7]. Havemann reviewed the high-performance interconnects [8]. Soden discussed the role of IC failure by reviewing the new techniques and tools [9]. However, these reviews are confined in specific field without the status and analysis systematically of the overall trend. In order to understand the present situation and trend of interconnect reliability, a comprehensive review is necessary. Especially, a brief history and the future trend of interconnect system are summarized by some statistic surveys. All these can provide important guidance for the new researchers of this area.

This paper is arranged as following: the status and globalization trend of the interconnect reliability by statistical survey on more than 1000 papers during the last four decades are given in Section 2. The trends of interconnect modeling and interconnect process are illustrated in Sections 3 and 4, respectively. Finally, the challenge and prospect on the interconnect techniques are addressed in Section 5.

2. Statistical Survey Analysis

Over the past 40 years, the research on IC interconnect reliability has experienced several large fluctuation and become more attractive. The status and tendency are analyzed by reviewing the academic papers here. In this paper, the statistic data are taken from the related journals or magazines and conferences from 1969 to 2017. The review covers the following journals, like IEEE Transactions on Reliability, IEEE Transactions on Device and Material Reliability, Microelectronics reliability, Applied Physics etc, which are the top reliability journals based on the IC reliability. Similarly, the conferences include IEEE International Reliability Physics Symposium Proceedings, Integrated Reliability Workshop Final Report (IRW), IEEE International Physical and Failure Analysis of Integrated Circuits, Reliability and Maintainability Symposium (RAMS) Annual and some other related forums.

Figure 1 shows the research trend by the statistics of the total papers from 1969 to 2017. The blue curve indicates that the number of papers has kept upward year by year, even there is little fluctuation. This trend agrees well with the development of semiconductor industry and electronic market. It also can be illustrated by the

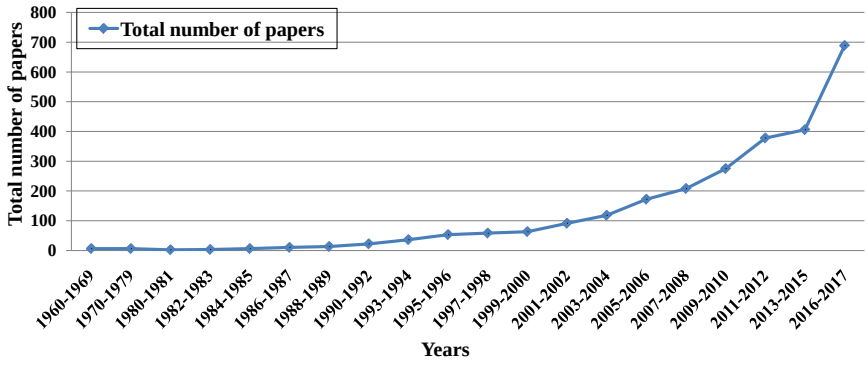

Figure 1. The paper trend of IC interconnect reliability.

truth that with the turn up of the very large scale integration (VLSI) in the late 80s, the industrial community started to pay more attention to IC reliability and the number of papers increased slowly. In the 90s, the mobile communication industry outburst and the ultra large scale integrated (ULSI) arose. The researchers turned more attention to interconnect reliability and the papers increased continuously. It also can be observed that the number of papers increased significantly from 2000 to 2017. Especially, the number in 2014 was 450% over that of 2000. Therefore, the research continues to be attractive in the next few years.

The paper distribution is shown in **Figure 2** through reviewing papers of journal or magazine and conference respectively. It is shown clearly that the overall trend is upward. From 1986 to 1994, the number of journal or magazine papers was more than that of conference. Since 1995, the number of conference papers has exceeded that of journal or magazine in the same period. The trend can be illustrated by the fact that the international communication became frequent after 2000, therefore the researchers started to exchange their progresses and cooperate by attending some related meetings. In general, the research spot is always changing closely with the industry development and market demands. Furthermore, the trend of CMOS technology node with physical gate length is shown in **Figure 3**, which can demonstrate that the COMS technology node is identical with the development of electronic market. In turn, electronic market is closely following with the development of the semiconductor industry.

At the same time, a large amount of universities and companies have engaged in the research of interconnet reliability. The paper distribution of university and company during 1960 to 2017 is depicted in **Figure 4**. This trend can be illustrated that due to the widely attention of industrial community, papers from company occupied the majority part at the begining. Then, with the rapid IC development, the academic community started to turn their attention to interconnect reliability. Therefore, papers from university increased significantly and even surpassed that of company from 1993.

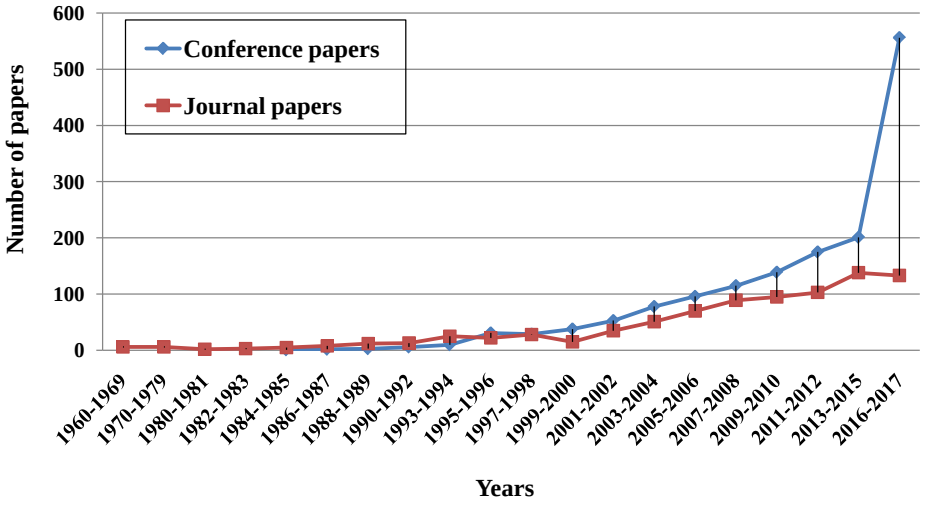

Figure 2. The trend of journals and conference papers.

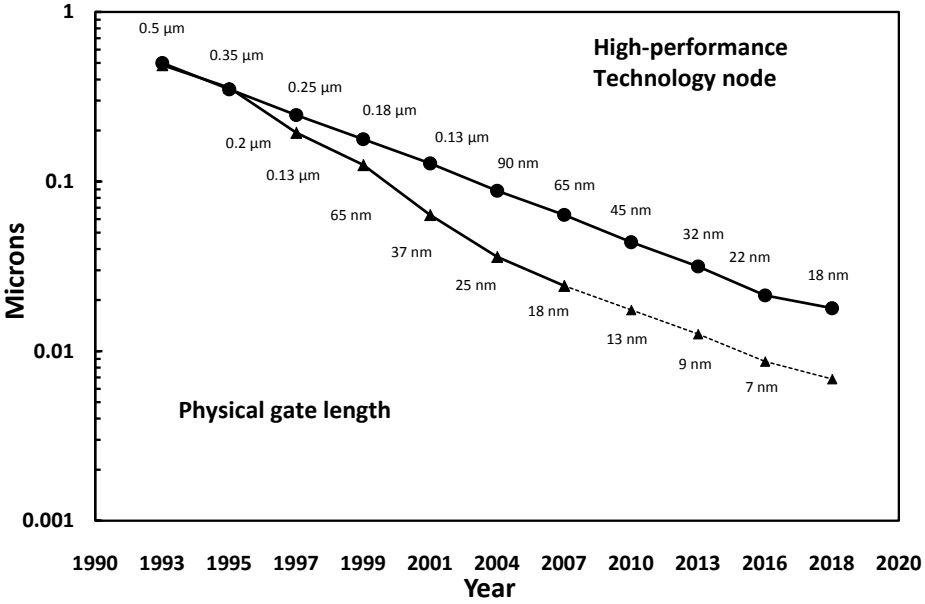

Figure 3. CMOS technology node vs. physical gate length.

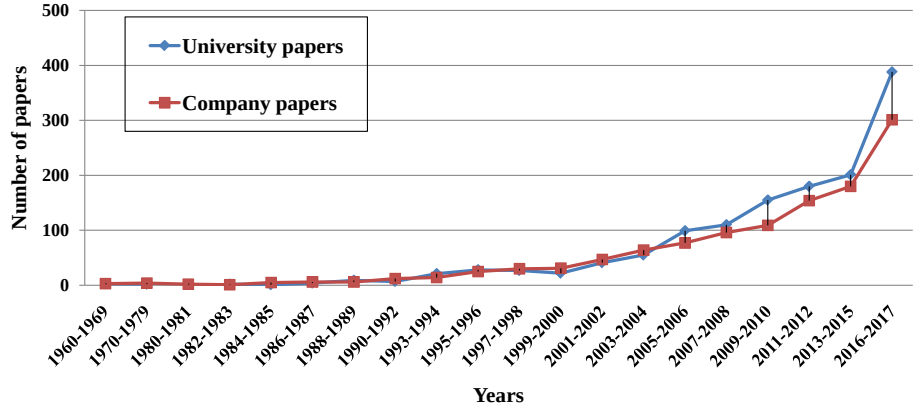

Figure 4. The trend of the company and university papers.

In a broad sense, IC reliability can be divided into five types which include the interconnect reliability, device reliability, circuit-level reliability, ESD reliability and others. **Figure 5** depicts the distribution of these types. It is observed that interconnect reliability accounts for 38% of the whole field and shows an increasing trend year by year. Moreover, interconnect failure has become the main problem for IC reliability nowadays.

Nowadays, with the achievement of industry internationalization, the frequent competition and cooperation between countries, enterprises, institutes or universities have been greatly enhanced. Even in order to solve the key technology problem, the original competing companies started to cooperate each other. The trend of cooperation is proceeding apace and becomes widespread. Moreover, according to the number of authors, the papers also can be graded into multi-author and single author. By widespread statistic, the papers were composed by single author from 1960 to 1983. At that time, the communication was just confined within campus or single company. Since 1994, with the rapid rise of 2G which promoted the development of electronic market, increasing universities and companies started to cooperate. However，the majority of cooperation was between two companies in one country. From 2001 to 2012, the papers composed by multi-author had an increase of 300% above that of 1970 to 1985. The cooperation trend of cooperation across affiliations is shown in **Figure 6**. It can be shown that the multi-author cooperation has become widespread.

Furthermore, the papers can be classified into six categories according to the location of author's laboratory or company. The papers distribution in different regions is depicted in **Figure 7**. It can be seen that the papers published by America kept ahead all the time from 1969 to 1980. After 90's, the research appeared a shift trend that America was still in the leading status and the papers from Europe and Asia-Pacific increased dramatically. From 1995, the globalization trend became more popular. The yellow curve indicates that the number of papers from Asia-Pacific is increasing linear. It can be illustrated that since 70's Asia was the install base for semiconductor industry, because the wafer process industry and package technique started from here. Now the increase from Asia-pacific is becoming prominent, especially the semiconductor industry has made substantial progress in Japan. Into the 21st, the corporation groups keep high enthusiasm on interconnect reliability and the number remains relatively high level.

In a word, the research of interconnect reliability has received more attention year by year with widely cooperation. The papers of conference and multi-author are becoming popular. America is still the mainstream with the rapid rising in Asia-Pacific. All these indicate that interconnect reliability has become the focus to IC reliability [10] [11]. In order to study the interconnect reliability deeply, the trends of interconnect modeling and process are given as follow.

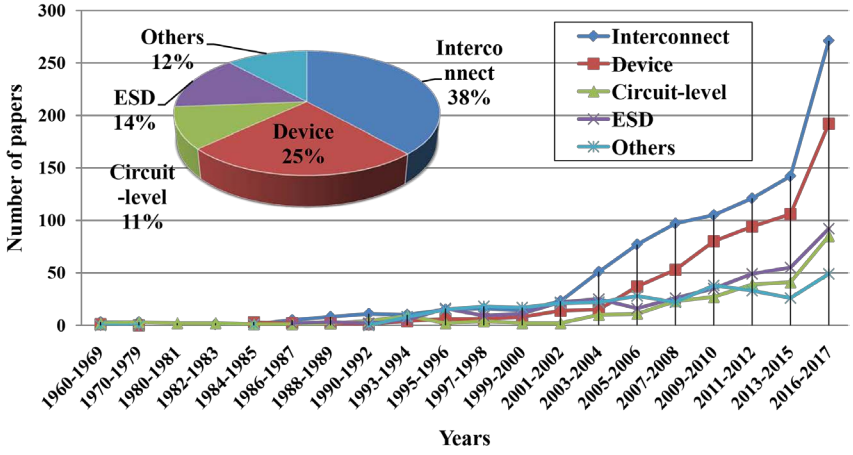

Figure 5. The distribution of different types of IC reliability.

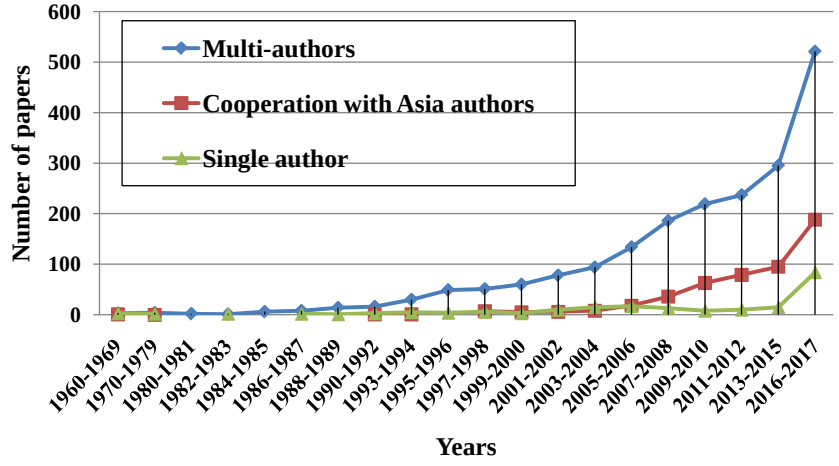

Figure 6. The trend of cooperation across affiliations.

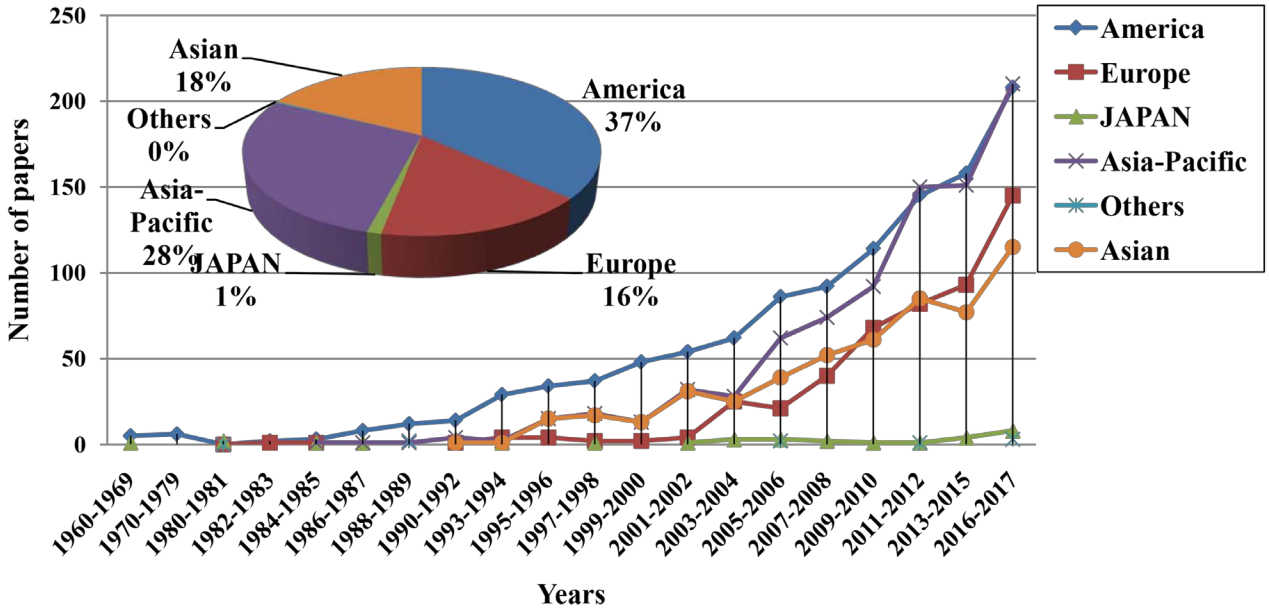

Figure 7. The distribution of papers of different regions.

3. Trend of Interconnect Modeling

In order to model the interconnect failures, accurate modeling and powerful simulation are the most effective methods. Considerable research on interconnect modeling have been carried out to simulate the failure. For instance, Dimagiba, *et al.* reviewed the first level interconnect modeling methodology [12]. Tan, *et al.* utilized the finite element modeling (FEM) to analysis electro-migration (EM) for narrow interconnects [13]. The interconnect modeling trend is summarized in **Figure 8**, it can be concluded that model is developed from physics-based model to failure model, from physical phenomena to essence origin. To cater for the temperature and thermo-mechanical stress effects, as well as other factors, the model has developed and improved from 1D to 2D and finally to 3D. It is worth to mention that in the 1960s to the early 70s, there was a climax of EM modeling. The first interconnect model was proposed by Black and known as the simple empirical model in 1967 which depicted the EM physical phenomena [14]. The first EM model was proposed by Huntington and Fiks which was known as the ballistic model [15]. Then, in order to limit current crowding, the 2D model emerged [16]. As most physical system can be described based on a set of partial differential equations, FEM is evolved to be a effective tool in solving these partial differential equations and obtaining solutions that represent the

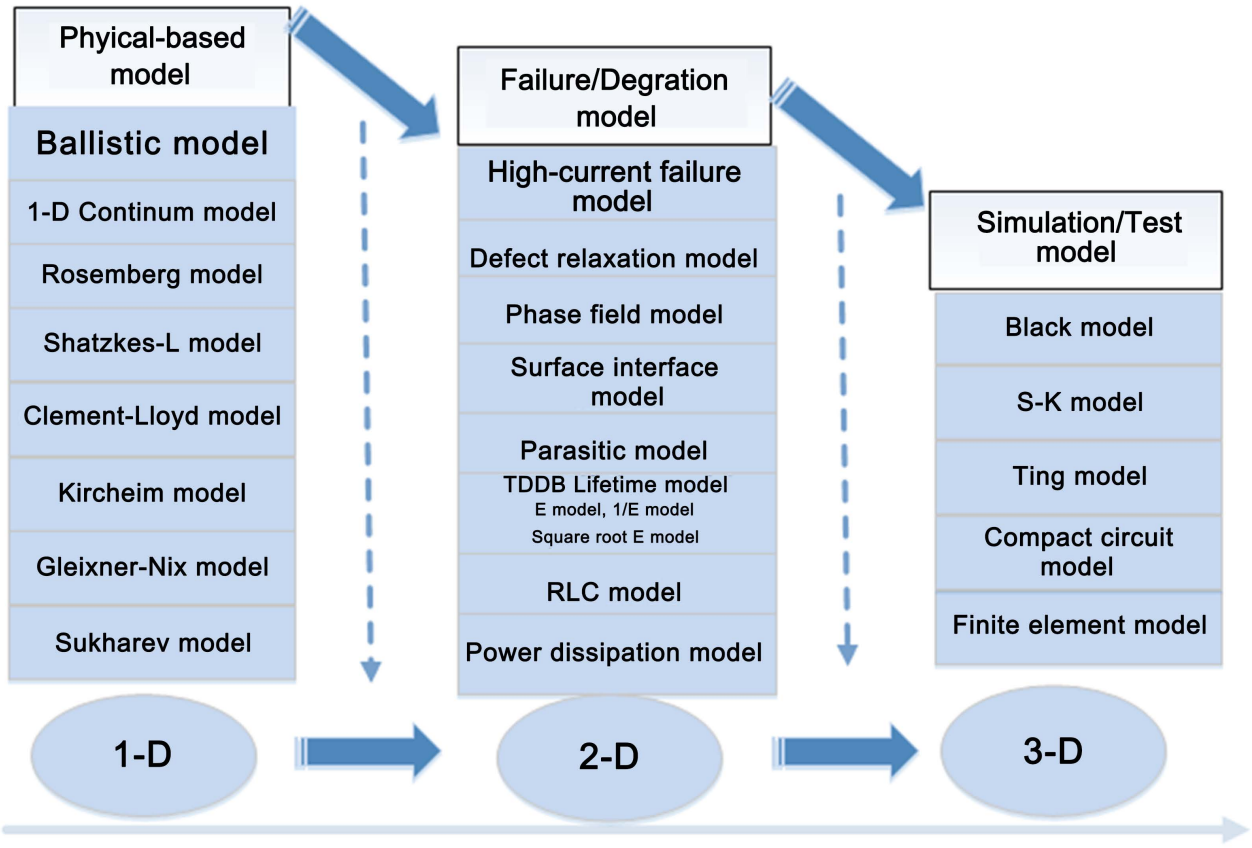

Figure 8. The interconnect modeling trend.

physical process of degradation of interconnect system [17] [18] [19]. Furthermore, considering the joule heating and coupling effect, Rzepka *et al.* provided a pioneer work to combine various driving forces using finite element analysis(FEA) in 1999 [20]. However, 2D modeling was also unable to represent the geometry of the whole circuit due to layers overlapping. Moreover, the studies were based on Al interconnect without considering void growth. With the scaling of the interconnect dimension and the increase in the number of metal layers, it becomes increasingly difficult to achieve the efficient simulation using 2D model. Therefore, the 3D model considering all the factors is needed. In 2001, Dalleau and Weide-Zaage developed a FEA model for EM simulation from the perspective of driving forces considering dynamic void growth [21]. They developed the FEM to predict the EM voids, in which three mechanisms including EM, thermo-migration(TM) and stress migration(SM) were considered [22]. Later, Tan *et al.* used FEM to finish 3D modeling analysis for simple circuit [23]. Nowadays, it is popular to construct 3D model combining FEM to analysis EM [24] [25].

All the available models can reflect the evolution and state of the art for interconnect modeling [26] [27]. However, the modeling analysis in complicated circuit has not been studied, which is the next spot in future. That is to say, reliability modeling for complicated IC is urgent for us with the development of CMOS technique.

4. Trend of Interconnect Process

Nowadays, the advanced manufacture techniques enable a direct observation of the influence of process changes on the IC interconnect reliability. The decrease of feature size introduces random process changes which mainly come from pollution, environmental variation and high temperature [28]. It brings the variation of IC physical structure and degradation of the circuit performance.

The changes of different processes are summarized in **Figure 9**. It can be observed that Al interconnect process is the dig to etching technique and interconnect is etched on Al film [29]. The process steps include etching, sputtering, exposure and cleaning [30]. Cu interconnect process was developed by IBM in 1985. Because it is difficult to etch for Cu, the double embedded technology, namely DD process, which includes oxidization, doping, deposition, printing, sputtering, electroplating, chemical mechanical polish (CMP), annealing and so on [31]. Photolithography is to carve micro holes and grooves on silica after precipitation. Sputtering is to make barrier layer (TaN/Ta) which can enhance the adhesion with Cu. The main purpose of electroplating is to make Cu film dense, no crack, no void and no defect. The CMP is the flattening treatment which is carried out on Cu layer and the main intention is to flat the surface and remove the morphology caused by deposition and etching [32]. It is used for global planarization and affords limited depth in optical lithography with the increasing interconnect level. Annealing is used to release stress and make grain uniform

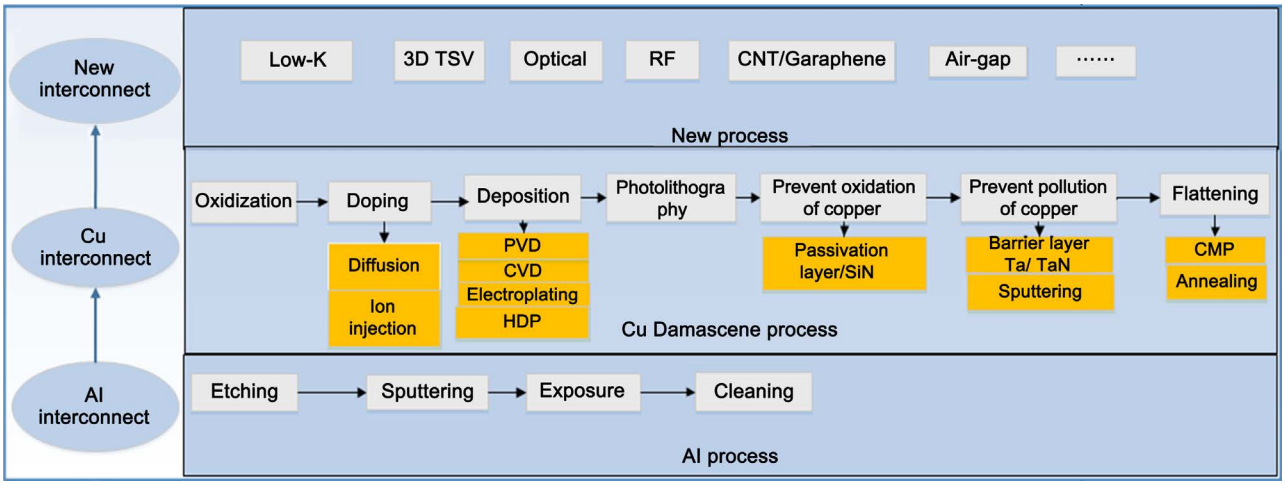

Figure 9. The changes of interconnect process.

distributed. Especially the DD process deposits interconnect and hole at the same time, which would further reduce the process steps, time and cost. Physical vapor deposition (PVD) is used for adhesion or barrier layers. Chemical vapor deposition (CVD) is used for contacts, vias and inter-dielectric. High density plasma (HDP) deposition is used to improve the capability of gap-filling. It is worth been mentioned that CMP and DD can achieve the graphic processing for Cu interconnect. The barrier layer (TaN) is used to solve the problem of Cu pollution and the passivation layer (SiN) is used to prevent Cu being oxidized.

It should be pointed out that the serious process changes due to the deviation of non-ideal characters must be considered in circuit-level interconnect optimization [33]. It is difficult to predict and control the parasitic coupling effect which is caused by process changes. Cu DD as well as low-k material is proposed as the possible solution. Consequently, the integration of new materials, graphic through-hole, chip planarization have become serious challenges for interconnect process.

5. Challenges and Prospects

In recent decades, the technology of semiconductor has made great progress driven by the various application demands. In 90 nm node, the interconnect delay has exceeded gate delay, which shows that IC has developed from the transistor era into the interconnect era [34]. As reviewed in the previous sections, some interconnect methods are developed, especially for high power, large-signal and high frequency applications. However, the requirement for interconnect reliability is stricter than in the past. The modern interconnect reliability is faced with more challenges.

In the near term, the most difficult challenge for interconnect is the introduction of new materials to meet the targets of technology and reliability. The new material with better electrical conductivity and lower dielectric constant simultaneously is needed [35]. In addition, in order to enhance conductor feature and

dielectric character, new materials and methods are continuously to be attempted, such as using the cooled metal, superconductor metal as interconnect materials and using optical or biology as interconnect dielectrics. In the long term, the impact of scaling down on interconnect must be mitigated. To design the reasonable interconnect structure is the pursuit of goals in future.

Furthermore, with the development of semiconductor technology, the higher requirements for interconnect technology and process are needed. Technologies must catch up with the exploitation of new materials and new methods. In order to keep continuous development, it needs to develop higher performance of interconnect technology which not only has larger breakthrough in material, but also innovates the interconnect structure. For instance, TSV technology is used in 3D interconnect to shorten the distance between lines. The asynchronous interconnect architecture has replaced the synchronous architecture. However, a massive reformation is still needed.

Meanwhile, in the deep sub-micron era, physical properties of interconnect lines would cause some restrictions, such as long transmission delay, low bandwidth and high power consumption etc. At the same time, the material may reach the physical extremity in one day. For example, the width restriction of silicon processing is 10 nm and it is difficult to produce the products with stable performance and high integration. When the feature size is approaching the physical extremity, electronic transition happens and results in the deadly leakage current. Meanwhile, the increase of integration density would lead to a sharp increase in cost. In addition, the transistor which is used as switch would generate enough heat to burn itself, thus IC will face the problem of power dissipation. Even the technology and physical problems can be solved finally, the increase of interconnect delay and performance degradation are not inhibited completely.

Therefore, in order to solve these problems and become compatible with existing semiconductor process, new innovation technology which can break the traditional limit should be proposed. Furthermore, it is reported that More-than-Moore is no longer to pursue the advancement of technology node costly, it can impulse comprehensive innovation and lead to fundamental changes in development of ICs. All these can give some important guidance for the new researchers to understand the present situation of this area.

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