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28-nm UTBB FD-SOI vs. 22-nm Tri-Gate FinFET Review: A Designer Guide—Part II

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Abstract

This is Part II of a two-part paper that explores the 28-nm UTBB FD-SOI CMOS and the 22-nm Tri-Gate FinFET technology as the better alternatives to bulk transistors especially when the transistor's architecture is going fully depleted and its size is becoming much smaller, 28-nm and above. Reliability tests of those alternatives are first discussed. Then, a comparison is made between the two alternative transistors comparing their physical properties, electrical properties, and their preferences in different applications.

Keywords

UTBB FD-SOI: Ultra-Thin Body and Box Fully Depleted Silicon on Insulator, Tri-Gate FinFET, DIBL: Drain Induced Barrier Lowering

1. Introduction

The downscaling of bulk silicon transistors, of about 28-nm and below, increases the leakage current and reduces the performance. A solution was introduced to overcome those challenges while continuing downscaling the transistor's geometry using the following alternatives: UTBB FD-SOI and Tri-Gate FinFET. Both transistors share CMOS technology with a fully depleted transistor architecture but make the transistor a better switch.

2. Reliability Test for UTBB FD-SOI and Tri-Gate

The drop in performance of a CMOS transistor is mainly attributable to two mechanisms: The Hot Carrier Injection (HCI) and the breakdown of the gate oxide TDDB.

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When a transistor is subjected to a high drain-source voltage V_{DS}, the drain current I_{DS} decreases over time. Too strong electric field can cause an avalanche current and then destruction of the SiO_2-Si interface. In UTBB FD-SOI technologies, the electric field is much lower [1]. The HCI stresses, including $V_g = V_d$ stress, have been performed at 125˚C. Forward saturation current (I_{dsatF}) degradation is reported at stress conditions as well as projected degradation at operating voltage, is compared to degradation model from bulk 28-nm process, for comparable I_{ON}. It is found that HCI degradation is slower for 28-nm UTBB FD-SOI than 28-nm bulk **Figure 1** at same I_{ON}. Another stress test is done to see the effect of body bias voltage, exhibit accelerated I_{dsatF} degradation in FBB and reduced degradation in RBB **Figure 2**. As a result, the hot carrier-related effects are much less critical than the Bulk technology [2].

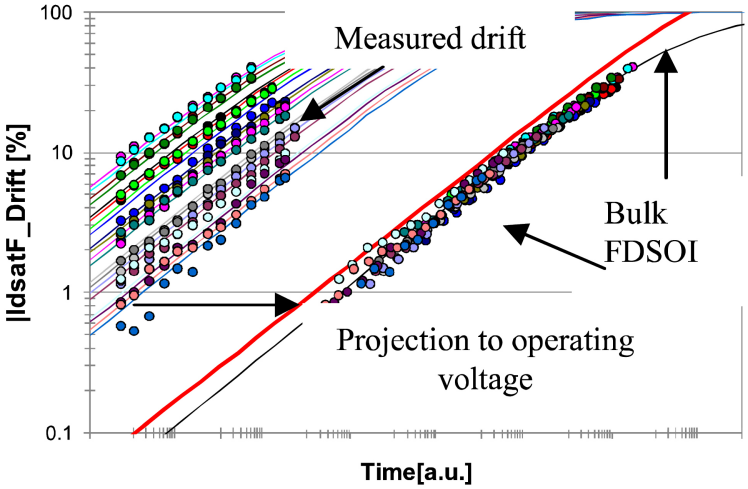

Figure 1. Measured (symbols) and modeled (lines) I_{dsatF} drift as function of time for various stress voltage and operating condition for 28-nm UTBB FD-SOI, compared to 28-nm bulk (redline) [2].

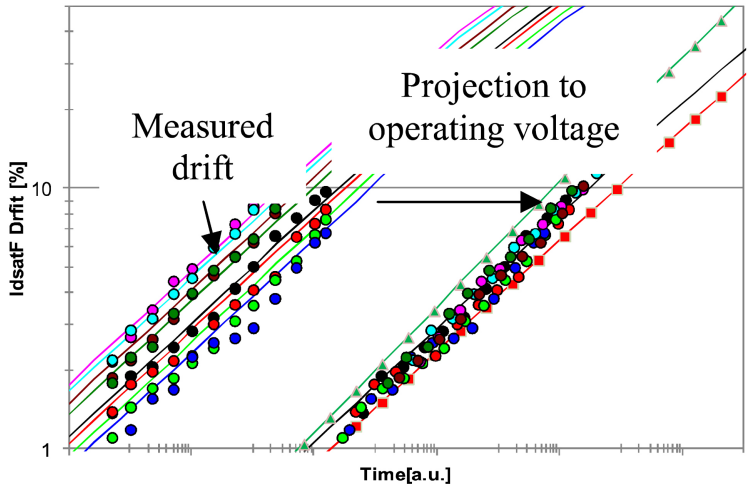

Figure 2. Measured (symbols) and modeled (lines) I_{dsatF} drift for various stress voltage and projected to operating voltage for V_{BB} = 0 (black line), RBB (squares) and FBB (triangles) [2].

An HCI test is also done on the 22-nm Tri-Gate FinFET and on 32-nm planar FET, the result is shown in **Figure 3** [3]. The Figure shows that the 22-nm technology has much lower degradation than that of 32-nm at low drain biases. At higher drain bias, an increased fraction of total degradation from hot carrier is apparent, but the total is still lower than in the planar 32-nm planar FET technology. The increased fraction of hot electron degradation is related to the channel length reduction in 22-nm versus 32-nm, doping profiles [4], and the Tri-Gate architecture.

When very high voltages are applied between the drain and the gate of a transistor, a conductive path can be formed through the gate oxide. This phenomenon is called the breakdown of the gate-oxide (TDDB). The percolation model [5] detailed in **Figure 4** makes it easy to explain the formation of the conductive path. When a high voltage is applied to the gate, traps are created in the gate-oxide. As soon as enough traps have emerged, a conductive path is formed between the drain and the gate.

A TDDB test is done on 28-nm UTBB FD-SOI and 28-nm Bulk transistor, the results have similar slopes for same equivalent oxide thickness as shown in **Figure 5**.

A TDDB test is done on the 22-nm Tri-Gate FinFET and on 32-nm planar FET. For PMOS, the 32-nm indicates slightly more intrinsic robustness over the 22-nm as shown in **Figure 6**. While for NMOS, the 22-nm technology is improved over the 32-nm technology as shown in **Figure 7**. The benefit largely

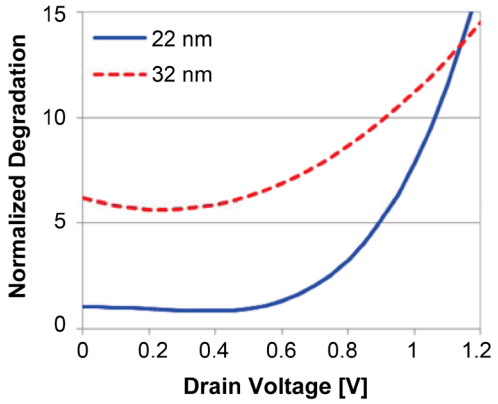

Figure 3. Overall N-FET degradation [3].

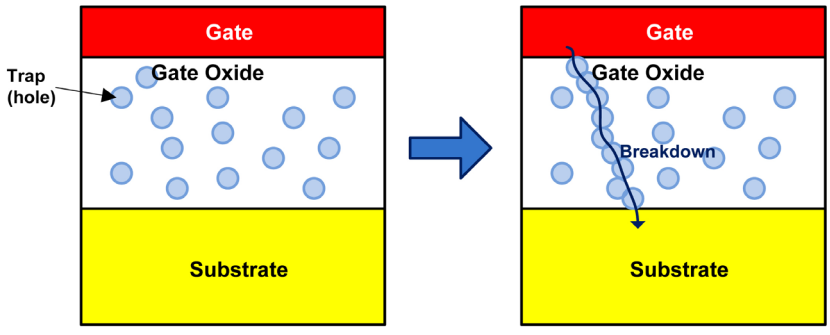

Figure 4. TDDB mechanism.

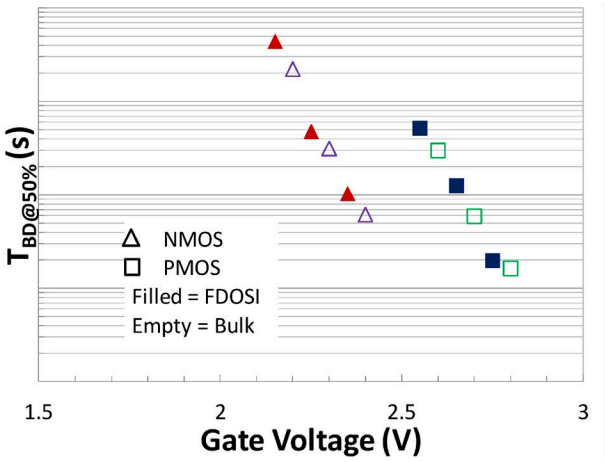

Figure 5. Time to breakdown as function of V_g, UTBB FD-SOI vs Bulk [2].

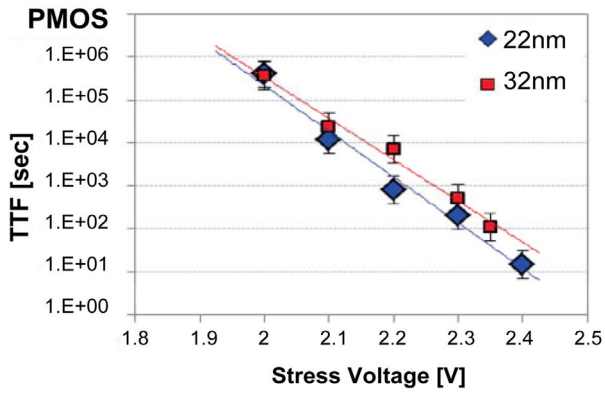

Figure 6. PMOS TDDB test result [3].

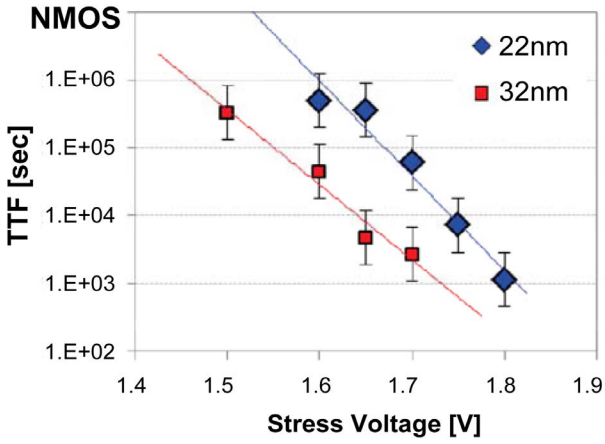

Figure 7. NMOS TDDB test result [3].

comes from the ability to tune the metal gate work function to more mid gap, which reduces the field across the oxide.

3. 28-nm UTBB FD-SOI VS 22-nm Tri-Gate FinFET

Both UTBB FD-SOI and Tri-Gate FinFET share CMOS technology with a fully

depleted transistor architecture where any additional voltage to the gate generates charges which make the transistora better switch. As a result, lower supply and threshold voltage give much lower dynamic power dissipation. The sections below compared the physical and electrical characteristics of both transistors, and then make an analysis to determine which is more appropriate in analog and digital applications.

3.1. Individual Transistor Comparison

3.1.1. Electrostatic

The Tri-Gate FinFET have better electrostatics (DIBL and SS) and higher drive current per unit area but higher leakage current; A comparison summary is shown in **Table 1** [6] [7] [8].

3.1.2. Capacitance

The UTBB has lower gate capacitance and less effective capacitance than that of the Tri-Gate, which makes the UTBB FD-SOI capable to work on higher frequency. For example, at the point where UTBB and Tri-Gate have an I_{on} (+30%) more than that of the bulk transistor of I_{ON} = 900 μA/μm, the gate capacitance of the UTBB transistor still constant while the Tri-Gate width transistor is increased by 30% and the gate capacitance by 30% [9]. Then, the very high effective drive current per sq μm of the Tri-Gate FinFET is mitigated somewhat by the higher parasitic capacitances, especially with the multiple fins common gate transistor.

3.1.3. Random Dopant Fluctuations

The UTBB is undoped channel device so it is better in lowering the random dopants fluctuations (drops by ×3.3 [9]) and better device matching because the Tri-Gate needs low fin doping (fluctuations drops by ×1.8 [9]) and as the height of the fin increases, the dopants fluctuations are increased too [10]. Also, there is a mismatch between the neighbor fins [11].

3.1.4. Flexibility

The UTBB is more flexible and have more management over speed and power because of the Body Bias technique which offers a threshold voltage control [12] while Tri-Gate has no body bias [13].

Table 1. DIBL, SS, ION, and IOFF comparison between Tri-Gate FinFET and 28-nm UTBB.

	28 nm UTBB of T_{soi} = 7 nm [6]		Intel 22 nm Tri-Gate FinFET [7] [8]	
	NMOS	PMOS	NMOS	PMOS
I_{ON} (μA/μm)	1070	610	1260 @ 0.8 V_{DD}	1100 @ 0.8 V_{DD}
I_{FF} (nA/μm)	16	30	100	
DIBL (mV/V)	90 - 95	90 - 95	46	50
SS (mV/dec)	85 - 90 @ 1 V V_{DD}		69	72

3.1.5. Sources of Variability

The sources of variability are the Tbox (buried oxide thickness) and Tsi (silicon thickness) in UTBB transistor while in Intel Tri-Gate transistor, the sources are the Hfin (fin height), Dfin (fin dimension), and Fin taper [14].

3.1.6. Fabrication Complexity

For fabrication, the Tri-Gate is more complex process which faced with the challenges of a disruptive approach that requires mastering technological processes compatible with tri-dimensional geometries (in terms of doping, etching, etc.) while the UTBB is much more in continuity with planar Bulk process and may be seen as a better choice of benefits vs. manufacturability trade-off than Tri-Gate FinFET [15] [16].

3.1.7. Cost

The cost is a major challenge facing chip manufacturers. Intel estimates that FD-SOI increases the added cost of a finished wafer by 10%, compared to 2% - 3% for Tri-Gate. But, Global Foundries said that 20% lower die cost and a 50% lower mask cost than Tri-Gate FinFET [17]. There is a point that the extra cost of SOI wafers is offset by cost savings made because no longer need to dope the channels, so the extra cost of the start wafer (SOI) is absorbed.

3.2. Transistor Characteristics in Chips

In a chip embedding billions of transistors, the characteristics of each transistor are not exactly the same. The main reason of this is the different quantity of dopants injected in the channel during manufacturing process. In UTBB FD-SOI, dopants usage is greatly reduced which limits the variability. As a result, the characteristics of each transistor are closer to the average. That allows the transistors to run faster since less margin need to be allowed for process variability. Tri-Gate FinFET has a bigger margin of variability because the complex process of the vertical Fin etching can't give the same Fins shape; that also leads to variant threshold voltage for each transistor.

Such comparisons [18] show that the UTBB FD-SOI is more suited for low power/low leakage applications than the Tri-Gate due to its efficiency at low power. However, the Intel Tri-Gate FinFET is more suited for the high performance (high power) application than the UTBB FD-SOI.

Nevertheless, designers should take also into consideration another factor the type of the circuit: analog, RF, digital, memories, etc.

3.3. For Analog and RF Blocks

Analog designers look for the gain, noise figure, flicker noise, mismatch, power capabilities and f_T/f_{MAX} (f_T: Maximum cut-off frequency, f_{MAX}: Maximum oscillation frequency). Tri-Gate FinFET can achieve significantly higher gain and lower flicker noise than planar-bulk and UTBB FD-SOI MOSFETs due to its superior electrostatic integrity, higher carrier mobility, and lower DIBL. However, gain is lower at higher frequencies due to large source/drain resistance, and the higher

parasitic capacitance (effective capacitance with miller component from region between FINs) limits the maximum frequency and raises the noise figure. Differently, the total dielectric isolation of the channel in the UTBB FD-SOI creates lower gate and source/drain capacitance, reduces source/drain leakage currents, and improves latch-up immunity. Additionally, the absence of channel doping and pocket implants in the fully depleted transistor produces lower noise specifications, lower mismatch, and increase the gain. UTBB FD-SOI has higher f_T/f_{MAX} than that of Tri-Gate FinFET due to reduced gate capacitance and raised-S/D (Source/Drain) epitaxy which reduced the access resistance {f_T of N(P): 300(260) GHz and f_{MAX} of N(P): 170(120) GHz [19]}. All these advantages, in addition to the large R_{ON}/R_{OFF} ratio, make UTBB FD-SOI more attractive and favorable to the designers of RF circuits such as: power amplifier, mixer, base-band amplifier, and low noise amplifier. The high gain and lower noise with high speed switch (due to lower parasitic capacitance) attract the analog circuits too. For example, the ADC will be smaller and higher speed, or the LNA will have higher gain and smaller noise figure. So, UTBB FD-SOI has higher success than Tri-Gate FinFET in analog and RF application [20] [21].

Global Foundries made a case study of smart watch which described as co-integrated circuit with low power and RF enabling in [17], where it has a CPU frequency of 1.5 GHz, operating voltage at 0.6 V, and an integration path of Bluetooth, and Wi-Fi with power management integrated circuit. The comparisons are done between 40-nm low power bulk transistor, 28-nm super low power bulk transistor, 28-nm UTBB FD-SOI, and Tri-Gate FinFET. It starts with the 40 nm device; it is interesting to see the battery life improvement over the 40 nm, 28-nm, 28-nm UTBB, and Tri-Gate FinFET as seen in **Table 2**. The battery life time is increased due to the power reduction at the ISO frequency, from 4.5 days to approximately 13.85 days with 109.7 mw/day where the Tri-Gate FinFET approaches 11.58 days with 131.2 mw/day. If the forward body bias technique is applied, the power consumed is decreased 76.3 mw/day and the battery life continues increasing to 19.91 days which is around x5 of the 40-nm device. Other than that, a Bluetooth and Wi-Fi are added to the UTBB with FBB, and it still

Table 2. Smart watch performance over transistors [17].

Smart watch	Power @ ISO Freq	Freq.@ ISO power	mW/Day (static + active)	Battery Life (Days)
40LP	1	1	334	4.65
28SLP	0.71	1.56	238.6	6.37
FINFET	0.39	2.8	131.2	11.58
FD-SOI	0.33	2.55	109.7	13.85
FD + FBB	0.23	2.97	76.3	19.91
FD + FBB + BLE	0.23	2.97	85.9	17.7
FD + FBB + BLE + WIFI	0.23	2.97	108.3	14

has lower power consumption (108.3 mw/day) than Tri-Gate FinFET and more battery life (14 days).

3.4. For Digital Blocks

In big digital blocks as CPUs and servers, increased power efficiency and decreasing the volume of the digital integrated circuits are the most important requirements. Increasing performance is done by reducing the power:

$$P = \alpha CFV_{dd}^2 + I_{leakage} V_{dd} . \quad (1)$$

where V_{DD} has more majority role, Intel 22-nm Tri-Gate FinFET transistor has 37% improved speed performance and 50% power reduction at 0.7 V over the 32-nm planar FinFET as mentioned before. On the other hand, the 28-nm UTBB FD-SOI transistor can achieve the same Tri-Gate FinFET performance at 200 mV_{lower} V_{DD} or (350 mV_{lower} V_{DD} with FBB = 1.5 V) [17]. The other comparison is that the Tri-Gate FinFET has the best digital scaling area over the UTBB and the Bulk CMOS, which gives priority for the Tri-Gate FinFET. The advantage of the leakage in UTBB transistor will not make a big difference in reducing the power because most of the transistors in CPUs and servers are working and not in standby. Therefore, if it's really a big digital chip with high density and without significant analog integration, where leakage is not a biggest concern and ultimate performance is more favorable, the Tri-Gate FinFET will be absolutely preferable.

3.5. For Embedded SRAM

Power efficiency and reductions in both static and dynamic power dissipation are needed to improve efficiency. Both transistors have high performance (if UTBB is with FBB). For SRAMs, the point of difference is that the biggest number of transistors can be in standby mode while some others are writing or reading, so lowering leakage can make a big improvement on the power consumption.

The UTBB with RBB (in N-MOS) is the best choice for lowering leakage. Other advantage of the UTBB is the lower gate capacitance which means that lower row of transistor can be used in addition to the better matching which leads to build smaller SRAMs. Also, the UTBB FD-SOI transistor has the best SER (soft error rate) because of the radiation hardness that is done by its isolation; the gain against the Alpha radiation with respect to bulk CMOS is x1000 for UTBB and x15 for Tri-Gate FinFET, while for Neutron radiation: x100 for UTBB and x10 for Tri-Gate FinFET [22]. Also, the radiation hardness gives a benefit for sensors and automotive applications. Those reasons make the UTBB preferable for embedded SRAMs circuits.

4. Conclusion

This paper, including Part I and Part II, provided a detailed comparison about bulk transistors and the better alternative technology that overcome the chal-

lenges faced by the conventional CMOS scaling. Alternative downscaled technology of fully depleted architecture, such as planar UTBB FD-SOI and Tri-Gate FinFET, is the key solution at 28-nm and beyond. Through the detailed comparison study of this paper, it turns out that the technology of 28-nm UTBBFD-SOI appears to be the most promising, reliable, and flexible for SoC applications.

5. Future Work

Currently, STMicroelectronics is working to produce 14-nm UTBB FDSOI transistor which boost 30% speed and 30% less power consumption [9]. Intel Tri-Gate FinFET, on the other hand, is in the process to produce 14nm transistors which decrease the parasitic capacitance and resistance; a challenge to enter the RF applications. Tri-Gate FinFET can be built on SOI substrate as IBM is doing, which has simpler manufacturing, better control over electrostatics in vertically aligned thin channel area [23] [24], higher on state drive performance [25], and back bias capability [26], but higher heat dissipation.

Transistor scaling is a continuous improvement for UTBB FD-SOI with a roadmap: from 28-nm, to 22-nm, to 14-nm, to 10-nm and below which will face physical limitation related to the electrons. Tri-Gate FinFET is more momentum [27]; it is a 3D structure which starts a new generation of transistors, it has a big chance to grow, and it has more performance per unit volume.

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