

# Mg Tilted-Angle Ion Implantation for Threshold Voltage Control and Suppression of the Short Channel Effect in GaN MISFETs

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## Abstract

This paper demonstrates that threshold voltages of GaN MISFET are controllable by varying the Mg ion doses for Mg ion implantation. Furthermore, it demonstrates for the first time that the short channel effect can be suppressed using a halo structure that has a p-layer in channel regions adjacent to source/drain regions using tilt ion implantation. A device with a Mg dose of  $8 \times 10^{13}/\text{cm}^2$  achieved maximum drain current of 240 mA/mm and a transconductance of 40 mS/mm. These results indicate a definite potential for the use of our new process in GaN MISFETs for applications in power switching devices.

## Keywords

GaN, MISFET, Mg Ion Implantation, Threshold Voltage

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## 1. Introduction

Gallium nitride (GaN) is an ideal material for high power, high frequency, and high temperature devices due to its remarkable properties such as a wide band-gap, a high breakdown electric field, and a high saturation velocity [1]. One of the applications of GaN is in a high electron mobility transistor (HEMT) with the structure of AlGaIn/GaN, which has been the focus of many researchers as it can be successfully used in high speed, high power devices [2] [3]. Threshold voltage control in HEMTs is well known to be very difficult, as complicated processes such as recessed gate etching are needed [4]. Recessed gate HEMTs have high performance ( $g_m \approx 150$  mS/mm) and normally-off operation, but still have a problem of threshold voltage fluctuation due to recessed gate structure and the short channel effect. Therefore, a MISFET (non-HEMT) is required to overcome this problem. To fabricate a MISFET, it is necessary to form p-type

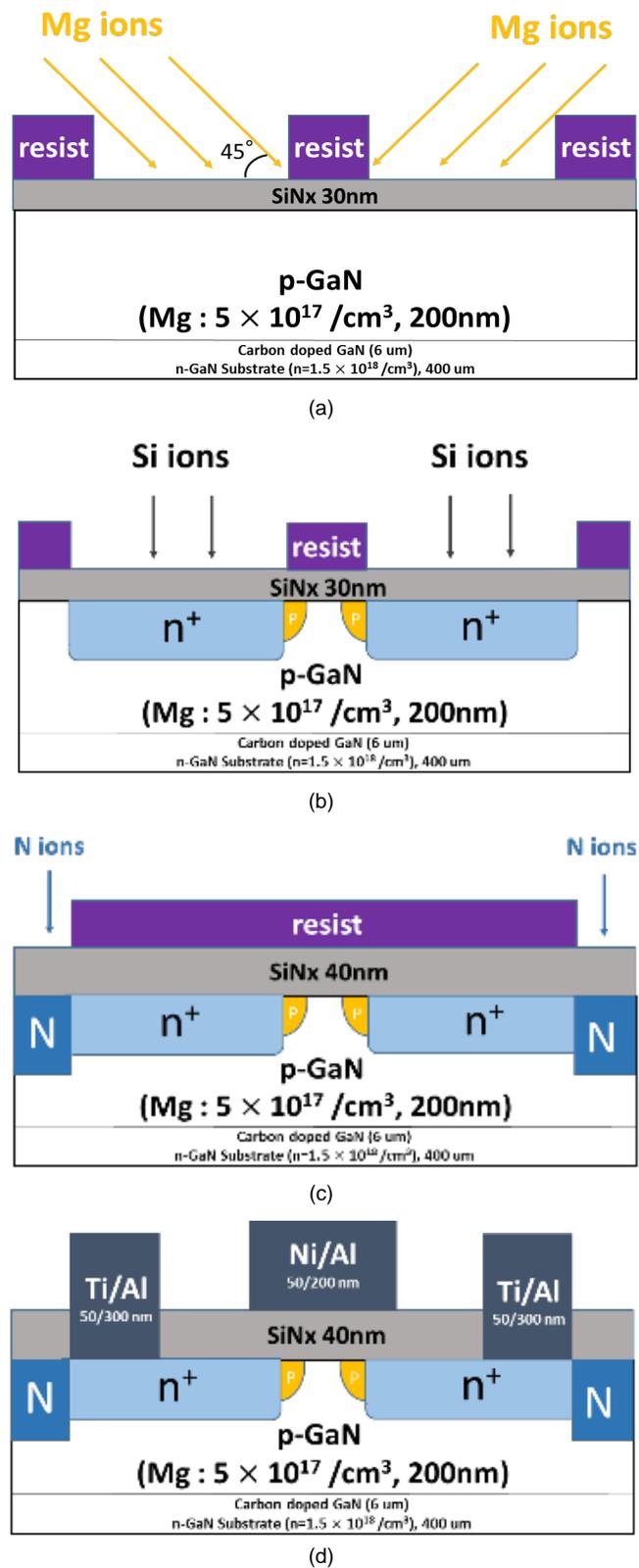
regions by ion implantation. However, this process has been challenging. One recent study reported the formation of a p-type conductive layer by Mg ion implantation. Also, there are some reports of forming the p-type layer evaluated by Hall measurements [5] [6]. However, Mg ion implantation hasn't been applied to GaN device fabrication in the past. This paper demonstrates that the threshold voltage of a GaN MISFET can be controlled using Mg ion implantation and that the short channel effect is suppressed with a halo structure that has a p-layer in channel regions adjacent to source/drain regions using tilt ion implantation [7].

## 2. Device Fabrication

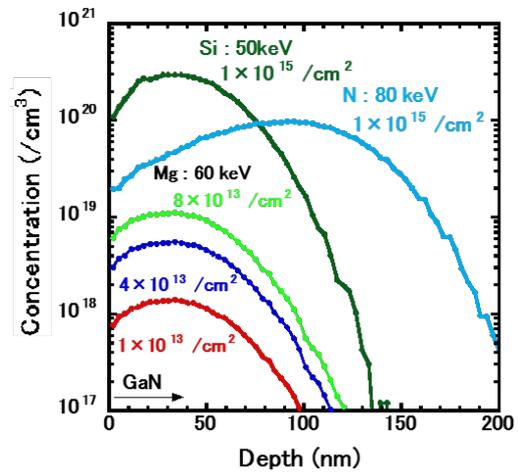
Epitaxial layer structures were grown by metal-organic vapor phase epitaxy (MOVPE) on free-standing GaN substrates, which reduce threading dislocation densities of epitaxial layers on GaN to approximately  $10^6/\text{cm}^2$ . The crystallinity of the epitaxial layers is important because there is a report that the p-type layer grown by ion implantation depends on the dislocation densities of the epitaxial layers [8]. The epitaxial layers consist of Mg-doped-GaN (Mg:  $5 \times 10^{17}/\text{cm}^3$ , 200 nm)/carbon-doped-GaN (C:  $1.1 \times 10^{19}/\text{cm}^3$ , 6  $\mu\text{m}$ ) layer on a GaN substrate ( $n = 1.5 \times 10^{18}/\text{cm}^3$ , 400  $\mu\text{m}$ ). A 30 nm-thick SiNx film was deposited on the layers. Mg ions were implanted to the SiNx film surface with a tilted angle of 45 degrees at doses of  $1 \times 10^{13}/\text{cm}^2$ ,  $4 \times 10^{13}/\text{cm}^2$  and  $8 \times 10^{13}/\text{cm}^2$  at an energy of 60 keV as shown in **Figure 1(a)**. After the lithography process to form  $n^+$  regions (source/drain), Si ions were implanted on sample surfaces at a dose of  $1 \times 10^{15}/\text{cm}^2$  at an energy of 50 keV as shown in **Figure 1(b)**. The SiNx films were then removed and 40 nm thick SiNx films were deposited again, followed by activation annealing at 1230°C for 1 min in ambient  $\text{N}_2$ . N ions were implanted into field regions at a dose of  $1 \times 10^{15}/\text{cm}^2$  at an energy of 80 keV to perform device isolation of GaN MISFETs as shown in **Figure 1(c)** [9]. The simulated impurity profiles of Mg, Si, and N ions are shown in **Figure 2**. Source/drain electrodes were formed by depositing Ti/Al (50/300 nm) layers, followed by metallization annealing at 550°C for 1 min. Finally, gate electrodes were formed by depositing Ni/Al (50/200 nm) layers as shown in **Figure 1(d)**.

## 3. Device Performance

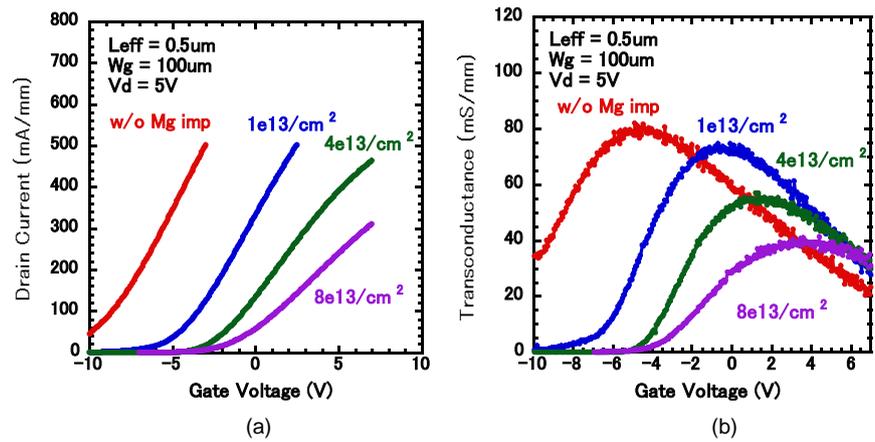
**Figure 3** shows  $I_d - V_g$  (a) and  $g_m - V_g$  (b) characteristics of the GaN MISFETs. The threshold voltage of the MISFETs increases with increasing the dose of Mg ions, which means that the threshold voltage of GaN MISFETs is controllable. **Figure 4** shows  $I_d - V_d$  characteristics of the fabricated GaN MISFETs with the Mg ion dose of  $8 \times 10^{13}/\text{cm}^2$ . Maximum drain current of 240 mA/mm at  $V_g = 5\text{V}$  and maximum transconductance of 40 mS/mm were obtained for 0.5  $\mu\text{m}$  gate length. The MISFETs indicate normally-on characteristics despite using a p-type epitaxial layer and Mg ion implantation. This might be caused by high temperature annealing that activated Si and Mg impurities because high temperature annealing introduces N vacancies that act as donors in GaN [10].



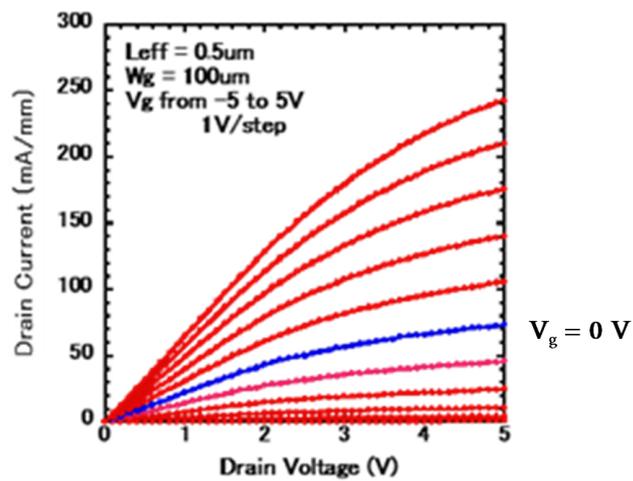
**Figure 1.** Fabrication processes of GaN MISFETs. Tilted Mg ion implantation for controlling threshold voltage (a), vertical Si ion implantation for forming source/drain regions (b), N ion implantation for forming isolation regions in SiNx film (c) and the fabricated GaN MISFETs (d).



**Figure 2.** Simulated implanted impurity depth profiles of Si ions for the formation of source/drain regions, Mg ions adjacent to the source/drain regions, and N ions for field isolation regions.



**Figure 3.**  $I_d - V_g$  (a) and  $g_m - V_g$  (b) characteristics of the fabricated GaN MISFETs. The threshold voltage increases with increasing the dose of implanted Mg ions.



**Figure 4.**  $I_d - V_d$  characteristics of the fabricated GaN MISFETs with tilted Mg ion implantation (dose:  $8 \times 10^{13}/\text{cm}^2$ ).

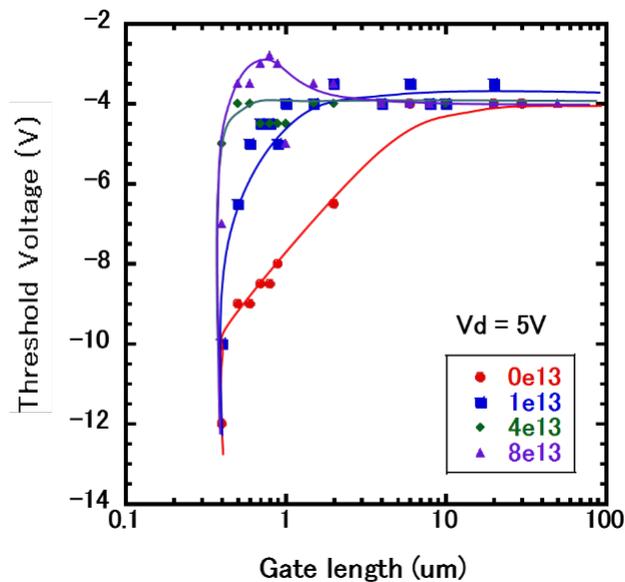
**Table 1** compares the characteristics of fabricated GaN MISFETs with various Mg doses. As the Mg dose increases, the threshold voltage increases, the maximum transconductance decreases, and the drain current ( $V_g - V_{th} = 5\text{ V}$ ,  $V_d = 5\text{ V}$ ) decreases. **Figure 5** shows the relationship between the threshold voltage and the gate length of the devices. The threshold voltage of MISFET without Mg implantation decreases with decreasing the gate length. This is caused by short channel effects. However, the threshold voltage of MISFET with Mg implantation does not decrease with decreasing the gate length because the short channel effects are suppressed depending upon the dose of Mg ions. In other words, Mg ion implantation suppresses the short channel effect. The threshold voltage of the MISFET with the Mg dose of  $8 \times 10^{13}/\text{cm}^2$  is increased at the gate length around  $0.7\ \mu\text{m}$ . This might be caused by the reverse short channel effect (RSCE) and the higher implant dose shows a larger RSCE [11].

#### 4. Summary

This paper demonstrated that threshold voltage of GaN MISFET is increased by increasing the ion doses of Mg ion implantation, which means that the threshold voltage of GaN MISFETs is controllable. In addition, it demonstrated for the

**Table 1.** Comparison of characteristics of GaN MISFETs.

Tilt angle Mg implanted GaN MISFET	Threshold Voltage $V_{th}$ (V)	Maximum Transconductance $g_{mmax}$ (mS/mm)	Drain Current $I_d$ (mA/mm) ( $V_g - V_{th} = 5\text{ V}$ , $V_d = 5\text{ V}$ )
Mg dose: $1 \times 10^{13}/\text{cm}^2$	-6.5	73	225
Mg dose: $4 \times 10^{13}/\text{cm}^2$	-4	55	188
Mg dose: $8 \times 10^{13}/\text{cm}^2$	-3.5	40	106



**Figure 5.** Relationship between the threshold voltage and gate length for the devices.

first time that Mg implantation suppresses the short channel effect. The fabricated GaN MISFET (dose:  $8 \times 10^{13}/\text{cm}^2$ ) achieved the maximum drain current of 240 mA/mm and transconductance of 40 mS/mm. These results indicate a definite potential for the use of this new process in GaN MISFETs applications of power switching devices.

## References

- [1] Wakejima, A., Nakayama, T., Ota, K., Okamoto, Y., Ando, Y., Kuroda, N., Tanomura, M., Matsunaga, K. and Miyamoto, H. (2006) Pulsed 0.75kW Output Single-Ended GaN-FET Amplifier for L/S Band Applications. *Electron. Lett.*, **42**, 1349-1350. <https://doi.org/10.1049/el:20062950>
- [2] Nomoto, K., Tajima, T., Mishima, T., Satoh, M. and Nakamura, T. (2007) Remarkable Reduction of On-Resistance by Ion Implantation in GaN/AlGaIn/GaN HEMTs with Low Gate Leakage Current. *IEEE Electron Device Lett.*, **28**, 939-941. <https://doi.org/10.1109/LED.2007.906930>
- [3] Katayose, H., Ohta, M., Nomoto, K., Onojima, N. and Nakamura, T. (2011) 55 nm Gate Ion-Implanted GaN-HEMTs on Sapphire and Si Substrates. *Phys. Status Solidi C*, **8**, 2410-2412. <https://doi.org/10.1002/pssc.201001017>
- [4] Kanamura, M., Ohki, T., Kikkawa, T., Imanishi, K., Imada, T., Yamada, A. and Hara, N. (2010) Enhancement-Mode GaN MIS-HEMTs with n-GaN/i-AlN/n-GaN Triple Cap Layer and High-k Gate Dielectrics. *IEEE Electron Lett*, **31**, 189-191. <https://doi.org/10.1109/LED.2009.2039026>
- [5] Feigelson, B.N., Anderson, T.J., Abraham, M., Freitas, J.A., Hite, J.K., Eddy, C.R. and Kub, F.J. (2012) Multicycle Rapid Thermal Annealing Technique and Its Application for the Electrical Activation of Mg Implanted in GaN. *Journal of Crystal Growth*, **350**, 21-26. <https://doi.org/10.1016/j.jcrysgro.2011.12.016>
- [6] Anderson, T.J., Feigelson, B.N., Kub, F.J., Tadjer, M.J., Hobart, K.D., Mastro, M.A., Hite, J.K. and Eddy, C.R. (2014) Activation of Mg Implanted in GaN by Multicycle Rapid Thermal Annealing. *Electronics. Lett.*, **50**, 197-198. <https://doi.org/10.1049/el.2013.3214>
- [7] Chatterjee, A., Vasanth, K., Grider, D.T., Nandakumar, M., Pollack, G., Aggarwal, R., Rodder, M. and Shichijo, H. (1999) Transistor Design Issues in Integrating Analog Functions with High Performance Digital CMOS. *Sympo. VLSI*, 147-148,.
- [8] Oikawa, T., Saijo, Y., Kato, S., Mishima, T. and Nakamura, T. (2015) Formation of Definite GaN p-n Junction by Mg-Ion Implantation to n-GaN Epitaxial Layers Grown on a High-Quality Free-Standing GaN Substrate. *Nuclear Instruments and Methods in Physics Research B*, **365**, 168-170. <https://doi.org/10.1016/j.nimb.2015.07.095>
- [9] Kasai, H., Ogawa, H., Nishimura, T., Nakamura, T. (2014) Nitrogen Ion Implantation Isolation Technology for Normally-Off GaN MISFETs on p-GaN Substrate. *Phys. Status Solidi C*, **11**, 914-917. <https://doi.org/10.1002/pssc.201300436>
- [10] Lin, Y.-J., Chen, Y.-M., Cheng, T.-J. and Ker, Q. (2004) Schottky Barrier Height and Nitrogen-Vacancy-Related Defects in Ti Alloyed Ohmic Contacts to n-GaN. *J. Appl. Phys.*, **95**, 571-575. <https://doi.org/10.1063/1.1633658>
- [11] Wu, J.-W., Cheng, C.-C., Chiu, K.-L., Guo, J.-C., Lien, W.-Y., Chang, C.-S., Huang, G.-W. and Wang, T. (2004) Pocket Implantation Effect on Drain Current Flicker Noise in Analog nMOSFET Devices. *IEEE Transactions Electron Devices*, **51**, 1262-1266. <https://doi.org/10.1109/TED.2004.831369>



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