

Design of 2-to-4 All-Optical Decoder with the Help of Terahertz Optical Asymmetric Demultiplexer

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Abstract

An all-optical 2-to-4 decoder unit with the assist of terahertz optical asymmetric demultiplexer (TOAD) is presented. The all-optical 2-to-4 decoder with a set of all-optical switches is designed which can be used to achieve a high-speed central processor unit using optical hardware. The unique output lines can be used for all-optical header processing. We attempt to develop an integrated all-optical circuit which can perform decoding of signal. This scheme is very simple and flexible for performing different logic operation and to design advanced complex logic. Simulated results are confirming the described methods.

Keywords

Terahertz Optical Asymmetric Demultiplexer, Semiconductor Optical Amplifier, All-Optical Decoder

1. Introduction

By the advent of optical networks and optical communication systems need for all-optical circuits and devices has been started. Currently communication networks aim to reach very bit rates and ultrafast data transfer rates with terabit per second bit rates. In order to achieve such a high bit rate, we should have a complete optical network without any electronics to optical conversion. In such a network, all communication steps such as sending, receiving and data processing should be performed totally in optical domain. A decoder is important for header processing in typical core router/demultiplexer for addressing output port. There are many research areas which

have been proposed using various all-optical switching and all-optical logic operation, such as all-optical packet-switching [1], all-optical demultiplexing [2] semiconductor optical amplifier (SOA) [3]-[5], TOAD based interferometer device [6]-[9], cascaded microring resonators [10], and all-optical code conversion [11]-[13]. Among the different proposed schemes, the terahertz optical asymmetric demultiplexer (TOAD)/semiconductor optical amplifier (SOA)-assisted Sagnac gate effectively combines fast switching time and a reasonable noise figure, with the ease of integration and overall practicality that enables it to compete favorably with other similar optical time division multiplexing devices. TOAD is characterized by the attractive features of low power consumption, fast switching time, low latency, high repetition rate, jitter tolerance, noise and thermal stability, compactness and high nonlinear properties, which allow their competent utilization in a real ultra-high speed optical communications environment. TOAD has the potential of being integrated, which can be frequently and consistently manufactured and massively produced so that they can be of viable value.

In this paper we propose and describe the TOAD based switch to design 2-to-4 line decoder in all-optical domain. It can convert binary information from n input line to a maximum of 2^n unique output line.

2. Operation of TOAD Based Switch

The basic design of TOAD based switch is shown in **Figure 1** [6]. Here a semiconductor optical amplifier (SOA) is placed asymmetrically in a loop. The output power at upper and lower can be expressed as [7]-[9] [11]-[13]

$$P_{\text{Upper}}(t) = \frac{P_{\text{IS}}(t)}{4} \times \left\{ G_{\text{CW}}(t) + G_{\text{CCW}}(t) - 2\sqrt{G_{\text{CW}}(t) \times G_{\text{CCW}}(t)} \times \cos(\Delta j) \right\} \quad (1)$$

$$P_{\text{Lower}}(t) = \frac{P_{\text{IS}}(t)}{4} \times \left\{ G_{\text{CW}}(t) + G_{\text{CCW}}(t) + 2\sqrt{G_{\text{CW}}(t) \times G_{\text{CCW}}(t)} \times \cos(\Delta j) \right\} \quad (2)$$

where, $G_{\text{CW}}(t), G_{\text{CCW}}(t)$ is the power gain.

The time-dependent phase difference between clockwise (CW) and counter clockwise (CCW) pulses [7]-[9] is

$$\Delta\phi = -\frac{\alpha}{2} \ln \left[\frac{G_{\text{CW}}(t)}{G_{\text{CCW}}(t)} \right] \quad (3)$$

with α being the line-width enhancement factor. In the absence of a control signal, data signal (incoming signal) enters the fiber loop, pass through the SOA at different times as they counter-propagate around the loop and experience the same unsaturated small amplifier gain G_{ss} and recombine at the input coupler *i.e.* $G_{\text{CCW}} \approx G_{\text{CW}}$. Then, $\Delta\phi \approx 0$ and expression for $P_{\text{up}} \approx 0$ and $P_{\text{LOW}}(t) = P_{\text{IS}}(t) \cdot G_{\text{ss}}$. It shows that data is reflected back toward the source. When a control pulse is injected into the loop (CP = on), it saturates the SOA at time t_s and changes its index of refraction. The gain of the SOA decreases rapidly as [11]-[13]:

$$G(t) = \frac{1}{1 - \left(1 - \frac{1}{G_{\text{ss}}}\right) \exp\left(-\frac{E_{\text{cp}}(t)}{E_{\text{sat}}}\right)} \quad (4)$$

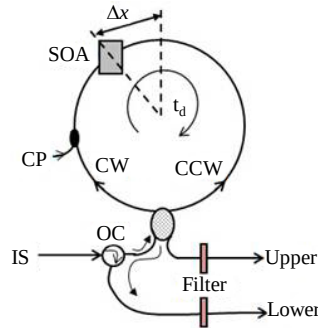


Figure 1. A TOAD based optical switch with single control pulse (CP), where SOA: semiconductor optical amplifier, CW: clockwise pulse, CCW: counterclockwise pulse, t_d : pulse round trip time, Δx : asymmetric distance, IS: incoming signal and OC: optical circulator.

Therefore when they recombine at the input coupler, then $\Delta\varphi \approx -\pi$ (obtained from Equations (3) and (4)) and the data will exit from the upper port *i.e.* $P_{UP}(t) \neq 0$ and $P_{LOW}(t) \approx 0$, the corresponding values can be obtained from the equations (1) and (2), respectively. The energy of the control pulse is ten times greater than that of the incoming pulse. A filter may be used at the output of TOAD based switch to reject the control and pass the incoming pulse. The schematic diagram of TOAD based switch is shown in [Figure 2](#).

A decoder is a combinational circuit which changes binary information from n inputs to maximum of 2^n unique outputs. The only inputs in decoders are the control bits. In digital electronics, a decoder can capture the shape of a many inputs and outputs logic circuit that converts coded inputs into its coded outputs, where the input and output codes are different e.g. n to 2^n . A 2-to-4 decoder operates according to the truth [Table 1](#) with enable input (EI). This EI is used for activate (EI = 1) or deactivate (EI = 0) the decoder. Decoding is essential in applications such as memory address, decoding data, multiplexing and 7 segment displays. A block diagram of 2-to-4 decoder (2 input lines and 4 output lines) with enable input (EI) is shown in [Figure 3](#).

To implement the optical 2-to-4 decoder, we use TOAD-based optical switches, namely s_1 to s_4 as shown in **Figure 3**. Parallel binary numbers are used as inputs to a decoder and that are used to sense the presence of particular binary information at the input. The output specifies absence or presence of particular number at the decoder input. Here upper and lower ports of T_1 are fed to T_3 and T_4 as incoming signal and both output ports of T_2 are considered as control signals of T_3 and T_4 respectively. In a TOAD based switch the incoming signal is of wavelength λ_2 and the control pulse signal is of wavelength λ_1 , where $\lambda_1 \neq \lambda_2$. So, when a light of wavelength λ_2 from an output port of one TOAD based switch is connected as a control signal to another TOAD based switch, then the wavelength λ_2 is required to be converted to wavelength λ_1 for the second switch. This is done

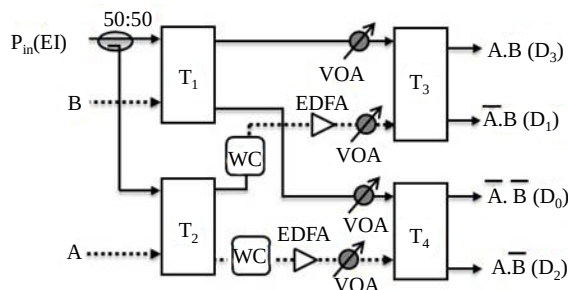
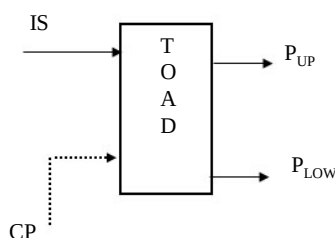


Figure 3. A block diagram of all-optical decoder, where $P_{in}(EI)$: Incoming light signal (enable input), A and B: input data signals, T_1 - T_4 : TOAD based switches, 50:50: 3 dB coupler, WC: wavelength converter, VOA: variable optical attenuator, EDFA: Er^{+3} doped fiber amplifier. Solid line indicates optical data signal of wavelength λ_2 and dotted line indicates control signal path of wavelength λ_1 .

with the help of a wavelength converter (WC). Its size is few micrometers and power consumption is also negligible. Then the optical power is amplified by Er^{+3} doped fiber amplifier (EDFA) with its gain G_{EDFA} . Power of the wavelength converted amplified signal can be adjusted by variable optical attenuator (VOA) before fed it to the TOAD as control signal. All the output ports of TOADs T_3 and T_4 are utilized to verify the [Table 1](#).

In this circuit, we can remove the extra enable input which is required for activate and deactivate the decoder circuit. Here the incoming single P_{in} itself uses as an enable input. When P_{in} is 0 *i.e.*, the incoming signal is absence for the switches T_1 and T_2 and no outputs receive any light as filter block the control signal if any. So when P_{in} is 1 *i.e.*, the incoming signal is present for the switches T_1 and T_2 hence the circuit becomes active and depending on the values of input A and B , the desired output will be obtained at the any of the output terminal of D_0 , D_1 , D_2 and D_3 . The logic level “0” and “1” are indicated as “Absence” and “Presence” of light signals respectively. There are 4 different input combinations for implementing double input binary logic, depending on the state of input variables (A and B) when incoming signal is present.

4. Simulated Results

Numerical simulation has been done to confirm the operation of this proposed circuit. The parameters used in this simulation are as follows: saturation energy of the SOA (E_{sat}) = 1000 fJ, gain recovery time of the SOA (τ_e) = 50 ps, unsaturated amplifier gain of the SOA (G_{ss}) = 30 dB, eccentricity of the loop (T_{asym}) = 15 ps, FWHM of the control pulse (σ) = 3.6 ps, control pulse energy (E_{cp}) = 100 fJ, bit period (T_c) = 50 ps, and a line-width enhancement factor (α) = 6. The simulated input and output waveforms are given in [Figure 4](#).

Table 1. Truth table of decoder with enable input.

Enable input	Inputs		Outputs			
EI	A	B	D_0	D_1	D_2	D_3
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

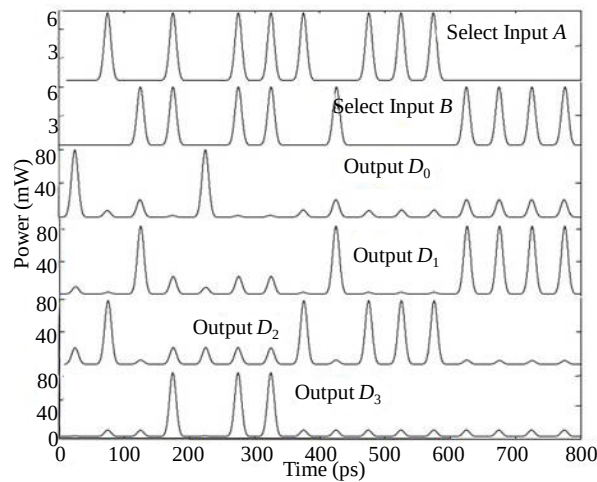


Figure 4. A Simulated input and output waveforms, where power (mW) is along the y-axis whereas time is along the x-axis in ps.

In order to assess the performance of the circuit at 20 Gbit/s, we define the contrast ratio (CR) as

$$CR(\text{dB}) = 10 \log \left(\frac{P_{\text{mean}}^1}{P_{\text{mean}}^0} \right) \quad (5)$$

where P_{mean}^1 and P_{mean}^0 is the mean of the peak power of the 1-states and 0-states, respectively. For high performance, it must be as high as possible so that largest fraction of the incoming data signal exits at the target output of the circuit. The operation of the circuit depends on the proper SOA gain saturation and in particular its recovery, it is evident that the carrier lifetime, control pulse energy and input pulse width are important performance parameter. For this reason, the effect on the CR with different control pulse energy and gain recovery time is depicted in **Figure 5**. The common characteristic of all curves in **Figure 5** is that CR increases with increasing control pulse energy and gain recovery time up to a certain value (~ 100 fJ and ~ 100 ps) after which CR is decreased. This can be explained physically by considering the SOA dynamic gain response. The saturation energy decreases with decrease of gain recovery time for constant saturation power.

This in turn means that less energy is required in order to saturate the SOA and obtain a large change in the amplification of the counter-propagating pulses. The value of ~ 100 fJ for control pulse energy, ~ 100 ps for gain recovery time and pulse width ~ 12 ps is applied for getting the contrast ratio greater than 9 dB. The lower control pulse energy and small-signal gain values are insufficient for full switching. This occurs because the created phase difference is much less than the required value π , which reduces the contrast ratio. The eye-diagram is the superposition of the outputs for the repetition period of the inputs, i.e., inputs varies from $0 \rightarrow 0$, $0 \rightarrow 1$, $1 \rightarrow 1$, $1 \rightarrow 0$, and so on [14]. **Figure 6** is called a *pseudo-eye-diagram* [14]. The relative eye opening (O) is defined as $O = (P_{\text{min}}^1 - P_{\text{max}}^0) / P_{\text{min}}^1$, P_{min}^1 and P_{max}^0 are the minimum and maximum powers at 1-state and 0-state, respectively, which can be calculated from **Figure 6**. An eye-diagram with large eyes indicates a clear transmission with a low bit error rate. Here, we get PED (O) = 82.36%, which indicates an excellent response of the circuit to the incoming data at its output terminals.

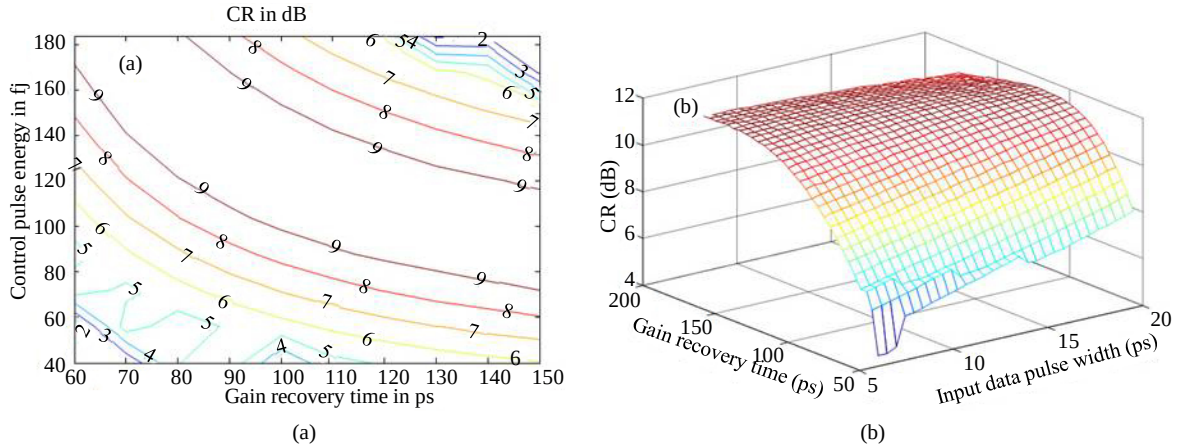


Figure 5. Variation of CR with (a) control pulse energy and gain recovery time and (b) gain recovery time and pulse width at the outputs.

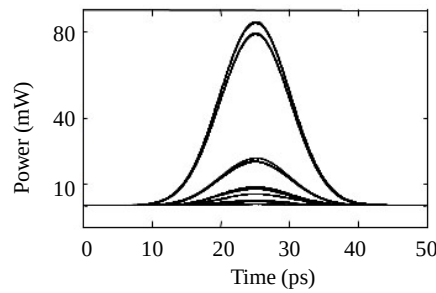


Figure 6. Simulated output waveforms with pseudo-eye-diagram (PED).

5. Conclusion

All-optical decoder is expected to be helpful in optical system nodes because of smartness and flexibility. In this paper, we have proposed and theoretically demonstrated the operations of decoder. By conducting numerical simulation, we have specified the requirements for the input pulse width, gain recovery time and control pulse energy so that the performance metrics of contrast ratio and relative opening of the eye diagram are satisfactory. This model may be expanded for studying more compound all-optical decoder.

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