

Novel Adder Circuits Based on Quantum-Dot Cellular Automata (QCA)

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Abstract

Quantum-dot cellular automaton (QCA) is a novel nanotechnology that provides a very different computation platform than traditional CMOS, in which polarization of electrons indicates the digital information. This paper demonstrates designing combinational circuits based on quantum-dot cellular automata (QCA) nanotechnology, which offers a way to implement logic and all interconnections with only one homogeneous layer of cells. In this paper, the authors have proposed a novel design of XOR gate. This model proves designing capabilities of combinational circuits that are compatible with QCA gates within nano-scale. Novel adder circuits such as half adders, full adders, which avoid the fore, mentioned noise paths, crossovers by careful clocking organization, have been proposed. Experiment results show that the performance of proposed designs is more efficient than conventional designs. The modular layouts are verified with the freely available QCADesigner tool.

Keywords

Quantum Dot Cellular Automata (QCA), XOR Gate, Half Adder, Full Adder, Nanotechnology, QCADesigner

1. Introduction

Quantum-dot cellular automaton (QCA) is a new nanotechnology that can help us to achieve low power consumption, high device density, and high clock frequency. Since QCA, size is smaller than CMOS it can, even be implemented in molecular or atomic size. Further, in CMOS, by decreasing the transistor sizes, some problems such as power consumption cannot be ignored. A number of research efforts have been focused on new devices

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that might replace CMOS technology [1]. Utilizing the QCA technology [2] for implementing logic circuits is one of the approaches which, in addition to decreasing the size of logic circuits and increasing the clock frequency and reduces the power consumption of these circuits. The emerging technologies pertaining to circuit design lay great emphasis on small size, high device density, and low power dissipation to achieve objective of portability of systems [3]. Quantum-dot Cellular Automata (QCA) [4] [5], promises aforementioned features.

The implementation of circuits using QCA is based on coulombic interactions. QCA circuits can be used to implement combinational circuits by arranging cells with proper clock delays. So far, several studies have been reported about QCA full adder [6]-[12]. Initial adder designs were constructed with five majority gates (a fundamental QCA logic gate) and three inverters [11]. Tougaw and Lent proposed the first design for a QCA 1-bit full adder by connecting “n”, such 1-bit QCA full adders, a carry look ahead (CLA) adder can be obtained, since the carry is generated before the sum in the QCA adder [13]. A new bitserial QCA adder has also been proposed [14], which uses carry feedback and only requires three majority gates and two inverters. However, this bit-serial approach requires a complicated clocking scheme and feedback control. In this paper, we propose an efficient XOR gate with proper clock delay organizations which has been presented. The present design consists of less area to conventional designs [15].

2. Quantum-Dot Cellular Automata (QCA)

The fundamental unit of QCA device is QCA cell. A QCA cell, created with four quantum Dots positioned at the vertices of a square [16] [17], coupled by tunneling barriers has been in **Figure 1(a)**. These quantum dots are sites in which electrons are able to tunnel between them but cannot leave the cell. The electrons will tend to occupy diagonally opposite sites into the quantum dots due to electrostatic force of interaction.

Quantum dots are small semi-conductor or metal islands with a diameter that is small enough to make their charging energy greater than k_bT (where k_b is Boltzmann’s constant and T is the operating temperature).

Two mobile electrons are loaded in the cell, which can move to different quantum dots in the QCA cell by means of electron tunneling. The lines connecting the quantum dots in **Figure 1(b)** can represent tunneling paths. The electrons in the cell, placed adjacent to each other will interact; as a result, the polarization of one cell will be directly affected by the polarization of its neighboring cells.

If the barriers between cells are sufficiently high, the electrons will be well localized in individual dots. The Coulomb repulsion between the electrons will tend to make them occupy antipodal sites in the square as shown in **Figure 1(b)**. For an isolated cell there are two energetically equivalent arrangements of the extra electrons which we denote as a cell polarization $P = +1$ and $P = -1$. The term “cell polarization” refers only to this arrangement of charge and does not imply a dipole moment for the cell. The cell polarization is used to encode binary information, thus, $P = +1$ represents a binary 1 and $P = -1$ represents a binary 0. The two polarization states of the cell will not be energetically equivalent if other cells are nearby. Consider two cells close to one another as shown in the inset of **Figure 1(c)**. It illustrates the case when cell 2 has a polarization of $P = +1$ state, the ground-state configuration of cell 1 follows the same polarization. Similarly if cell 2 is in the $P = -1$ state, the ground state of cell 1 will match it. This shows the nonlinear response of the cell–cell interaction, which plays the role of voltage gain in conventional devices.

In QCA implementations, the power consumption of QCA circuits is mainly affected by clock signals. Therefore, in practice using a proper clock, the power consumption will be very less but still it is data dependent. In order to remove the data dependency of power traces, Bennett clocking scheme can be used for different inputs [18]. By using Bennett clocking, the power dependence of QCA circuits on the inputs can be effectively removed making it impossible to perform power analysis attack [19].

2.1. QCA Logic Circuits

Some basic elements for QCA logic implementation are wire, inverter, and majority voter [20] shown in **Figure 2(a)**, **Figure 2(b)** & **Figure 2(c)**. The QCA wire is formed by an array of QCA cells shown in **Figure 2(b)**, which provides a medium for data propagation based on Coulomb interactions. The simplest inverter is built by placing QCA cells in a diagonal structure shown in **Figure 2(c)**. The polarization of the output QCA cell “out” or “output” is the opposite of the polarization of input QCA cell “in” or “input”. Here the MV, is equivalent to a logic function $F(A, B, C) = AB + AC + BC$ and can be implemented by five QCA cells arranged in a cross. Cells

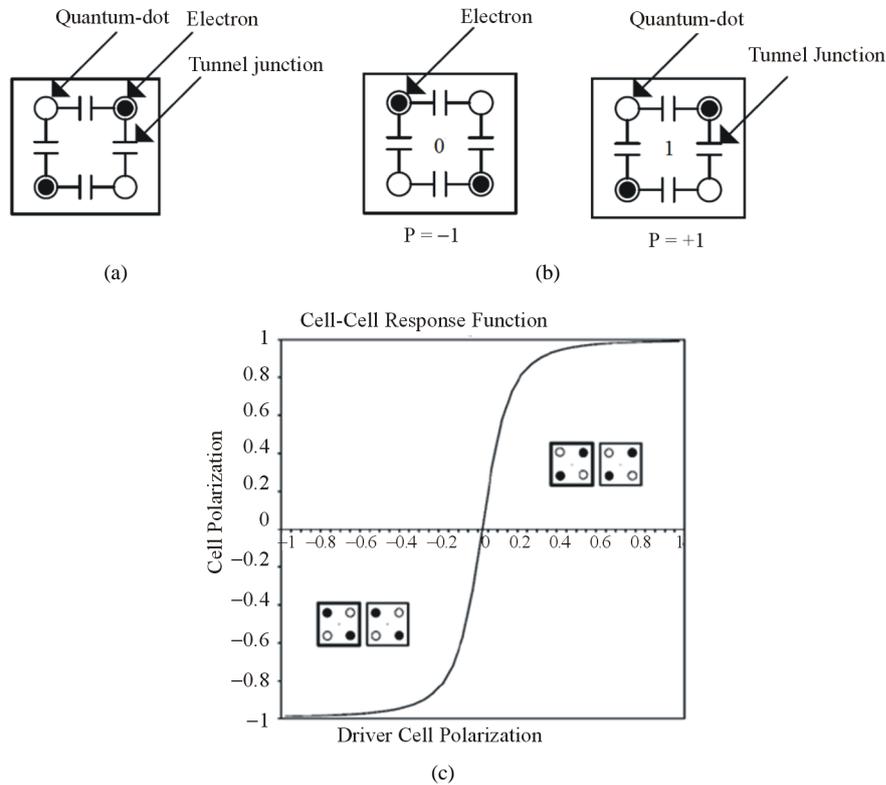


Figure 1. (a) Basic QCA cell; (b) Basic four-dot QCA cell showing the possible ground-state polarizations; (c) Non-linear interaction between QCA cells.

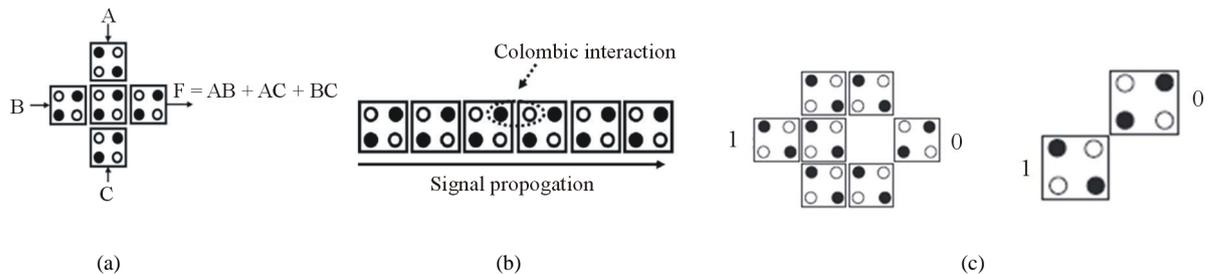


Figure 2. Basic QCA logic devices: (a) Majority vote; (b) Wire; (c) Inverter.

A, B, and C are input cells, and cell D is the output cell that is polarized according to the polarization of majority of the input cells. Logical AND and OR functions can be implemented from majority vote by presetting one input to binary values 0 and 1, respectively.

2.2. QCA Clock

A QCA cell has four clock zones and each clock zone has four phases; Switch, Hold, Release and Relax [21]. **Figure 3(a)** shows its operation process. During the switch phase, QCA cells begin to become unpolarized and their inter-dot potential barriers are low. The barriers are then raised during this phase and the QCA cells become polarized according to the state of their driver (*i.e.* their input cell). It is in this clock phase that the actual computation (or switching) occurs. By the end of this clock phase, barriers are high enough to suppress any electron tunneling and cell states are fixed. During the hold phase, barriers are held high so the outputs of the sub array can be used as inputs to the next stage. In the release phase, barriers are lowered and cells are allowed to relax to an unpolarized state. Finally, during the fourth clock phase, the relax phase, cell barriers remain lowered and cells remain in an unpolarized state [20]-[22]. In the mean time, the large-scale QCA circuit is parti-

tioned into four clock zones; **Figure 3(b)** shows each clock zone signal and demonstrates pipeline mechanism. All cells in a certain zone are controlled by the same QCA clock signal. Cells in each zone perform a specific calculation; the state of a zone is then fixed so that it can serve as input signal to the next zone. This results into information transfers in a pipelined fashion.

3. QCA Implementations

In addition to basic logic gates, exclusive-OR (XOR) and exclusive-NOR (XNOR) gates are also used in the design of digital circuits. These have special functions and applications. These gates are particularly useful in arithmetic operations as well as code generators. XOR and XNOR gates are usually found as 2-input gates. No multiple-input XOR/XNOR gates are available since they are complex to fabricate with hardware. Different authors have proposed QCA XOR gates for conventional layout [23]-[25]. The design has complexity of cells and coplanar crossovers or multiple layers to implement. The area of these conventional designs is large. The performance of various QCA layouts XOR gates has been shown in [26].

3.1. Proposed XOR Gate

It is possible to implement all combinational and sequential logic functions by properly arranging cells so that the polarization of one cell sets the polarization of a nearby cell [27]. According to previous studies, several logic gates and computing devices [28] are implemented with QCA. We propose an efficient XOR gates with less crossovers, area $0.03 \mu\text{m}^2$, of 30 cells and 0.5 clock delays as shown in **Figure 4(a)** compared to previous designs [26]. The simulation results of proposed XOR gate is shown in **Figure 4(b)**.

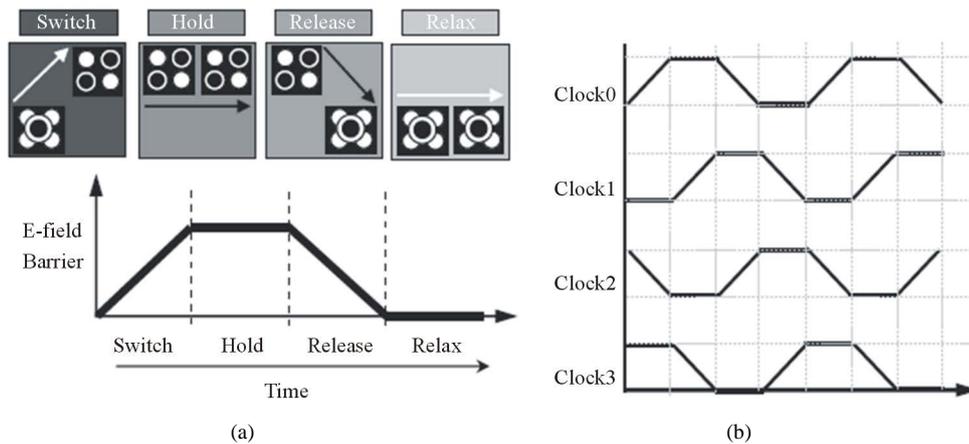


Figure 3. (a) Four phases of QCA clock; (b) Clock zones signal.

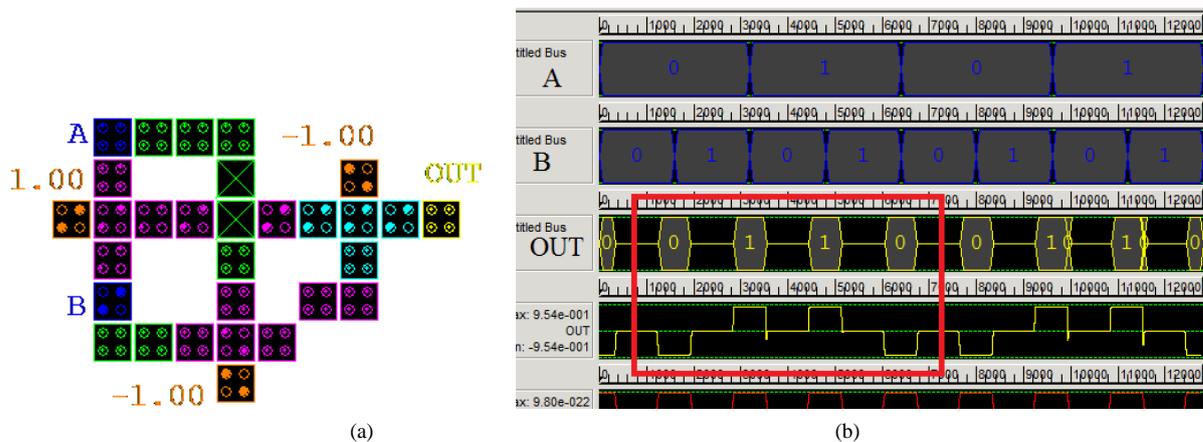


Figure 4. (a) QCA layout of XOR gate; (b) Simulation results.

3.2. Proposed QCA Layout of Half Adders

Digital computers perform various arithmetic operations. The most basic operation is the addition. The addition operation is achieved by majority logic that can reduce the overall number of gates required to create the adder circuits. Researchers have proposed the QCA implementation of half adder [29]. The design needs either coplanar crossovers or multiple layers to implement. The half adder is a combinational circuit that performs addition of two bits. It is designed conventionally by XOR and AND gates. When two inputs A and B are added, the Sum and Carry outputs are produced. The truth table of conventional half adder is shown in Table 1. The logic function for half adder is:

$$\text{Sum} = A'.B + A.B' \text{ which is exclusive-OR (XOR) function}$$

$$\text{Carry} = A.B, \text{ which is an (AND) function}$$

Thus, QCA majority logic can be written as:

$$\text{Sum} = m(m(A', B, 0), 1)$$

$$\text{Carry} = m(m(A, B, 0))$$

3.2.1. The First Design

QCA based half adder circuit proposed in this paper has been shown in Figure 5(a). A simulation result of the proposed design is shown in Figure 5(b). The simulation results of this gate have been checked using QCADesigner. The circuit is designed with the regular arrangement of QCA cells with proper latency. The proposed half-adder consists of 27 cells, area 0.03 μm^2 and latency 0.5 clock delays, which is less as compared to [27]-[29]. The simulation results of novel half adder circuits have been checked with Table 1. The advantage of computing with the truth table is that it ensures the computing process to generate same output.

3.2.2. The Second Design

Another QCA half-adder is shown in Figure 6(a) using fewer crossovers. The construction of the half-adder is very simple consists of homogeneous layer of cells. The sum is carried out with XOR gate and carry is carried out with AND gate. The proposed half-adder consists of 46 cells, area 0.06 μm^2 and total circuit latency of 1 clock delays. The simulation result of the proposed half-adder is shown in Figure 6(b).

Table 1. Truth table for conventional half adder.

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

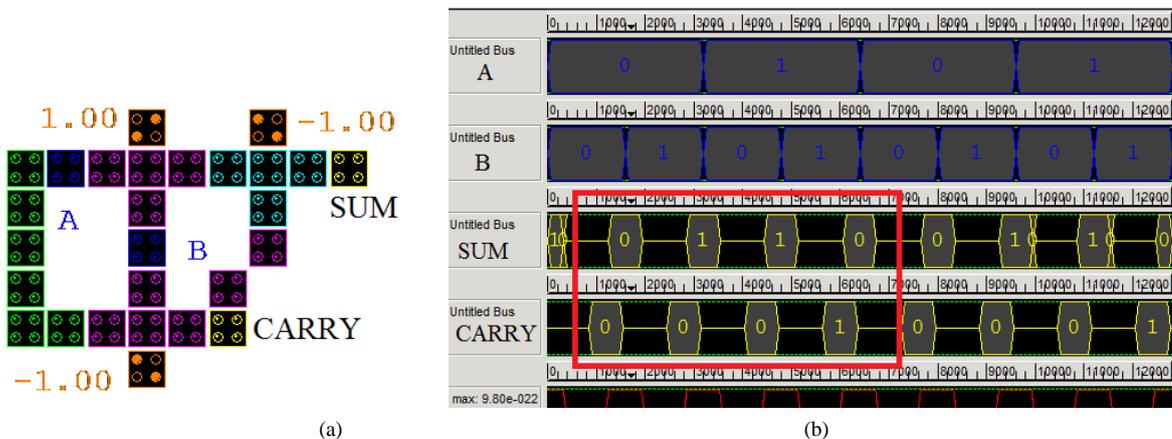


Figure 5. (a) QCA based half adder; (b) Simulation results.

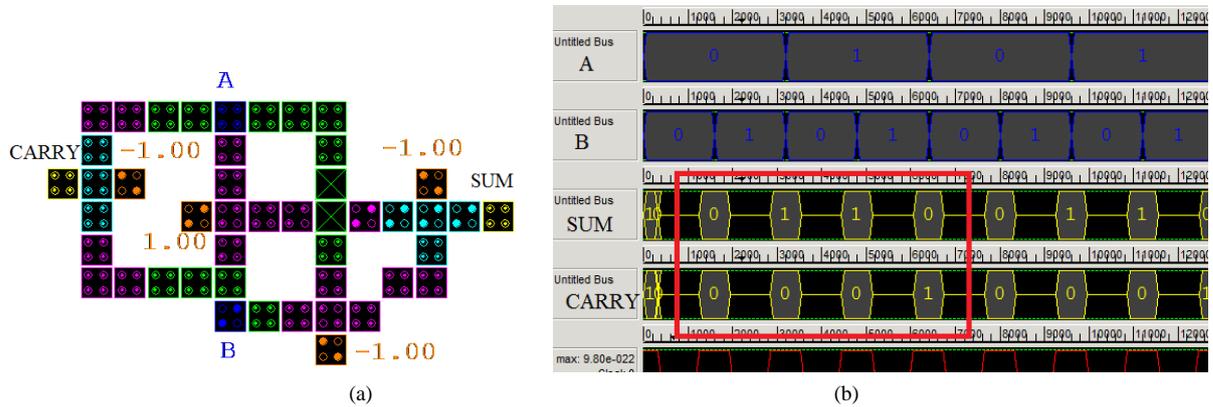


Figure 6. (a) QCA based half adder (b) Simulation results.

3.3. Proposed QCA Layout of Full Adders

Full adders are the main member of computational systems because adders can implement other operations. The proposed XOR design is applied to implement a QCA full adder. QCA implementation of full adders are presented in [30]-[36] has been used for comparison. The comparative study of QCA XOR gate, half adder, and full adder algorithm are given in Table 2.

The logic function of Majority full adder is expressed as:

$$M(A' M(M(B', C, 0), 1), 0), 1)$$

Sum can be represented in Majority logic as:

$$\text{Sum} = M[C'out, Cin, M(A, B, C' in)] \tag{1}$$

Carry Cout can be represented in Majority logic as:

$$\text{Cout} = M(A, B, Cin) \tag{2}$$

The logical truth table for conventional full adder is shown in Table 2.

3.3.1. The First Design

The QCA layout of the proposed full-adder is shown in Figure 7(a). The proposed full-adder circuit consists of less area and minimum crossovers. The circuit area of the proposed full-adder is $0.15 \mu\text{m}^2$, and circuit complexity of 120 cells, using total circuit latency of 2.5 clock delays. The simulation result of the proposed design is shown in Figure 7(b).

3.3.2. The Second Design

Figure 8(a) present the other proposed efficient QCA full adder with some inverter and Majority functions, the constructed using to the proposed design consists of no coplanar crossing connections. This QCA layout full adder consists of 69 cells and has $0.08 \mu\text{m}^2$ occupied area. The simulation result of proposed design is shown in Figure 8(b).

3.3.3. The Third Design

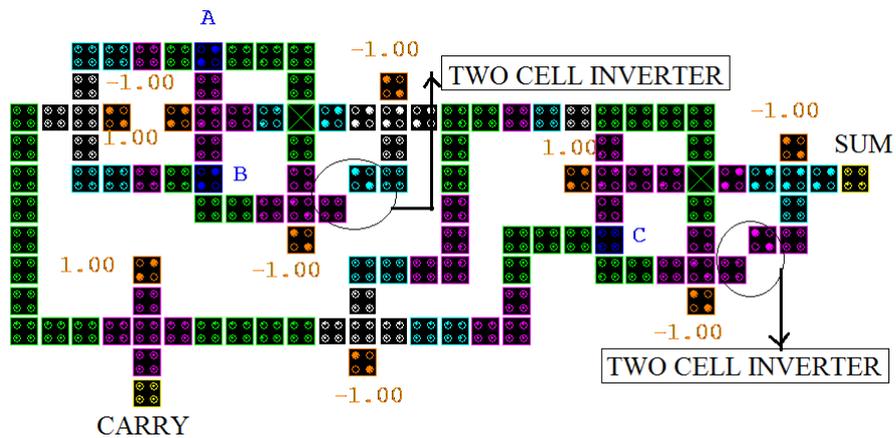
Figure 9(a) shows the QCA layout of other proposed full-adder designed basic majority gates and inverters. The simulation result of the proposed full-adder is shown in Figure 9(b). The design consists of basic cells with no crossovers or multilayer's. The circuit area of the proposed full-adder is $0.14 \mu\text{m}^2$, circuit complexity of 123 cells, and latency of 2 clock delays.

4. Comparison

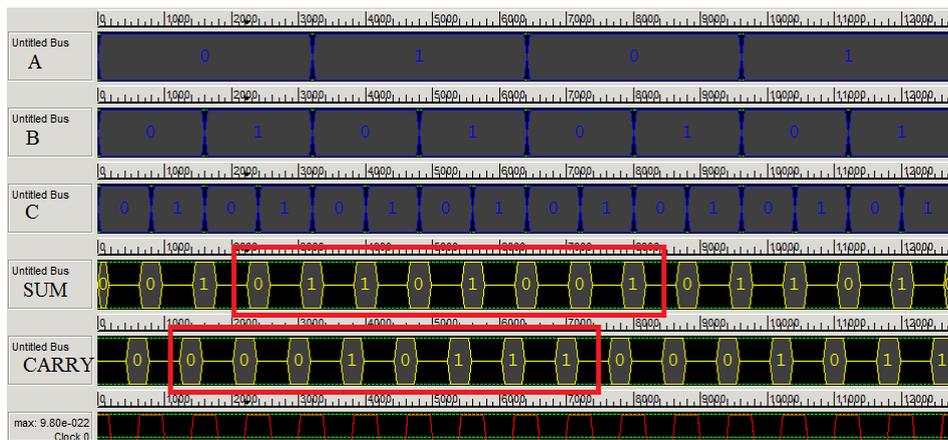
In this section, the proposed QCA XOR gate and its implementations for half adders and full adders have compared with conventional designs with regards delay, occupied area, and number of used QCA cells. The efficiency and robustness of these adders can verify according to circuit complexity, latency, and the area.

Table 2. Truth table for conventional full adder.

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



(a)



(b)

Figure 7. (a) QCA based full adder; (b) Simulation results.

Table 3 gives the comparative study of the proposed and conventional XOR gates and various adder circuits like half adders and full adders with regard to various parameters. The proposed XOR gate consists of less area, circuit complexity as compared to previous designs [15]. Researcher [17] has proposed the QCA implementation of half adder. The design needs either needs either coplanar crossovers or multiple layers to implement. We have proposed efficient half adders, which consists of fraction of area and less circuit complexity. In addition, it can be visualized that the proposed QCA layouts of adder circuits are better than the conventional designs because of low cell count and less multilayer connections. Some QCA full adders such as Zhang and Tougaw-Lent full adders occupy a large area because of using coplanar crossover connections and high cell count. It is clear from

the plotted graph shown in **Figure 10(a)** that the novel full adders enjoy the features of small area, superior performance factors in respect of area, latency, circuit stability, and low power dissipation than conventional designs present in [30]-[34]. The proposed designs show linear decrease of circuit area and improve the circuit efficiency. It can be seen that proposed structures are approximately 3-times smaller than conventional designs.

Figure 10(b) shows the comparative study of various structures in terms of latency (clock delays) and area occupied. Experiment results show that the performance of proposed designs is more efficient than conventional designs. For input/output synchronization, multiple crossovers, dummy wire channels are added to conventional designs show the worst performance.

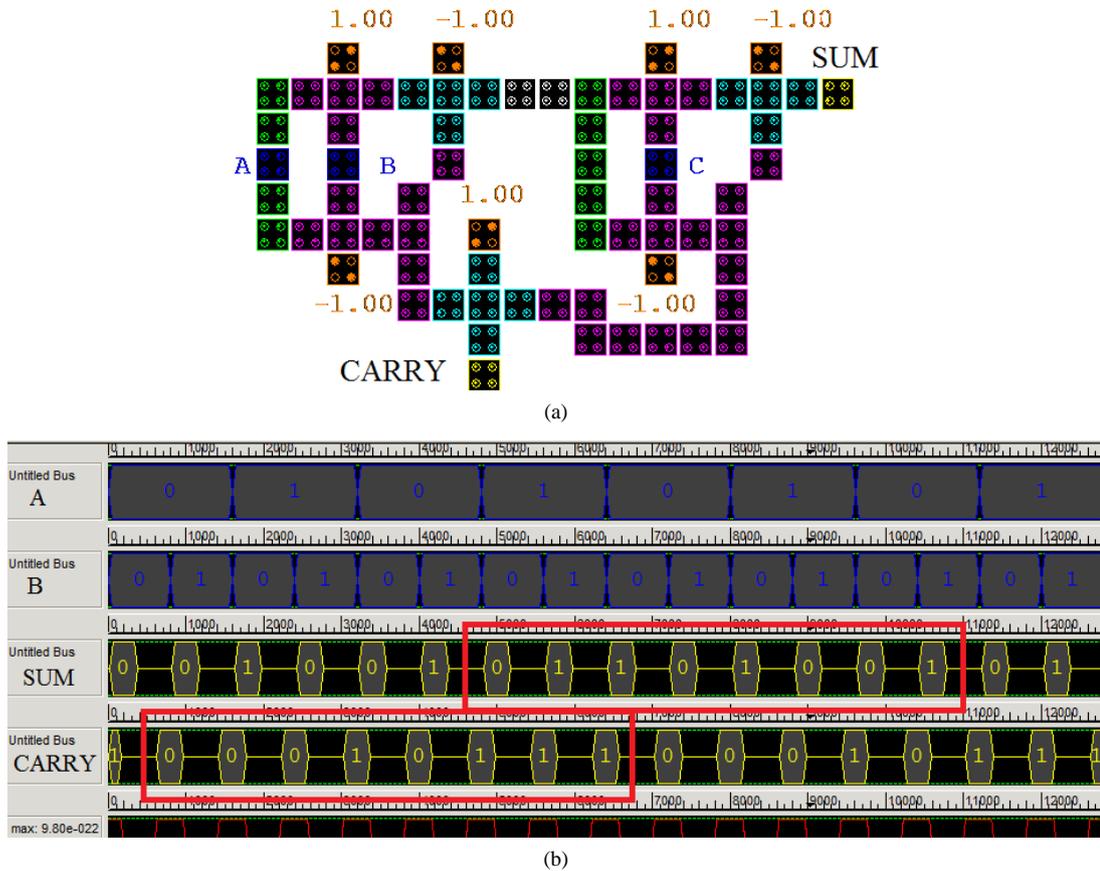


Figure 8. (a) QCA based full adder; (b) Simulation results.

Table 3. Comparative study of XOR gate and adder circuits with the results available in literature [15] [29] and [30]-[34].

QCA Structures	Previous Structures			Proposed Structures				
	Complexity	Area	Latency	Figures	Complexity	Area	Latency	
XOR gate [15]	34 cells	0.06 μm^2	1	Figure 4(a)	30 cells	0.03 μm^2	0.5	
Half adder [29]	77 cells	83160 $\text{nm}^2 = 0.08 \mu\text{m}^2$	1	Figure 5(a)	27 cells	0.03 μm^2	0.5	
	105 cells	108000 $\text{nm}^2 = 0.10 \mu\text{m}^2$	1	Figure 6(a)	46 cells	0.06 μm^2	1	
Full adders [30]	192 cells	0.20 μm^2	Not shown	Figure 7(a)	120 cells	0.15 μm^2	2.5	
	[31]	145 cells	0.17 μm^2	5	Figure 8(a)	69 cells	0.08 μm^2	1.5
	[32]	220 cells	0.36 μm^2	3	Figure 9(a)	123 cells	0.14 μm^2	2
	[33]	180 cells	0.22 μm^2	4				
	[34]	150 cells	2.25 μm^2	0.28				

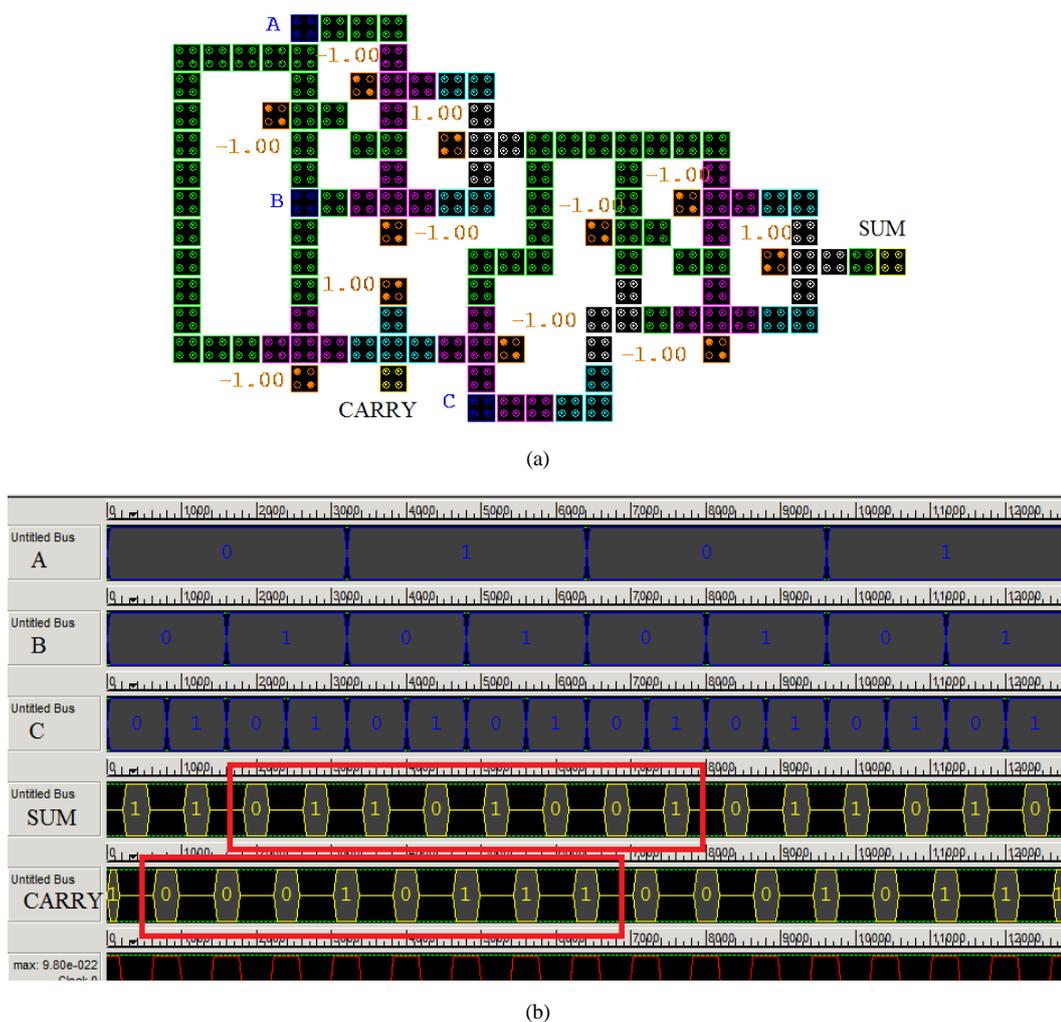


Figure 9. (a) QCA based full adder; (b) Simulation results.

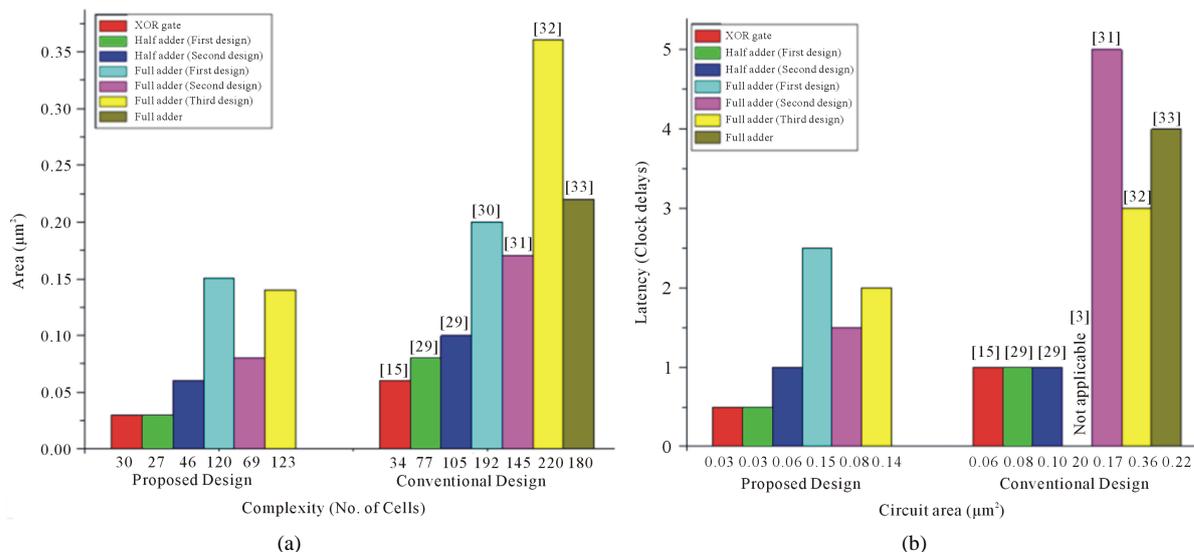


Figure 10. (a) Efficiency of proposed designs versus conventional designs (b) Area versus latency.

5. Conclusion

The proposed designs are a solution for implementations of QCA based circuits using minimum number of QCA cells, lesser clock delays and reduced area. This paper has demonstrated the design of improved QCA XOR gate and its implementations as novel adder structures, which will be useful as an efficient building block for larger arithmetic units. The simulation results of proposed (half/full) adder circuits have been verified using QCA Designer. These novel units have been found to have less practical latency and better throughput compared to the best corresponding cases found in the literature, the circuit area is found to be reduced to a fraction of the previous noise rejecting implementations. One aim of this paper is to design simple QCA structures with available basic gates with capable versatility and minimum garbage outputs susceptibility. In addition, results are verified by the truth table.

6. The Future Work

This paper has demonstrated the design of improved QCA XOR gate and its implementations as novel adder circuits, which will be useful as an efficient building block for larger arithmetic logic units (ALU) in future. In addition, the proposed designs are a solution for minimum number of QCA cells. The proposed architectural structures can be applied not only to general purpose processing, but to special purpose processing as well. The possibilities of applying the QCA technology to special purpose processing (such as digital signal processors) can also be explored. The QCA layouts and the simulation results are not only demonstrated but also analyzed for a clear understanding and facilitation of the future work. Control signal routing techniques above, work in the immediate future will have an extensive focus on methods for efficient interconnect and routing. Furthermore, an efficient and “safe” method of interconnect (*i.e.* one that avoids as much as possible the design problems) must be considered.

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